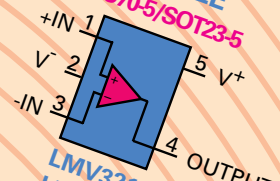
SMALLEST OP AMP & COMPARATOR IN THE WORLD THIS ONE'S FOR YOU!

LMV Products Qualification Package

Click Here For Web Info

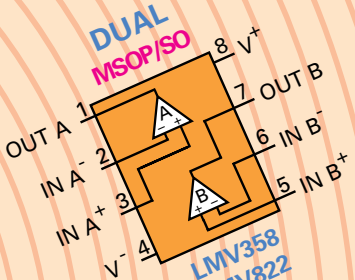
LMV321 LMV331 LMV821
LMV358 LMV393 LMV822
LMV324 LMV339 LMV824

SINGLE
SC70-5/SOT23-5



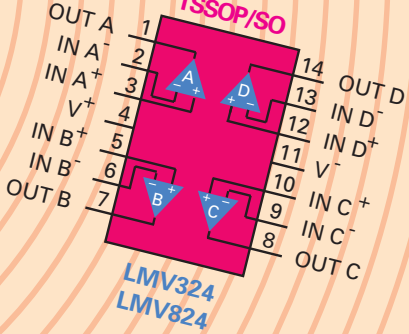
LMV321
LMV821
LMV331

DUAL
MSOP/SO



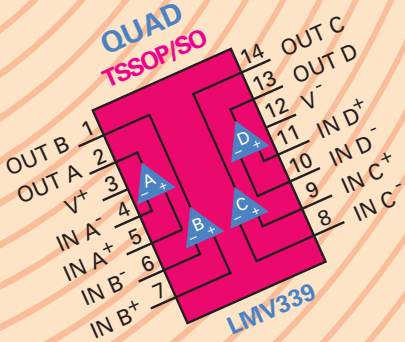
LMV358
LMV822
LMV393

QUAD
TSSOP/SO



LMV324
LMV824

QUAD
TSSOP/SO



LMV339

SPECS

- SC70-5 Package: 50% Smaller than SOT-23
- 2.7 to 5.5V Single Supply Operation
- Rail-to-Rail Output
- World's Smallest Op-Amp

National Semiconductor

WHAT CAN WE BUILD FOR YOU?™

National Semiconductor

LMV PRODUCTS
QUALIFICATION PACKAGE

March 1998

Table of Contents

1.0 INTRODUCTION

1.1 General Product Description

This qualification booklet covers a series of 9 products, 6 general purpose Op Amps and 3 general purpose Comparators. Each are available in 2 different package types for a total of 18 product/package combinations.

Quad Op Amp	LMV324M/MX (14 lead SOIC package) LMV324MT/MTX (14 lead TSSOP package)
	LMV824M/MX (14 lead SOIC package) LMV824MT/MTX (14 lead TSSOP package)
Dual Op Amp	LMV358M/MX (8 lead SOIC package) LMV358MM/MMX (8 lead MSOP package)
	LMV822M/MX (8 lead SOIC package) LMV822MM/MMX (8 lead MSOP package)
Single Op Amp	LMV321 M5/M5X (5 lead SOT-23 package) LMV321M7/M7X (5 lead SC70 package)
	LMV821 M5/M5X (5 lead SOT-23 package) LMV821 M7/M7X (5 lead SC70 package)
Quad Comparator	LMV339M/MX (14 lead SOIC package) LMV339MT/MTX (14 lead TSSOP package)
Dual Comparator	LMV393M/MX (8 lead SOIC package) LMV393MM/MMX (8 lead MSOP package)
Single Comparator	LMV331 M5/M5X (5 lead SOT-23 package) LMV331 M7/M7X (5 lead SC70 package)

They feature low voltage operation (2.7V to 5.0V for LMV300 series and 2.5V to 5.0V for LMV800 series) and are designed for applications where low power, small size, and price are main objectives. LMV800 series Op Amps offers enhanced performance over that of LMV300 series Op Amps.

1.2 Technical Product Description

All 9 products are manufactured using National's advanced Submicron Silicon Gate BiCMOS process. Internal name for this process is CS80CBi, which uses 6 inch wafers.

Actual silicon processing flow (oxide growths, implants, etching, etc.) are the same for all 9 products.

LMV300 Series

LMV358, LMV393, are metalization mask options of the **LMV324**, sharing previous mask steps in common with **LMV324.**
LMV324, LMV358, and LMV393 all have a die size of 23mils X 28mils.

LMV321 uses different mask set (different than LMV324), and the **LMV331** is a metalization mask option of the LMV321, sharing previous mask steps in common with LMV321.
LMV321 and LMV331 have a die size of 17mils X 17mils.

LMV339 uses it's own dedicated mask set (separate from LMV324 or LMV321 mask set).
LMV339 has a die size of 23mils X 28mils.

LMV800 Series

LMV822 is a metalization option of **LMV824**.
LMV824 and LMV822 both have a die size of 24mils X 34mils.

LMV821 uses it's own dedicated mask set (seperate from LMV824 mask set).
LMV821 has a die size of 19mils X 19mils.

1.3 Reliability/Qualification Overview

SC70 Package

The 5 lead SC70 package (used in LMV321M7/M7X, LMV821M7/M7X and LMV331M7/M7X) is new in the industry of linear integrated circuits. Other package types used for LMV300 and LMV800 series have been released previously.

The LMV321 was used as a qualification vehicle for this package and went through full package reliability (see Reliability Test Report FEM19970494 later in this qualification booklet under Reliability Reports section 5.0). Qualification of LMV321, LMV821, and LMV331 for use in SC70 package is covered by FEM19970494.

LMV300 and LMV800 Series

Because of same wafer fab process used on all 9 products, die layout simialrities, and same package types, the entire series was qualified by selecting particular products for actual reliabilty testing and qualifying the others by extension. (Qualifying by extension is a standard practice in the semiconductor industry.) Copies of all Reliability Test Reports listed below can below can be found under Reliability Reports section 5.0 later in this qualification booklet.

In Summary:

FSC19970377	LMV324 in SOIC and TSSOP packages LMV358 in MSOP package
FSC19980030	LMV824 in TSSOP package
FEM19970494	LMV321 in SC70 package
FEM19970440	LMV321 in SOT-23 package
FSC19980031	LMV821 in MDIP package
FSC19980093	LMV339 in SOIC package LMV393 in SOIC package LMV331 in SOT-23 package

1.4 Technical Assistance

Product Engineers

LMV324 and LMV358	Frank Smoot email: frank.smoot@nsc.com Tel: 408.721.5025
LMV824, LMV822, and LMV821	Altaf Ahmad email: altaf.ahmad@nsc.com Tel: 408.721.5957
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LMV339, LMV393, and LMV331	Doug Simin email: doug.simin@nsc.com Tel: 408.721.3245

Applications Engineers

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LMV824, LMV822, and LMV821	Kelly Flaherty email: kelly.flaherty@nsc.com Tel: 408.721.8390
LMV339, LMV393, and LMV331	Muna Acosta email: muna.acosta@nsc.com Tel: 408.721.5517

1.0 INTRODUCTION

2.0 DEVICE INFORMATION

2.1 DATASHEETS

2.1.1 LMV321/358/324 Datasheet

National Semiconductor

March 1998

LMV321 Single/ LMV358 Dual/ LMV324 Quad General Purpose, Low Voltage, Rail-to-Rail Output Operational Amplifiers

General Description

The LMV358/324 are low voltage (2.7–5.5V) versions of the dual and quad commodity op amps, LM358/324, which currently operate at 5–30V. The LMV321 is the single version.

The LMV321/358/324 are the most cost effective solutions for the applications where low voltage operation, space saving and low price are needed. They offer specifications that meet or exceed the familiar LM358/324. The LMV321/358/324 have rail-to-rail output swing capability and the input common-mode voltage range includes ground. They all exhibit excellent speed-power ratio, achieving 1 MHz of bandwidth and 1 V/µs of slew rate with low supply current.

The LMV321 is available in space saving SC70-5, which is approximately half the size of SOT23-5. The small package saves space on pc boards, and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

The chips are built with National's advanced submicron silicon-gate BiCMOS process. The LMV321/358/324 have bipolar input and output stages for improved noise performance and higher output current drive.

Features

(For V^+ = 5V and V^- = 0V, Typical Unless Otherwise Noted)

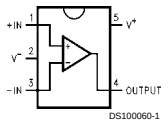
- Guaranteed 2.7V and 5V Performance
- No Crossover Distortion
- Space Saving Package — SC70-5 2.0x2.1x1.0mm
- Industrial Temp.Range — −40˚C to +85˚C
- Gain-Bandwidth Product — 1MHz
- Low Supply Current
  - LMV321 — 130µA
  - LMV358 — 210µA
  - LMV324 — 410µA
- Rail-to-Rail Output Swing @ 10kΩ Load — V^+−10mV; V^-+65mV
- V_{CM} — −0.2V to V^+ −0.8V

Applications

- Active Filters
- General Purpose Low Voltage Applications
- General Purpose Portable Devices

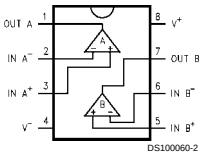
Connection Diagrams

5-Pin SC70-5/SOT23-5



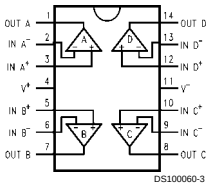
Top View

8-Pin SO/MSOP



Top View

14-Pin SO/TSSOP



Top View

2.0 DEVICE INFORMATION

Ordering Information

Package	Temperature Range Industrial −40˚C to +85˚C	Packaging Marking	Transport Media	NSC Drawing
5-Pin SC70-5	LMV321M7	A12	250 Units Tape and Reel	MAA05
	LMV321M7X	A12	3k Units Tape and Reel	
5-Pin SOT23-5	LMV321M5	A13	250 Units Tape and Reel	MA05B
	LMV321M5X	A13	3k Units Tape and Reel	
8-Pin Small Outline	LMV358M	LMV358M	Rails	M08A
	LMV358MX	LMV358M	2.5k Units Tape and Reel	
8-Pin MSOP	LMV358MM	V358	250 Units Tape and Reel	MUA08A
	LMV358MMX	V358	3.5k Units Tape and Reel	
14-Pin Small Outline	LMV324M	LMV324M	Rails	M14A
	LMV324MX	LMV324M	2.5k Units Tape and Reel	
14-Pin TSSOP	LMV324MT	LMV324MT	Rails	MTC14
	LMV324MTX	LMV324MT	2.5k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	100V
Human Body Model LMV358/324	2000V
LMV321	900V
Differential Input Voltage	± Supply Voltage
Supply Voltage (V^+–V^-)	5.5V
Output Short Circuit to V^+	(Note 3)
Output Short Circuit to V^-	(Note 4)
Mounting Temp.	
Lead Temp. (Soldering,10 sec)	260˚C
Infrared (15 sec)	215˚C
Storage Temp. Range	−65˚C to 150˚C
Junction Temp. (T_j, max) (Note 5)	150˚C

Operating Ratings (Note 1)

Supply Voltage	2.7V to 5.5V
Temperature Range	
LMV321, LMV358, LMV324	−40˚C≤T_J≤85˚C
Thermal Resistance (θ_{JA})(Note 10)	
5-pin SC70-5	478˚C/W
5-pin SOT23-5	265˚C/W
8-Pin SOIC	190˚C/W
8-Pin MSOP	235˚C/W
14-Pin SOIC	145˚C/W
14-Pin TSSOP	155˚C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = V^+/2 and R_L > 1 MΩ.

Symbol	Parameter	Conditions	Typ (Note 6)	Limit (Note 7)	Units
V_{OS}	Input Offset Voltage		1.7	7	mV max
TCV_{OS}	Input Offset Voltage Average Drift		5		µV/˚C
I_B	Input Bias Current		11	250	nA max
I_{OS}	Input Offset Current		5	50	nA max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.7V	63	50	dB min
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V V_O = 1V	60	50	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR≥50dB	−0.2	0	V min
			1.9	1.7	V max
V_O	Output Swing	R_L = 10kΩ to 1.35V	V^+ -10	V^+ -100	mV min
			60	180	mV max
I_S	Supply Current	LMV321	80	170	µA max
		LMV358 Both amplifiers	140	340	µA max
		LMV324 All four amplifiers	260	680	µA max

2.0 DEVICE INFORMATION

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = V^+/2 and R_L > 1 MΩ.

Symbol	Parameter	Conditions	Typ (Note 6)	Limit (Note 7)	Units
GBWP	Gain-Bandwidth Product	C_L = 200 pF	1		MHz
Φ_m	Phase Margin		60		Deg
G_m	Gain Margin		10		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	46		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.17		$\frac{pA}{\sqrt{Hz}}$

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = V^+/2 and R_L > 1 MΩ.
Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 6)	Limit (Note 7)	Units
V_{OS}	Input Offset Voltage		1.7	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		5		µV/˚C
I_B	Input Bias Current		15	250 **500**	nA max
I_{OS}	Input Offset Current		5	50 **150**	nA max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4V	65	50	dB min
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V V_O = 1V V_{CM} = 1V	60	50	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR≥50dB	−0.2	0	V min
			4.2	4	V max
A_V	Large Signal Voltage Gain (Note 8)	R_L = 2kΩ	100	15 **10**	V/mV min
V_O	Output Swing	R_L = 2kΩ to 2.5V	V^+ -40	V^+ -300 **V^+ -400**	mV min
			120	300 **400**	mV max
		R_L = 10kΩ to 2.5V	V^+ -10	V^+ -100 **V^+ -200**	mV min
			65	180 **280**	mV max
I_O	Output Short Circuit Current	Sourcing, V_O = 0V	60	5	mA min
		Sinking, V_O = 5V	160	10	mA min
I_S	Supply Current	LMV321	130	250 **350**	µA max
		LMV358 Both amplifiers	210	440 **615**	µA max
		LMV324 All four amplifiers	410	830 **1160**	µA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 6)	Limit (Note 7)	Units
SR	Slew Rate	(Note 9)	1		V/µs
GBWP	Gain-Bandwidth Product	C_L = 200 pF	1		MHz
Φ_m	Phase Margin		60		Deg
G_m	Gain Margin		10		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz,	39		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.21		$\frac{pA}{\sqrt{Hz}}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. Machine model, 0Ω in series with 200 pF.

Note 3: Shorting output to V^+ will adversely affect reliability.

Note 4: Shorting output to V^- will adversely affect reliability.

Note 5: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}-T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 6: Typical values represent the most likely parametric norm.

Note 7: All limits are guaranteed by testing or statistical analysis.

Note 8: R_L is connected to V^-. The output voltage is 0.5V ≤ V_O ≤ 4.5V.

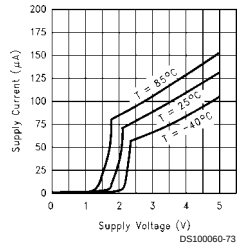
Note 9: Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.

Note 10: All numbers are typical, and apply for packages soldered directly onto a PC board in still air.

Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C.

Supply Current vs Supply Voltage (LMV321)



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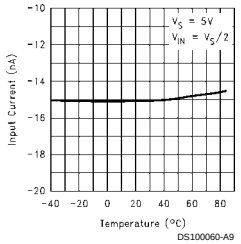
Input Current vs Temperature



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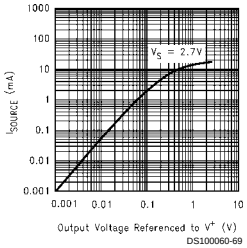
Sourcing Current vs Output Voltage



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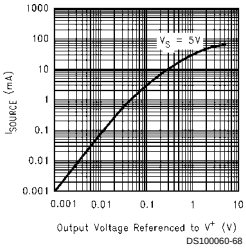
Sourcing Current vs Output Voltage



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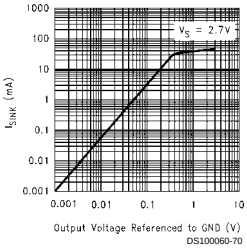
Sinking Current vs Output Voltage



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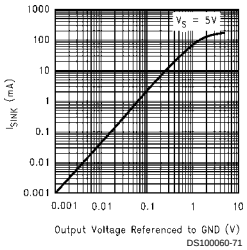
Sinking Current vs Output Voltage

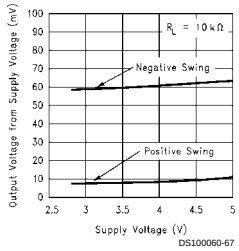


DS100060-71

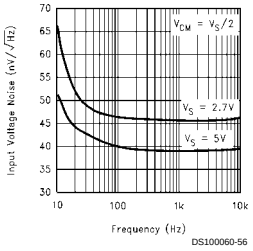
Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

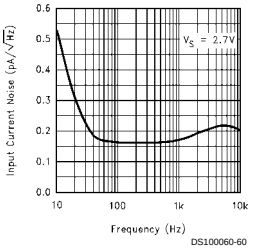
Output Voltage Swing vs Supply Voltage



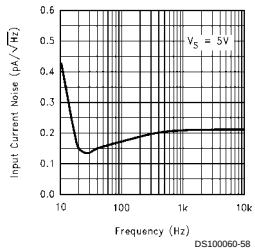
Input Voltage Noise vs Frequency



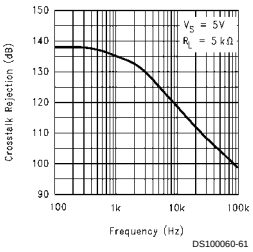
Input Current Noise vs Frequency



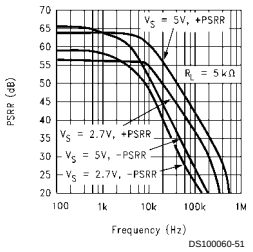
Input Current Noise vs Frequency



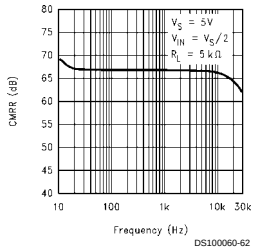
Crosstalk Rejection vs Frequency



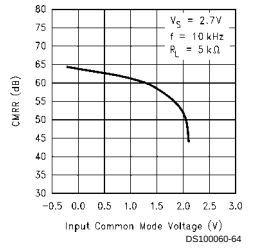
PSRR vs Frequency



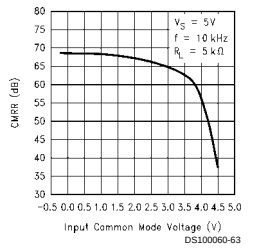
CMRR vs Frequency



CMRR vs Input Common Mode Voltage



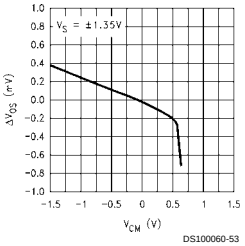
CMRR vs Input Common Mode Voltage



Typical Performance Characteristics

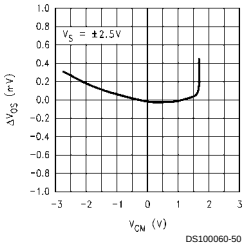
Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

Δ V_{OS} vs CMR



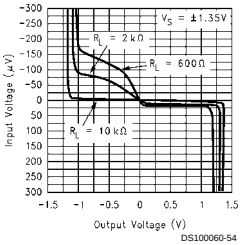
DS100060-53

Δ V_{OS} vs CMR



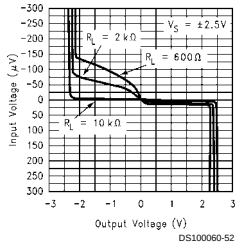
DS100060-50

Input Voltage vs Output Voltage



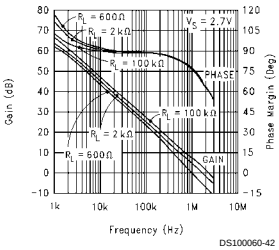
DS100060-54

Input Voltage vs Output Voltage



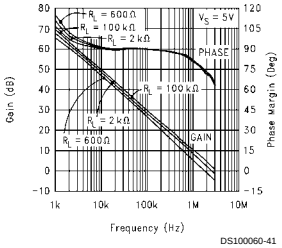
DS100060-52

Open Loop Frequency Response



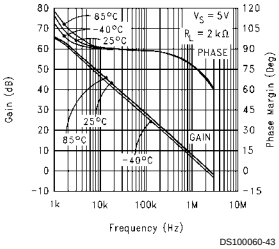
DS100060-42

Open Loop Frequency Response



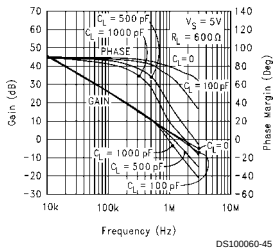
DS100060-41

Open Loop Frequency Response vs Temperature



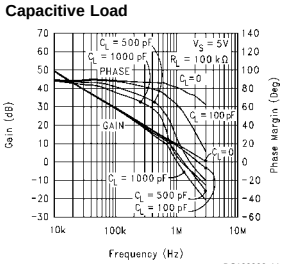
DS100060-43

Gain and Phase vs Capacitive Load



DS100060-45

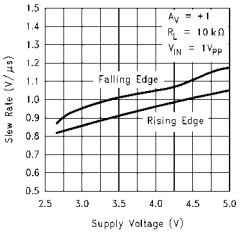
Gain and Phase vs Capacitive Load



DS100060-44

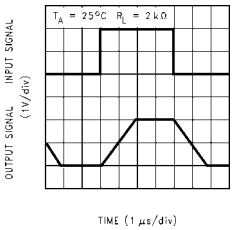
Typical Performance Characteristics Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

Slew Rate vs Supply Voltage



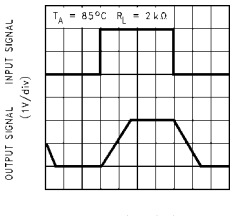
DS100060-57

Non-Inverting Large Signal Pulse Response



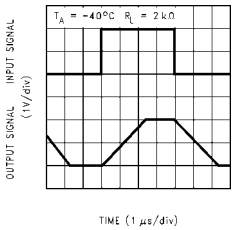
DS100060-88

Non-Inverting Large Signal Pulse Response



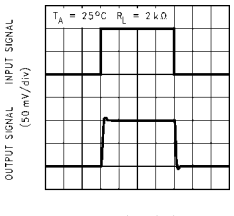
DS100060-A1

Non-Inverting Large Signal Pulse Response



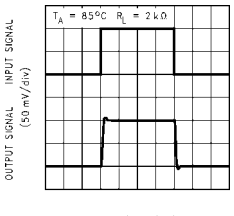
DS100060-A0

Non-Inverting Small Signal Pulse Response



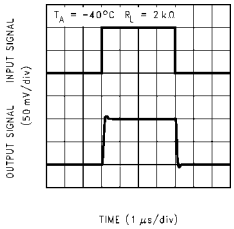
DS100060-89

Non-Inverting Small Signal Pulse Response



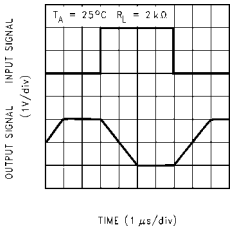
DS100060-A2

Non-Inverting Small Signal Pulse Response



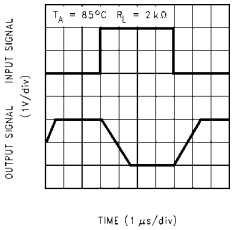
DS100060-A3

Inverting Large Signal Pulse Response



DS100060-90

Inverting Large Signal Pulse Response

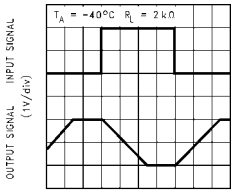


DS100060-A4

Typical Performance Characteristics

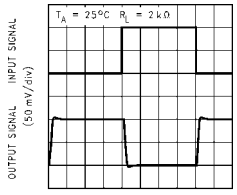
Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

Inverting Large Signal Pulse Response



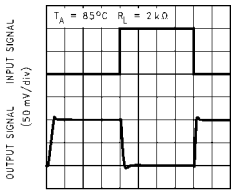
DS100060-A5

Inverting Small Signal Pulse Response



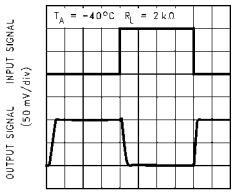
DS100060-91

Inverting Small Signal Pulse Response



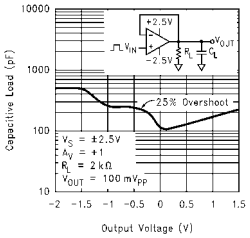
DS100060-A6

Inverting Small Signal Pulse Response



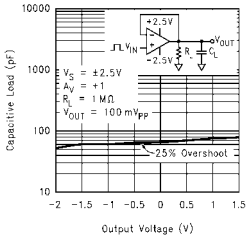
DS100060-A7

Stability vs Capacitive Load



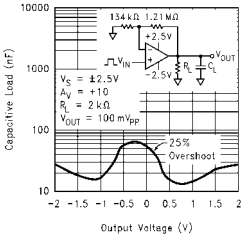
DS100060-46

Stability vs Capacitive Load



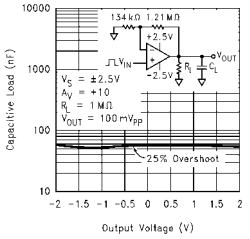
DS100060-47

Stability vs Capacitive Load



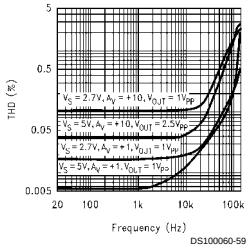
DS100060-49

Stability vs Capacitive Load



DS100060-48

THD vs Frequency

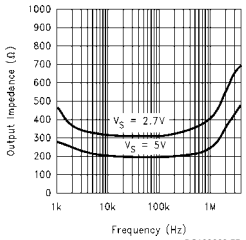


DS100060-59

Typical Performance Characteristics

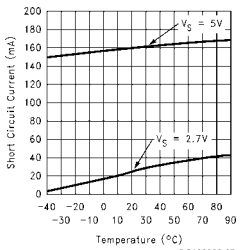
Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

Open Loop Output Impedance vs Frequency



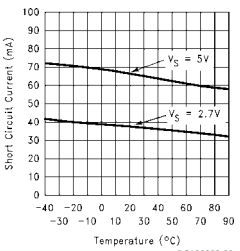
DS100060-55

Short Circuit Current vs Temperature (Sinking)



DS100060-65

Short Circuit Current vs Temperature (Sourcing)



DS100060-66

Application Notes

1.0 Benefits of the LMV321/358/324

Size. The small footprints of the LMV321/358/324 packages save space on printed circuit boards, and enable the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. The low profile of the LMV321/358/324 make them possible to use in PCMCIA type III cards.

Signal Integrity. Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the LMV321/358/324 can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

Simplified Board Layout. These products help you to avoid using long pc traces in your pc board layout. This means that no additional components, such as capacitors and resistors, are needed to filter out the unwanted signals due to the interference between the long pc traces.

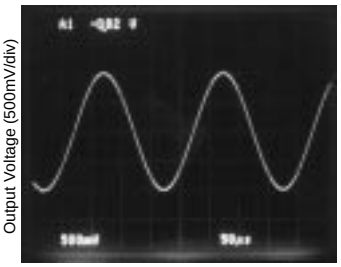
Low Supply Current. These devices will help you to maximize battery life. They are ideal for battery powered systems.

Low Supply Voltage. National provides guaranteed performance at 2.7V and 5V. These guarantees ensure operation throughout the battery lifetime.

Rail-to-Rail Output. Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

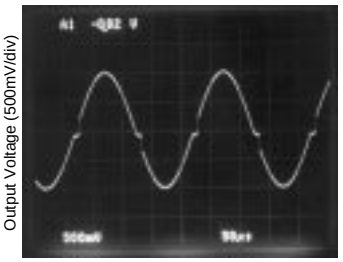
Input Includes Ground. Allows direct sensing near GND in single supply operation.

Ease of Use & No Crossover Distortion. The LMV321/358/324 offer specifications similar to the familiar LM324. In addition, the new LMV321/358/324 effectively eliminate the output crossover distortion. The scope photos in *Figure 1* and *Figure 2* compare the output swing of the LMV324 and the LM324 in a voltage follower configuration, with V_S = ± 2.5V and R_L (= 2kΩ) connected to GND. It is apparent that the crossover distortion has been eliminated in the new LMV324.



DS100060-97

FIGURE 1. Output Swing of LMV324



DS100060-98

FIGURE 2. Output Swing of LM324

2.0 Capacitive Load Tolerance

The LMV321/358/324 can directly drive 200 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive

Application Notes (Continued)

load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, circuit in *Figure 3* can be used.

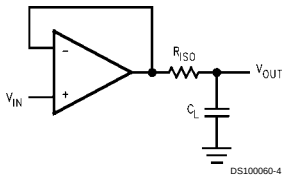


FIGURE 3. Indirectly Driving A Capacitive Load Using Resistive Isolation

In *Figure 3* , the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable Vout will be. *Figure 4* is an output waveform of *Figure 3* using 620Ω for R_{ISO} and 510 pF for C_L.

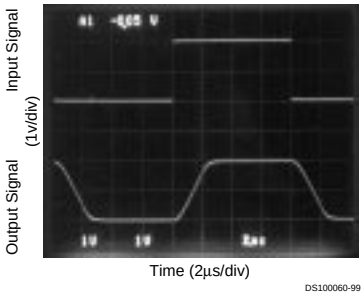


FIGURE 4. Pulse Response of the LMV324 Circuit in Figure 3

The circuit in *Figure 5* is an improvement to the one in *Figure 3* because it provides DC accuracy as well as AC stability. If there were a load resistor in *Figure 3*, the output would be voltage divided by R_{ISO} and the load resistor. Instead, in *Figure 5*, R_F provides the DC accuracy by using feed-forward techniques to connect V_{IN} to R_L. Caution is needed in choosing the value of R_F due to the input bias current of the LMV321/358/324. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of C_F . This in turn will slow down the pulse response.

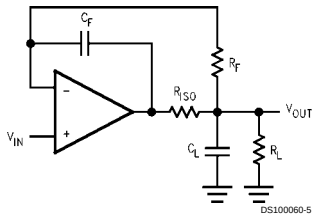


FIGURE 5. Indirectly Driving A Capacitive Load with DC Accuracy

3.0 Input Bias Current Cancellation

The LMV321/358/324 family has a bipolar input stage. The typical input bias current of LMV321/358/324 is 15 nA with 5V supply. Thus a 100 kΩ input resistor will cause 1.5 mV of error voltage. By balancing the resistor values at both inverting and non-inverting inputs, the error caused by the amplifier's input bias current will be reduced. The circuit in *Figure 6* shows how to cancel the error caused by input bias current.

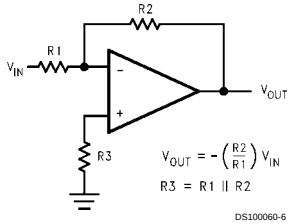


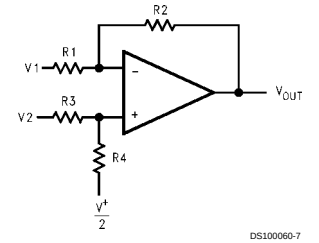
FIGURE 6. Cancelling the Error Caused by Input Bias Current

4.0 Typical Single-Supply Application Circuits

4.1 Difference Amplifier

The difference amplifier allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to two inputs. It is useful as a computational amplifier, in making a differential to single-ended conversion or in rejecting a common mode signal.

Application Notes (Continued)



$$V_{OUT} = \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R4}{R1}V_2 - \frac{R2}{R1}V_1 + \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R3}{R1} \cdot \frac{V^+}{2}$$

for R1 = R3 and R2 = R4

$$V_{OUT} = \frac{R2}{R1}(V_2 - V_1) + \frac{V^+}{2}$$

DS100060-19

FIGURE 7. Difference Amplifier

4.2 Instrumentation Circuits

The input impedance of the previous difference amplifier is set by the resistors R_1, R_2, R_3, and R_4. To eliminate the problems of low input impedance, one way is to use a voltage follower ahead of each input as shown in the following two instrumentation amplifiers.

4.2.1 Three-op-amp Instrumentation Amplifier

The quad LMV324 can be used to build a three-op-amp instrumentation amplifier as shown in *Figure 8*.

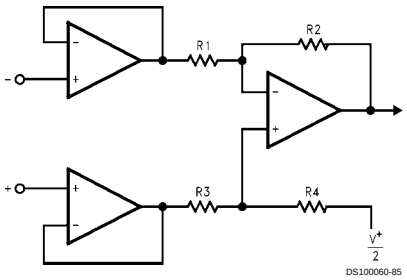
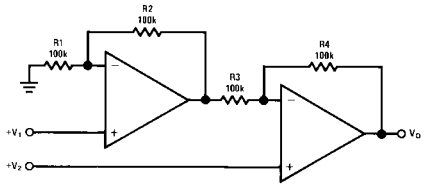


FIGURE 8. Three-op-amp Instrumentation Amplifier

The first stage of this instrumentation amplifier is a differential-input, differential-output amplifier, with two voltage followers. These two voltage followers assure that the input impedance is over 100 MΩ. The gain of this instrumentation amplifier is set by the ratio of R_2/R_1. R_3 should equal R_1, and R_4 equal R_2. Matching of R_3 to R_1 and R_4 to R_2 affects the CMRR. For good CMRR over temperature, low drift resistors should be used. Making R_4 slightly smaller than R_2 and adding a trim pot equal to twice the difference between R_2 and R_4 will allow the CMRR to be adjusted for optimum.

4.2.2 Two-op-amp Instrumentation Amplifier

A two-op-amp instrumentation amplifier can also be used to make a high-input-impedance dc differential amplifier (*Figure 9*) . As in the three-op-amp circuit, this instrumentation amplifier requires precise resistor matching for good CMRR. R4 should equal to R1 and R3 should equal R2.



$$V_O = \left(1 + \frac{R4}{R3}\right)(V_2 - V_1), \text{ where } R1 = R4 \text{ and } R2 = R3$$

As shown: $V_O = 2(V_2 - V_1)$

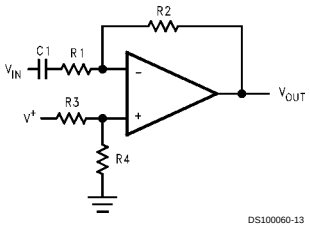
DS100060-35

FIGURE 9. Two-Op-amp Instrumentation Amplifier

4.3 Single-Supply Inverting Amplifier

There may be cases where the input signal going into the amplifier is negative. Because the amplifier is operating in single supply voltage, a voltage divider using R_3 and R_4 is implemented to bias the amplifier so the input signal is within the input common-mode voltage range of the amplifier. The capacitor C_1 is placed between the inverting input and resistor R_1 to block the DC signal going into the AC signal source, V_{IN}. The values of R_1 and C_1 affect the cutoff frequency, fc = $1/2\pi R_1 C_1$.

As a result, the output signal is centered around mid-supply (if the voltage divider provides $V^+/2$ at the non-inverting input). The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system.



$$V_{OUT} = -\frac{R2}{R1}V_{IN}$$

DS100060-20

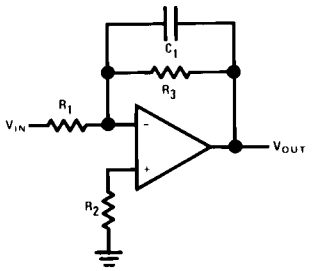
FIGURE 10. Single-Supply Inverting Amplifier

4.4 Active Filter

4.4.1 Simple Low-Pass Active Filter

The simple low-pass filter is shown in *Figure 11*. Its low-frequency gain ($\omega \rightarrow 0$) is defined by $-R_3/R_1$. This allows low-frequency gains other than unity to be obtained. The filter has a -20dB/decade roll-off after its corner frequency fc. R_2 should be chosen equal to the parallel combination of R_1 and R_3 to minimize errors due to bias current. The frequency response of the filter is shown in *Figure 12*.

Application Notes (Continued)



$$A_L = -\frac{R_3}{R_1}$$

$$f_c = \frac{1}{2\pi R_3 C_1}$$

$$R_2 = R_1 \,||\, R_3$$

DS100060-37

FIGURE 11. Simple Low-Pass Active Filter

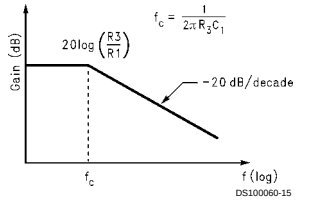


FIGURE 12. Frequency Response of Simple Low-Pass Active Filter in Figure 11

Note that the single-op-amp active filters are used in to the applications that require low quality factor, Q(≤ 10), low frequency (≤ 5 kHz), and low gain (≤ 10), or a small value for the product of gain times Q (≤ 100). The op amp should have an open loop voltage gain at the highest frequency of interest at least 50 times larger than the gain of the filter at this frequency. In addition, the selected op amp should have a slew rate that meets the following requirement:

$$\text{SlewRate} \geq 0.5 \times (\omega_H V_{OPP}) \times 10^{-6} \text{ V/µsec}$$

where ω_H is the highest frequency of interest, and V_{opp} is the output peak-to-peak voltage.

4.4.2 Sallen-Key 2nd-Order Active Low-Pass Filter

The Sallen-Key 2nd-order active low-pass filter is illustrated in *Figure 13*. The dc gain of the filter is expressed as

$$A_{LP} = \frac{R_3}{R_4} + 1 \tag{1}$$

Its transfer function is

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{\frac{1}{C_1 C_2 R_1 R_2} A_{LP}}{S^2 + S\left(\frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} - \frac{A_{LP}}{C_2 R_2}\right) + \frac{1}{C_1 C_2 R_1 R_2}} \tag{2}$$

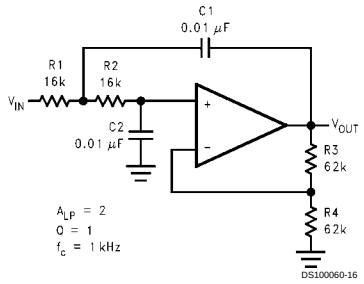


FIGURE 13. Sallen-Key 2nd-Order Active Low-Pass Filter

The following paragraphs explain how to select values for R_1, R_2, R_3, R_4, C_1, and C_2 for given filter requirements, such as A_{LP}, Q, and f_c.

The standard form for a 2nd-order low pass filter is

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{A_{LP}\,\omega_c^2}{S^2 + \left(\frac{\omega_c}{Q}\right)S + \omega_c^2} \tag{3}$$

where

Q: Pole Quality Factor

ω_C: Corner Frequency

Comparison between the *Equation (2)* and *Equation (3)* yields

$$\omega_c^2 = \frac{1}{C_1 C_2 R_1 R_2} \tag{4}$$

$$\frac{\omega_c}{Q} = \frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} - \frac{A_{LP}}{C_2 R_2} \tag{5}$$

To reduce the required calculations in filter design, it is convenient to introduce normalization into the components and design parameters. To normalize, let $\omega_C = \omega_n$ = 1rad/s, and $C_1 = C_2 = C_n$ = 1F, and substitute these values into *Equation (4)* and *Equation (5)*. From *Equation (4)*, we obtain

$$R_1 = \frac{1}{R_2} \tag{6}$$

From *Equation (5)*, we obtain

$$R_2 = \frac{1 \pm \sqrt{1 - 4Q^2(2 - A_{LP})}}{2Q} \tag{7}$$

For minimum dc offset, V+ = V-, the resistor values at both inverting and non-inverting inputs should be equal, which means

$$R_1 + R_2 = \frac{R_3 R_4}{R_3 + R_4} \tag{8}$$

From *Equation (1)* and *Equation (8)*, we obtain

$$R_3 = (R_1 + R_2)A_{LP} \tag{9}$$

Application Notes (Continued)

$$R_4 = \left(\frac{A_{LP}}{A_{LP}-1}\right)(R_1 + R_2) \quad (10)$$

The values of C_1 and C_2 are normally close to or equal to

$$C = \frac{10}{f_c}\ \mu F$$

As a design example:

Require: A_{LP} = 2, Q = 1, fc = 1KHz

Start by selecting C1 and C2. Choose a standard value that is close to

$$C = \frac{10}{f_c}\ \mu F$$

$$C_1 = C_2 = \frac{10}{1 \times 10^3}\ \mu F = 0.01\ \mu F$$

From *Equations (6), (7), (9), (10)*,

R_1= 1Ω

R_2= 1Ω

R_3= 4Ω

R_4= 4Ω

The above resistor values are normalized values with ω_n=1rad/s and $C_1 = C_2 = C_n$ = 1F. To scale the normalized cut-off frequency and resistances to the real values, two scaling factors are introduced, frequency scaling factor (k_f) and impedance scaling factor (k_m).

$$k_f = \frac{\omega_c}{\omega_n} = \frac{2\pi \times 1 \times 10^3}{1} = 2\pi \times 10^3$$

$$k_m k_f = \frac{Cn}{C1}$$

$$k_m = 1.59 \times 10^4$$

Scaled values:

$R_2 = R_1$ = 15.9 kΩ

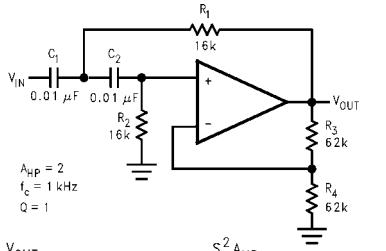
$R_3 = R_4$ = 63.6 kΩ

$C_1 = C_2$ = 0.01 µF

An adjustment to the scaling may be made in order to have realistic values for resistors and capacitors. The actual value used for each component is shown in the circuit.

4.4.3 2nd-order High Pass Filter

A 2nd-order high pass filter can be built by simply interchanging those frequency selective components (R_1, R_2, C_1, C_2) in the Sallen-Key 2nd-order active low pass filter. As shown in *Figure 14*, resistors become capacitors, and capacitors become resistors. The resulted high pass filter has the same corner frequency and the same maximum gain as the previous 2nd-order low pass filter if the same components are chosen.



$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{S^2 A_{HP}}{S^2 + S\left(\frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} + \frac{(1 - A_{HP})}{C_1 R_1}\right) + \frac{1}{C_1 C_2 R_1 R_2}}$$

Where $A_{HP} = 1 + \frac{R_3}{R_4}$

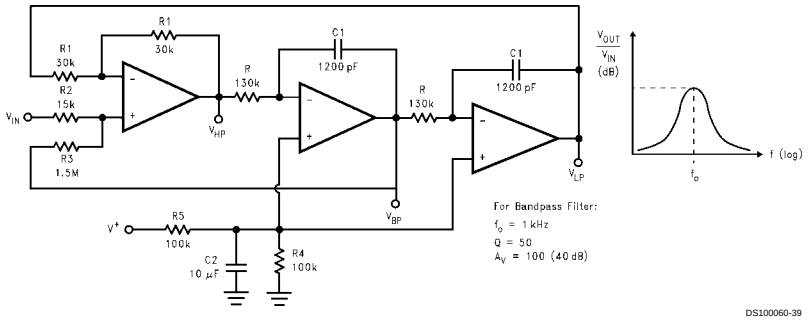
DS100060-83

FIGURE 14. Sallen-Key 2nd-Order Active High-Pass Filter

4.4.4 State Variable Filter

A state variable filter requires three op amps. One convenient way to build state variable filters is with a quad op amp, such as the LMV324 (*Figure 15*).

This circuit can simultaneously represent a low-pass filter, high-pass filter, and bandpass filter at three different outputs. The equations for these functions are listed below. It is also called "Bi-Quad" active filter as it can produce a transfer function which is quadratic in both numerator and denominator.



DS100060-39

FIGURE 15. State Variable Active Filter

Application Notes (Continued)

$$V_{LP} = \left(\frac{2R_3}{R_2 + R_3}\right) \frac{\frac{1}{R^2C^2}}{S^2 + \frac{1}{\left(\frac{R_2 + R_3}{2R_2}\right)RC} S + \frac{1}{R^2C^2}} V_{IN}$$

$$V_{HP} = \left(\frac{2R_3}{R_2 + R_3}\right) \frac{S^2}{S^2 + \frac{1}{\left(\frac{R_2 + R_3}{2R_2}\right)RC} S + \frac{1}{R^2C^2}} V_{IN}$$

$$V_{BP} = \left(\frac{2R_3}{R_2 + R_3}\right) \frac{\left(\frac{1}{RC}\right)S}{S^2 + \frac{1}{\left(\frac{R_2 + R_3}{2R_2}\right)RC} S + \frac{1}{R^2C^2}} V_{IN}$$

where for all three filters,

$$Q = \frac{R_2 + R_3}{2R_2} \quad (11)$$

$$\omega_0 = \frac{1}{RC} \quad \text{(resonant frequency)} \quad (12)$$

A design example for a bandpass filter is shown below:

Assume the system design requires a bandpass filter with f_O = 1 kHz and Q = 50. What needs to be calculated are capacitor and resistor values.

First choose convenient values for C_1, R_1 and R_2:

$$C_1 = 1200 \text{ pF}$$

$$2R2 = R_1 = 30 \text{ k}\Omega$$

Then from *Equation (11)*,

$$R_3 = R_2(2Q-1)$$

$$R_3 = 15 \text{ k}\Omega \times (2 \times 50 - 1)$$

$$= 1.5 \text{ M}\Omega$$

From *Equation (12)*,

$$R = \frac{1}{\omega_0 C_1}$$

$$R = \frac{1}{(2\pi \times 10^3)(1.2 \times 10^{-9})}$$

$$= 132.7 \text{ k}\Omega$$

From the above calculated values, the midband gain is $H_o = R_3/R_2 = 100$ (40dB). The nearest 5% standard values have been added to *Figure 15*.

4.5 Pulse Generators and Oscillators

A pulse generator is shown in *Figure 16*. Two diodes have been used to separate the charge and discharge paths to capacitor C.

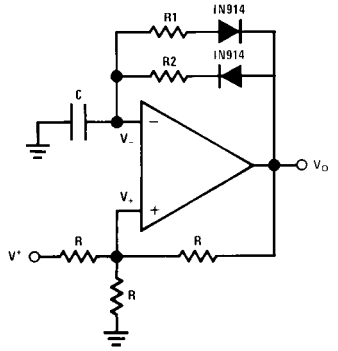


FIGURE 16. Pulse Generator

When the output voltage V_O is first at its high, V_{OH}, the capacitor C is charged toward V_{OH} through R_2. The voltage across C rises exponentially with a time constant $\tau = R_2C$, and this voltage is applied to the inverting input of the op amp. Meanwhile, the voltage at the non-inverting input is set at the positive threshold voltage (V_{TH+}) of the generator. The capacitor voltage continually increases until it reaches V_{TH+}, at which point the output of the generator will switch to its low, V_{OL} (=0V in this case). The voltage at the non-inverting input is switched to the negative threshold voltage (V_{TH-}) of the generator. The capacitor then starts to discharge toward V_{OL} exponentially through R_1, with a time constant $\tau = R_1C$. When the capacitor voltage reaches V_{TH-}, the output of the pulse generator switches to V_{OH}. The capacitor starts to charge, and the cycle repeats itself.

Application Notes (Continued)

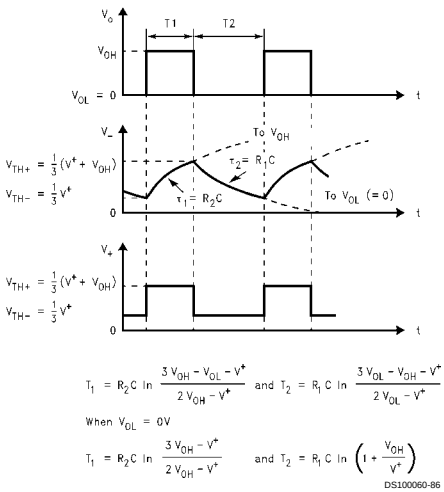


FIGURE 17. Waveforms of the Circuit in Figure 16

As shown in the waveforms in *Figure 17*, the pulse width (T_1) is set by R_2, C and V_{OH}, and the time between pulses (T_2) is set by R_1, C and V_{OL}. This pulse generator can be made to have different frequencies and pulse width by selecting different capacitor value and resistor values.

Figure 18 shows another pulse generator, with separate charge and discharge paths. The capacitor is charged through R1 and is discharged through R_2.

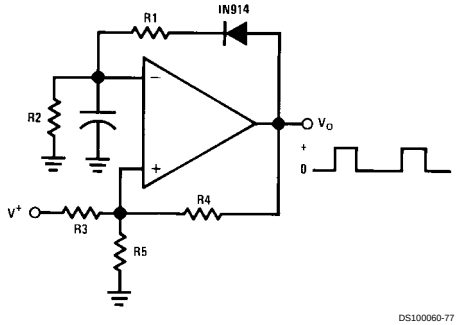


FIGURE 18. Pulse Generator

Figure 19 is a squarewave generator with the same path for charging and discharging the capacitor.

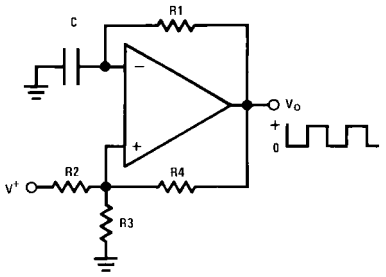


FIGURE 19. Squarewave Generator

4.6 Current Source and Sink

The LMV321/358/324 can be used in feedback loops which regulate the current in external PNP transistors to provide current sources or in external NPN transistors to provide current sinks.

4.6.1 Fixed Current Source

A multiple fixed current source is show in *Figure 20*. A voltage (V_{REF} = 2V) is established across resistor R_3 by the voltage divider (R_3 and R_4). Negative feedback is used to cause the voltage drop across R_1 to be equal to V_{REF}. This controls the emitter current of transistor Q_1 and if we neglect the base current of Q_1 and Q_2, essentially this same current is available out of the collector of Q_1.

Large input resistors can be used to reduce current loss and a Darlington connection can be used to reduce errors due to the β of Q_1.

The resistor, R_2, can be used to scale the collector current of Q_2 either above or below the 1 mA reference value.

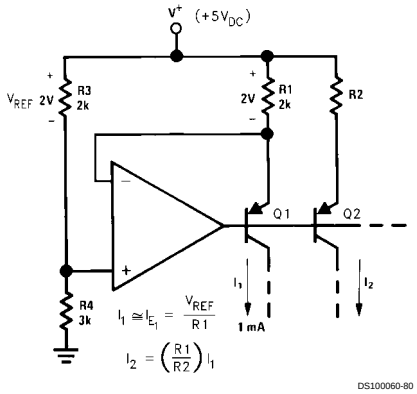


FIGURE 20. Fixed Current Source

Application Notes (Continued)

4.6.2 High Compliance Current Sink

A current sink circuit is shown in *Figure 21*. The circuit requires only one resistor (R_E) and supplies an output current which is directly proportional to this resistor value.

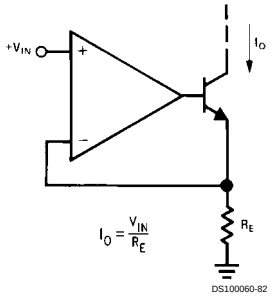


FIGURE 21. High Compliance Current Sink

4.7 Power Amplifier

A power amplifier is illustrated in *Figure 22*. This circuit can provide a higher output current because a transistor follower is added to the output of the op amp.

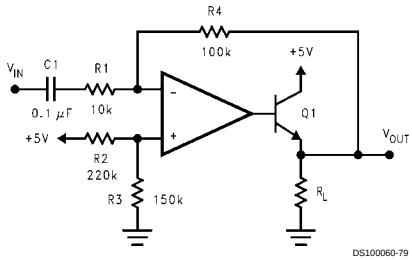


FIGURE 22. Power Amplifier

4.8 LED Driver

The LMV321/358/324 can be used to drive an LED as shown in *Figure 23*.

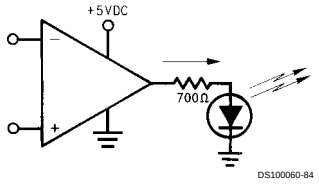


FIGURE 23. LED Driver

4.9 Comparator with Hysteresis

The LMV321/358/324 can be used as a low power comparator. *Figure 24* shows a comparator with hysteresis. The hysteresis is determined by the ratio of the two resistors.

$$V_{TH+} = V_{REF}/(1+R_1/R_2)+V_{OH}/(1+R_2/R_1)$$

$$V_{TH-} = V_{REF}/(1+R_1/R_2)+V_{OL}/(1+R_2/R_1)$$

$$V_H = (V_{OH}-V_{OL})/(1+R_2/R_1)$$

where

V_{TH+}: Positive Threshold Voltage

V_{TH-}: Negative Threshold Voltage

V_{OH}: Output Voltage at High

V_{OL}: Output Voltage at Low

V_H: Hysteresis Voltage

Since LMV321/358/324 have rail-to-rail output, the (V_{OH}–V_{OL}) equals to V_S, which is the supply voltage.

$$V_H = V_S/(1+R_2/R_1)$$

The differential voltage at the input of the op amp should not exceed the specified absolute maximum ratings. For real comparators that are much faster, we recommend you to use National's LMV331/393/339, which are single, dual and quad general purpose comparators for low voltage operation.

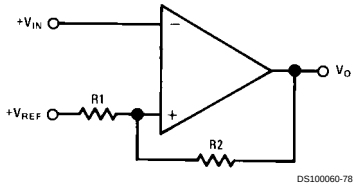
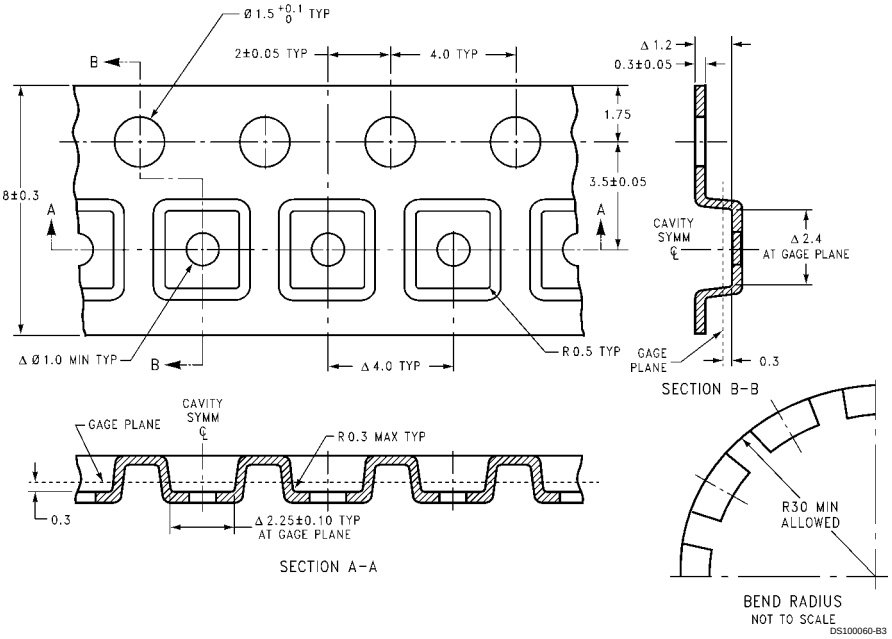


FIGURE 24. Comparator with Hysteresis

SC70-5 Tape and Reel Specification



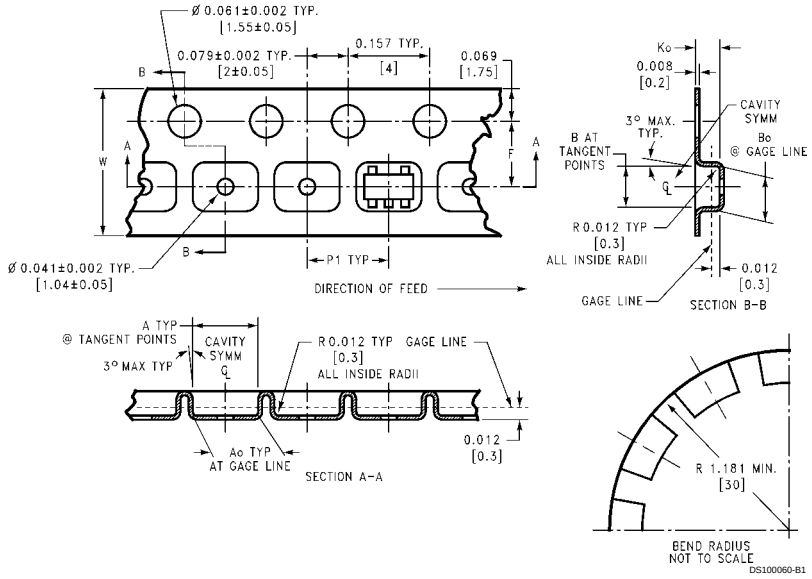
SOT-23-5 Tape and Reel Specification

TAPE FORMAT

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader	0 (min)	Empty	Sealed
(Start End)	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer	125 (min)	Empty	Sealed
(Hub End)	0 (min)	Empty	Sealed

SOT-23-5 Tape and Reel Specification (Continued)

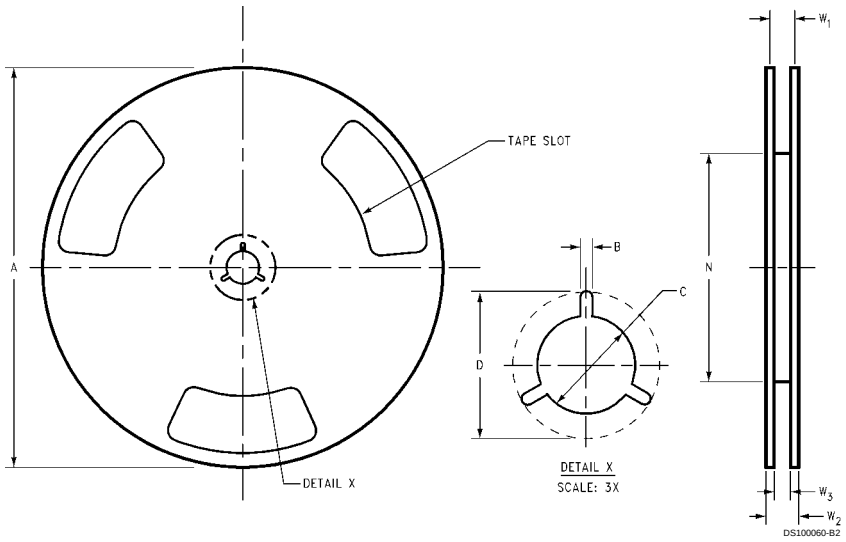
TAPE DIMENSIONS



8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ±0.002 (3.5 ±0.05)	0.055 ±0.004 (1.4 ±0.11)	0.157 (4)	0.315 ±0.012 (8 ±0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

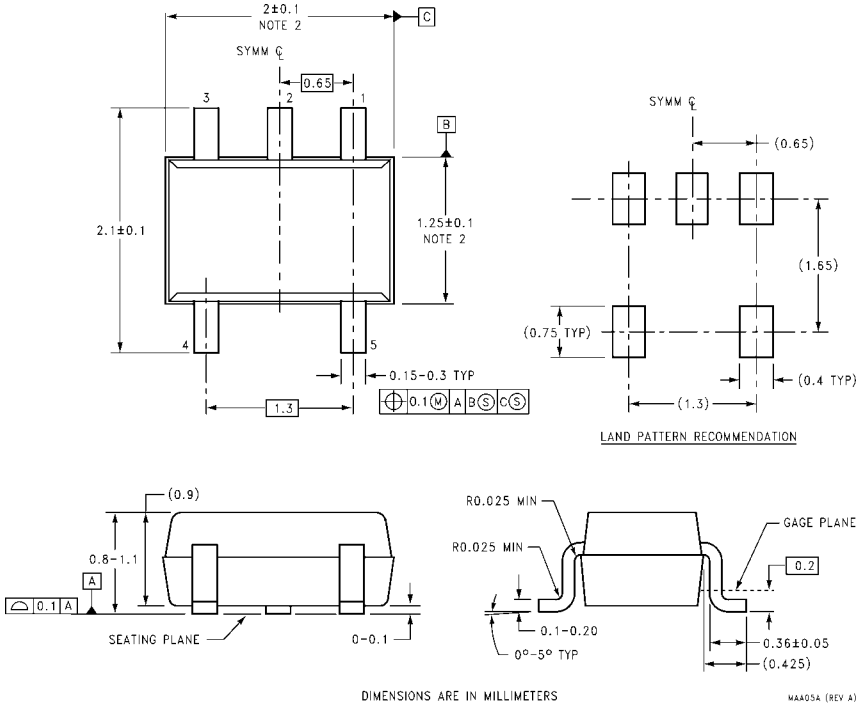
SOT-23-5 Tape and Reel Specification (Continued)

REEL DIMENSIONS



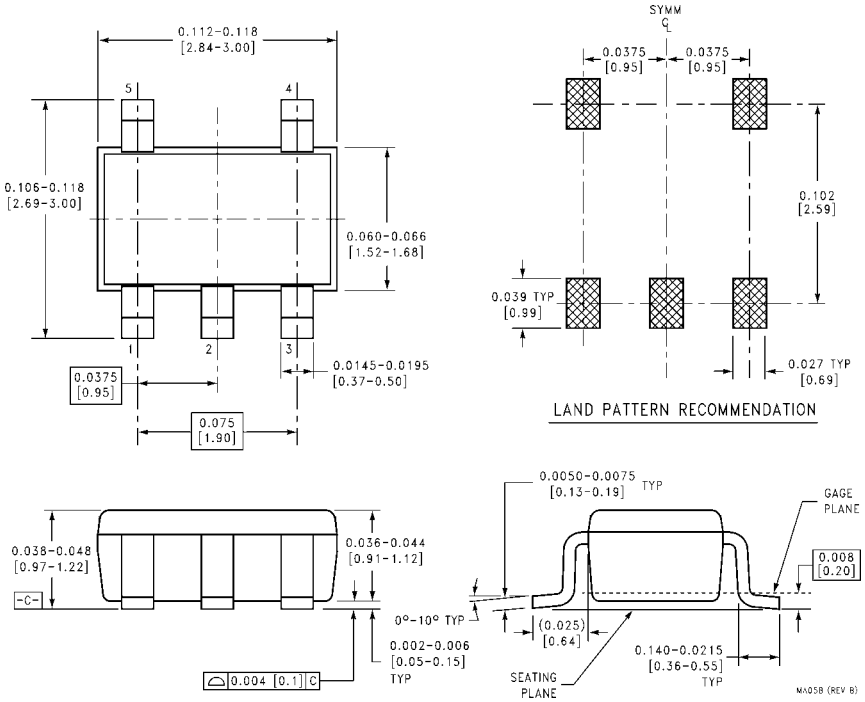
8 mm	7.00 330.00	0.059 1.50	0.512 13.00	0.795 20.20	2.165 55.00	0.331 + 0.059/−0.000 8.40 + 1.50/−0.00	0.567 14.40	W1+ 0.078/−0.039 W1 + 2.00/−1.00
Tape Size	A	B	C	D	N	W1	W2	W3

Physical Dimensions inches (millimeters) unless otherwise noted



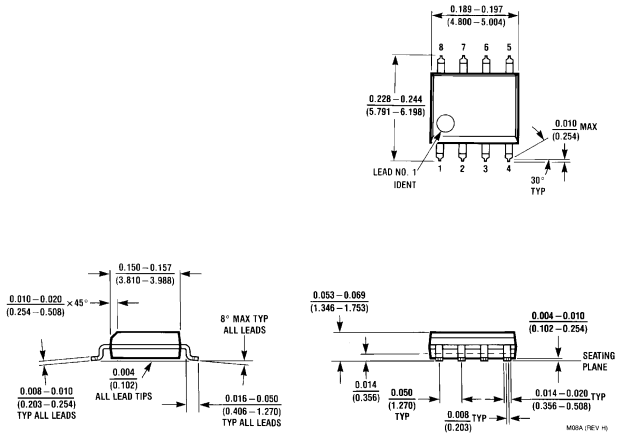
5-Pin SC70-5 Tape and Reel
Order Number LMV321M7 and LMV321M7X
NS Package Number MAA05A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



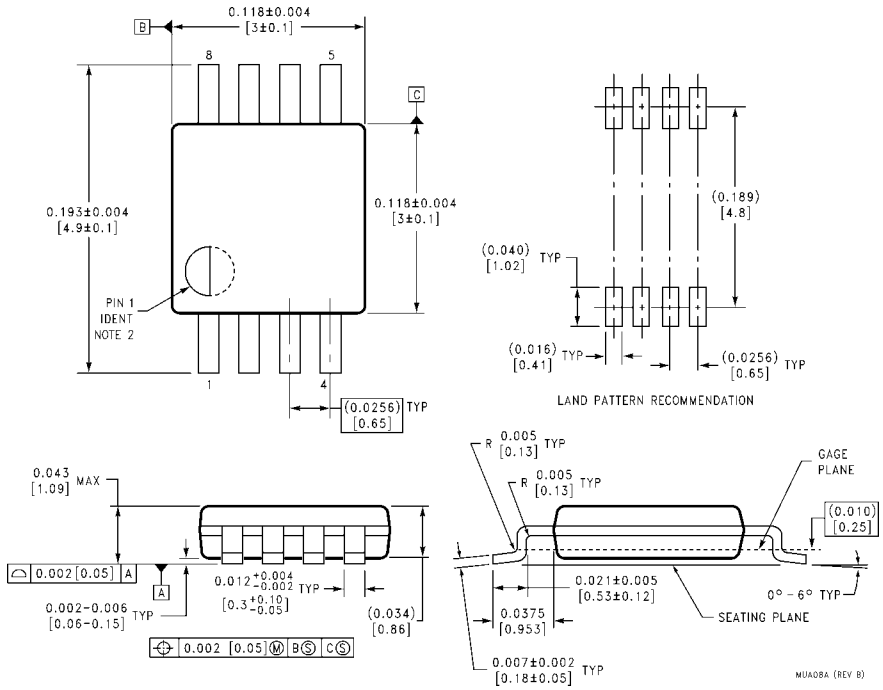
5-Pin SOT23-5 Tape and Reel
Order Number LMV321M5 and LMV321M5X
NS Package Number MA05B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



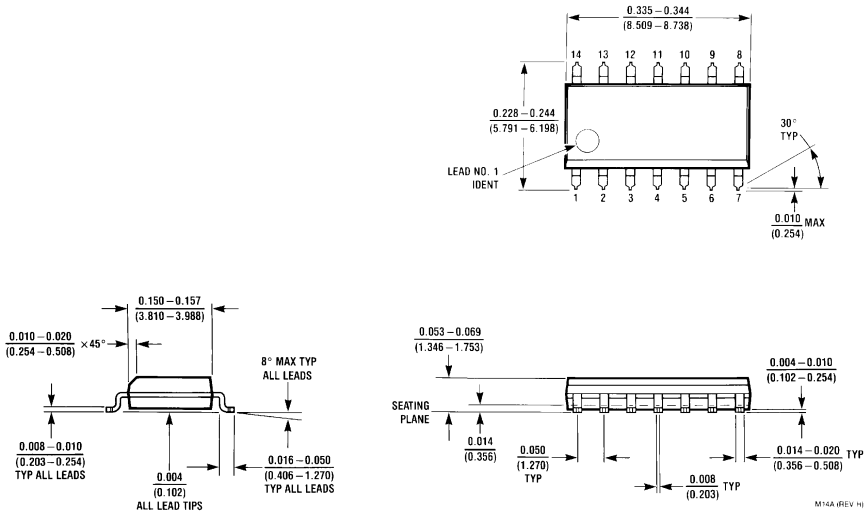
8-Pin Small Outline
Order Number LMV358M and LMV358MX
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



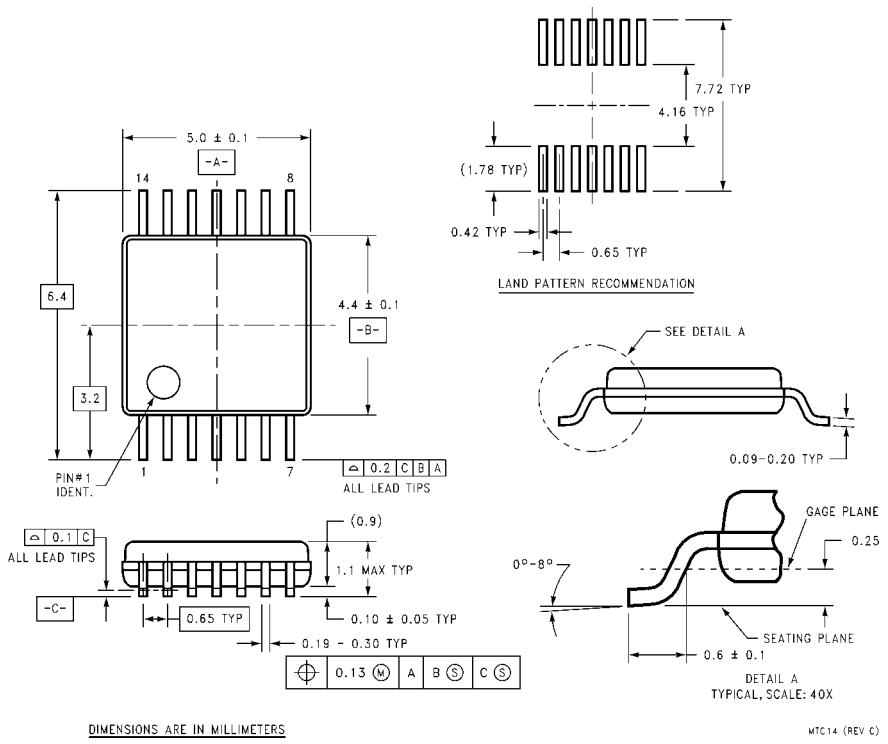
8-Pin MSOP
Order Number LMV358MM and LMV358MMX
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin Small Outline
Order Number LMV324M and LMV324MX
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin TSSOP
Order Number LMV324MT and LMV324MTX
NS Package Number MTC14

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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2.1.2 LMV331/393/339 Datasheet

National Semiconductor

February 1998

LMV331 Single / LMV393 Dual / LMV339 Quad General Purpose, Low Voltage, TinyPack Comparators

General Description

The LMV393 and LMV339 are low voltage (2.7-5V) versions of the dual and quad comparators, LM393/339, which are specified at 5-30V. The LMV331 is the single version, which is available in space saving SC70-5 and SOT23-5 packages. SC70-5 is approximately half the size of SOT23-5.

The LMV393 is available in 8-pin SOIC and 8-pin MSOP. The LMV339 is available in 14-pin SOIC and 14-pin TSSOP.

The LMV331/393/339 is the most cost-effective solution where space, low voltage, low power and price are the primary specification in circuit design for portable consumer products. They offer specifications that meet or exceed the familiar LM393/339 at a fraction of the supply current.

The chips are built with National's advanced Submicron Silicon-Gate BiCMOS process. The LMV331/393/339 have bipolar input and output stages for improved noise performance.

Features

(For 5V Supply, Typical Unless Otherwise Noted)

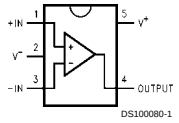
- Space Saving Package Space SC70-5 (2.0 x 2.1 x 1.0 mm)
- Space Saving Package Space SOT23-5 (3.00 x 3.01 x 1.43 mm)
- Guaranteed 2.7V and 5V Performance
- Industrial Temperature Range −40˚C to +85˚C
- Low Supply Current 60µA/Channel
- Input Common Mode Voltage Range Includes Ground
- Low Output Saturation Voltage 200 mV

Applications

- Mobile Communications
- Notebooks and PDA's
- Battery Powered Electronics
- General Purpose Portable Device
- General Purpose Low Voltage Applications

Connection Diagrams

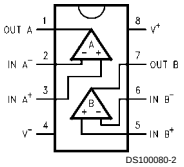
5-Pin SC70-5/SOT23-5



DS100080-1

Top View

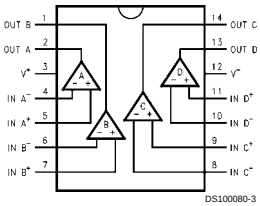
8-Pin SO/MSOP



DS100080-2

Top View

14-Pin SO/TSSOP



DS100080-3

Top View

2.0 DEVICE INFORMATION

Ordering Information

Package	Temperature Range	Packaging Marking	Transport Media	NSC Drawing
	Industrial −40˚C to +85˚C			
5-pin SC70-5	LMV331M7	C13	250 Units Tape and Reel	MAA05
	LMV331M7X	C13	3k Units Tape and Reel	
5-pin SOT23-5	LMV331M5	C12	250 Units Tape and Reel	MA05B
	LMV331M5X	C12	3k Units Tape and Reel	
8-pin Small Outline	LMV393M	LMV393M	Rails	M08A
	LMV393MX	LMV393M	2.5k Units Tape and Reel	
8-pin MSOP	LMV393MM	V393	250 UnitsTape and Reel	MUA08A
	LMV393MMX	V393	3.5k Units Tape and Reel	
14-pin Small Outline	LMV339M	LMV339M	Rails	M14A
	LMV339MX	LMV339M	2.5k Units Tape and Reel	
14-pin TSSOP	LMV339MT	LMV339MT	Rails	MTC14
	LMV339MTX	LMV339MT	2.5k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	
LMV331/ 393/ 339	800V
Machine Model LMV331/339/393	120V
Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	5.5V
Mounting Temperature	
Lead Temp. (soldering, 10 sec)	260˚C
Infrared (15 sec)	215˚C
Storage Temp. Range	−65˚C to +150˚C
Junction Temperature (Note 3)	150˚C

Operating Ratings (Note 1)

Supply Voltage	2.7V to 5.5V
Temperature Range	
LMV393, LMV339, LMV331	$-40^\circ C \le T_J \le +85^\circ C$
Thermal Resistance (θ_{JA})	
M Package, 8-pin Surface Mount	190˚C/W
M Package, 14-pin Surface Mount	145˚C/W
MTC Package, 14-pin TSSOP	155˚C/W
MAA05 Package, 5-pin SC70-5	478˚C/W
M05A Package 5 -pin SOT23-5	265˚C/W
MM Package, 8-pin Mini Surface Mount	235˚C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V+ = 2.7V, V− = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 4)	LMV331/ 393/339 Limit (Note 5)	Units
V_{OS}	Input Offset Voltage		1.7	7	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**5**		µV/˚C
I_B	Input Bias Current		10	250 **400**	nA max
I_{OS}	Input Offset Current		5	50 **150**	nA max
V_{CM}	Input Voltage Range		−0.1		V
			2.0		V
V_{SAT}	Saturation Voltage	$I_{sink} \le 1mA$	200		mV
I_O	Output Sink Current	$V_O \le 1.5V$	23	5	mA min
I_S	Supply Current	LMV331	40	100	µA max
		LMV393 Both Comparators	70	140	µA max
		LMV339 All four Comparators	140	200	µA max
	Output Leakage Current		.003	**1**	µA max

2.7V AC Electrical Characteristics

T_J = 25˚C, V+ = 2.7V, R_L = 5.1 kΩ, V− = 0V.

Symbol	Parameter	Conditions	Typ (Note 4)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive =10 mV	1000	ns
		Input Overdrive =100 mV	350	
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive =10 mV	500	ns
		Input Overdrive =100 mV	400	

2.0 DEVICE INFORMATION

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V+ = 5V, V− = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 4)	LMV331/ 393/339 Limit (Note 5)	Units
V_{OS}	Input Offset Voltage		1.7	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		5		µV/˚C
I_B	Input Bias Current		25	250 **400**	nA max
I_{OS}	Input Offset Current		2	50 **150**	nA max
V_{CM}	Input Voltage Range		−0.1		V
			4.2		V
A_V	Voltage Gain		50	20	V/mV min
V_{sat}	Saturation Voltage	$I_{sink} \leq 4$ mA	200	400 **700**	mV max
I_O	Output Sink Current	$V_O \leq 1.5V$	84	10	mA
I_S	Supply Current	LMV331	60	120 **150**	µA max
		LMV393 Both Comparators	100	200 **250**	µA max
		LMV339 All four Comparators	170	300 **350**	µA max
	Output Leakage Current		.003	**1**	µA max

5V AC Electrical Characteristics

T_J = 25˚C, V+ = 5V, R_L = 5.1 kΩ, V− = 0V.

Symbol	Parameter	Conditions	Typ (Note 4)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive =10 mV	600	ns
		Input Overdrive =100 mV	200	
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive =10 mV	450	ns
		Input Overdrive =100 mV	300	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.

Note 2: : Human body model, 1.5kΩ in series with 100 pF. Machine model, 200Ω in series with 100 pF.

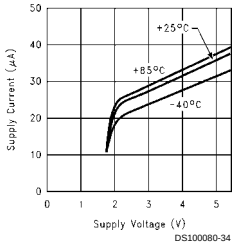
Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 4: Typical Values represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

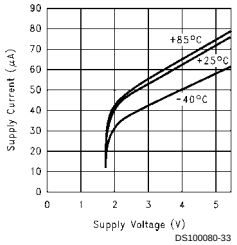
Typical Performance Characteristics Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C

Supply Current vs Supply Voltage Output High (LMV331)



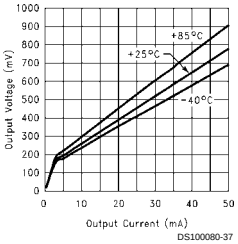
DS100080-34

Supply Current vs Supply Voltage Output Low (LMV331)



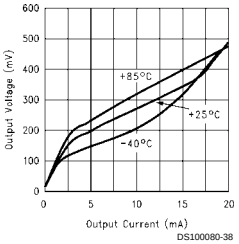
DS100080-33

Output Voltage vs Output Current at 5V Supply



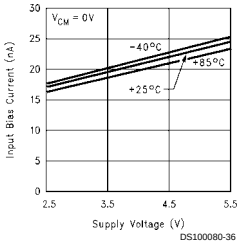
DS100080-37

Output Voltage vs Output Current at 2.7 Supply



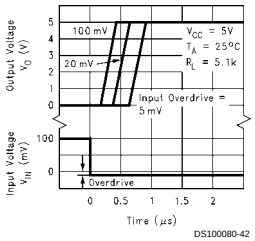
DS100080-38

Input Bias Current vs Supply Voltage



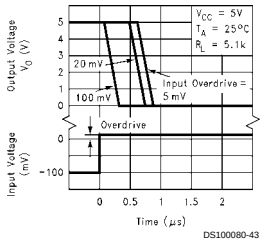
DS100080-36

Response Time vs Input Overdrives Negative Transition



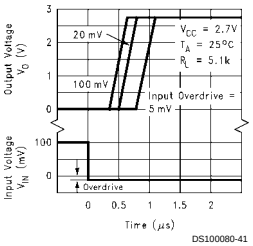
DS100080-42

Response Time for Input Overdrive Positive Transition



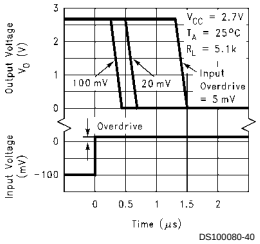
DS100080-43

Response Time vs Input Overdrives Negative Transition



DS100080-41

Response Time for Input Overdrive Positive Transition



DS100080-40

Application Circuits

Basic Comparator

A basic comparator circuit is used for converting analog signals to a digital output. The LMV331/393/339 have an open-collector output stage, which requires a pull-up resistor to a positive supply voltage for the output to switch properly. When the internal output transistor is off, the output voltage will be pulled up to the external positive voltage.

The output pull-up resistor should be chosen high enough so as to avoid excessive power dissipation yet low enough to supply enough drive to switch whatever load circuitry is used on the comparator output. On the LMV331/393/339 the pull-up resistor should range between 1k to 10kΩ.

The comparator compares the input voltage (V_{in}) at the non-inverting pin to the reference voltage (V_{ref}) at the inverting pin. If V_{in} is less than V_{ref}, the output voltage (V_o) is at the saturation voltage. On the other hand, if V_{in} is greater than V_{ref}, the output voltage (V_o) is at V_{cc}.

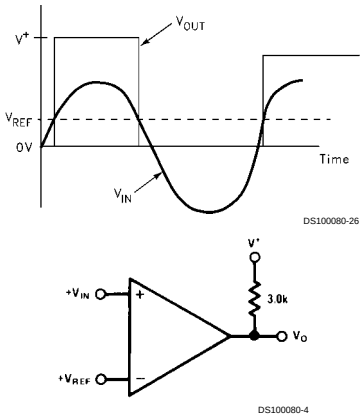


FIGURE 1. Basic Comparator

Comparator with Hysteresis

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the comparator's switching threshold. This problem can be prevented by the addition of hysteresis or positive feedback.

Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three resistor network that are referenced to the supply voltage V_{cc} of the comparator. When Vin at the inverting input is less than V_a, the voltage at the non-inverting node of the comparator ($V_{in} < V_a$), the output voltage is high (for simplicity assume V_o switches as high as V_{cc}). The three network resistors can be represented as $R_1//R_3$ in series with R_2. The lower input trip voltage V_{a1} is defined as

$$V_{a_1} = \frac{V_{CC}\ R_2}{(R_1 \,||\, R_3) + R_2}$$

When V_{in} is greater than Va (V_{in} V_a), the output voltage is low very close to ground. In this case the three network resistors can be presented as $R_2//R_3$ in series with R_1. The upper trip voltage V_{a2} is defined as

$$V_{a2} = \frac{V_{CC}(R_2 // R_3)}{R_1 + (R_2 // R_3)}$$

The total hysteresis provided by the network is defined as

$$\Delta V_a = V_{a1} - V_{a2}$$

To assure that the comparator will always switch fully to V_{cc} and not be pulled down by the load the resistors values should be chosen as follow:

$$R_{pull\text{-}up} << R_{load}$$

and $R_1 > R_{pull\text{-}up}$.

Application Circuits (Continued)

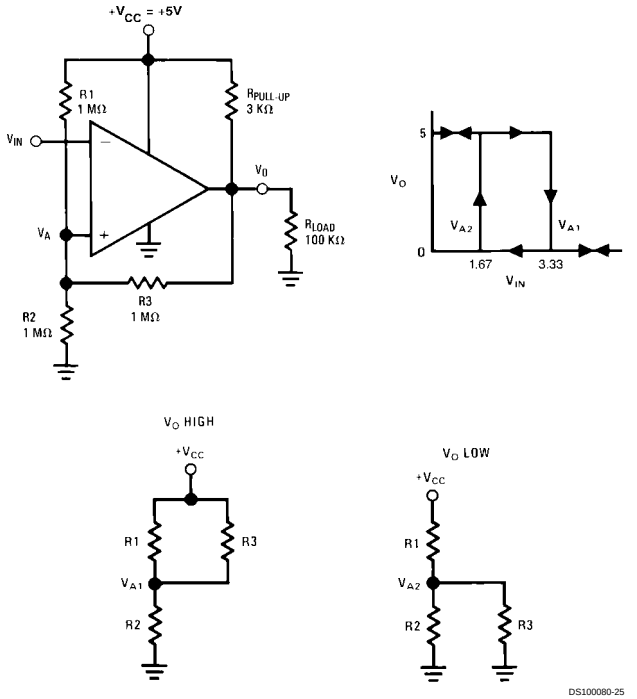


FIGURE 2. Inverting Comparator with Hysteresis

Non-Inverting Comparator with Hysteresis

Non inverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{ref}) at the inverting input. When V_{in} is low, the output is also low. For the output to switch from low to high, V_{in} must rise up to V_{in1} where V_{in1} is calculated by

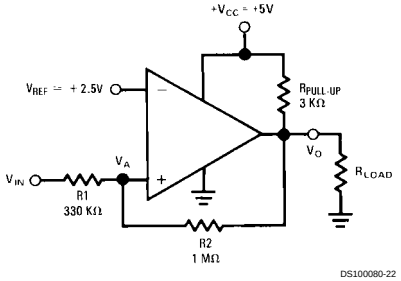
$$V_{in1} = \frac{V_{ref}(R_1 + R_2)}{R_2}$$

When V_{in} is high, the output is also high, to make the comparator switch back to it's low state, V_{in} must equal V_{ref} before V_a will again equal V_{ref}. V_{in} can be calculated by:

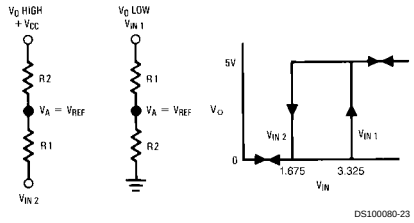
$$V_{in2} = \frac{V_{ref}(R_1 + R_2) - V_{CC}R_1}{R_2}$$

The hysteresis of this circuit is the difference between V_{in1} and V_{in2}.

$$\Delta V_{in} = V_{cc}R_1/R_2$$



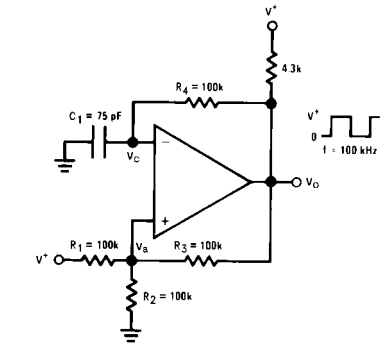
Application Circuits (Continued)



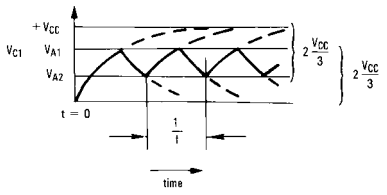
DS100080-23

Square Wave Oscillator

Comparators are ideal for oscillator applications. This square wave generator uses the minimum number of components. The output frequency is set by the RC time constant of the capacitor C_1 and the resistor in the negative feedback R_4. The maximum frequency is limited only by the large signal propagation delay of the comparator in addition to any capacitive loading at the output, which would degrade the output slew rate.



DS100080-8



DS100080-24

FIGURE 5. Squarewave Oscillator

To analyze the circuit, assume that the output is initially high. For this to be true, the voltage at the inverting input V_c has to be less than the voltage at the non-inverting input V_a. For V_c to be low, the capacitor C_1 has to be discharged and will charge up through the negative feedback resistor R_4. When it has charged up to value equal to the voltage at the positive input V_{a1}, the comparator output will switch.

V_{a1} will be given by:

$$V_{a1} = \frac{V_{CC}\, R_2}{R_2 + (R_1 \,//\, R_2)}$$

If:

$$R_1 = R_2 = R_3$$

Then:

$$V_{a1} = 2V_{cc}/3$$

When the output switches to ground, the value of V_a is reduced by the hysteresis network to a value given by:

$$V_{a2} = V_{cc}/3$$

Capacitor C_1 must now discharge through R_4 towards ground. The output will return to its high state when the voltage across the capacitor has discharged to a value equal to V_{a2}.

For the circuit shown, the period for one cycle of oscillation will be twice the time it takes for a single RC circuit to charge up to one half of its final value. The time to charge the capacitor can be calculated from

$$V_C = V_{max}\, e^{\frac{-t}{RC}}$$

Where V_{max} is the max applied potential across the capacitor = $(2V_{cc}/3)$

and V_C = Vmax/2 = $V_{CC}/3$

One period will be given by:

$$1/\text{freq} = 2t$$

or calculating the exponential gives:

$$1/\text{freq} = 2(0.694)\, R_4\, C_1$$

Resistors R_3 and R_4 must be at least two times larger than R_5 to insure that V_o will go all the way up to V_{cc} in the high state. The frequency stability of this circuit should strictly be a function of the external components.

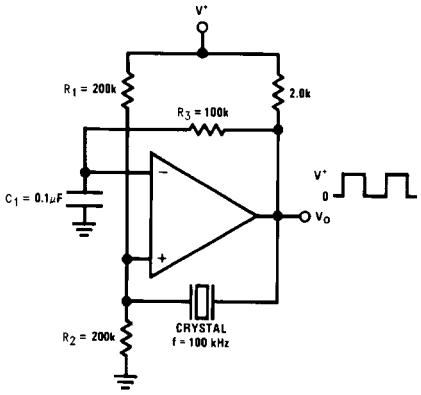
Free Running Multivibrator

A simple yet very stable oscillator that generates a clock for slower digital systems can be obtained by using a resonator as the feedback element. It is similar to the free running multivibrator, except that the positive feedback is obtained through a quartz crystal. The circuit oscillates when the transmission through the crystal is at a maximum, so the crystal in its series-resonant mode.

The value of R_1 and R_2 are equal so that the comparator will switch symmetrically about $+V_{cc}/2$. The RC constant of R_3 and C_1 is set to be several times greater than the period of the oscillating frequency, insuring a 50% duty cycle by maintaining a DC voltage at the inverting input equal to the absolute average of the output waveform.

Application Circuits (Continued)

When specifying the crystal, be sure to order series resonant with the desired temperature coefficient



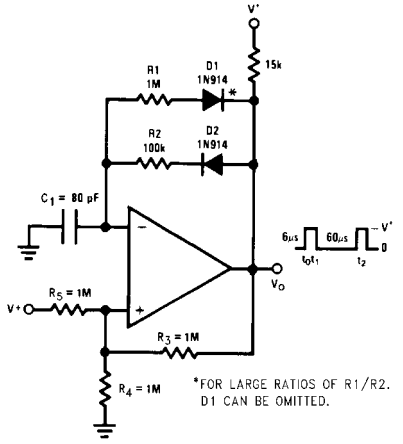
DS100080-7

FIGURE 6. Crystal controlled Oscillator

Pulse generator with variable duty cycle:

The pulse generator with variable duty cycle is just a minor modification of the basic square wave generator. Providing a separate charge and discharge path for capacitor C_1 generates a variable duty cycle. One path, through R_2 and D_2 will charge the capacitor and set the pulse width (t_1). The other path, R_1 and D_1 will discharge the capacitor and set the time between pulses (t_2).

By varying resistor R_1, the time between pulses of the generator can be changed without changing the pulse width. Similarly, by varying R_2, the pulse width will be altered without affecting the time between pulses. Both controls will change the frequency of the generator. The pulse width and time between pulses can be found from:



DS100080-9

FIGURE 7. Pulse Generator

$$V_1 = V_{max}\left(1 - e^{-t_1/R_4C_1}\right) \quad \text{rise time}$$

$$V_1 = V_{max}\, e^{-t_2/R_5C_1} \quad \text{fall time}$$

Where

$$V_{max} = \frac{2\,V_{CC}}{3}$$

and

$$V_1 = \frac{V_{max}}{3} = \frac{V_{CC}}{3}$$

Which gives

$$\frac{1}{2} = e^{-t_1/R_4C_1}$$

t_2 is then given by:

$$\frac{1}{2} = e^{-t_2/R_5C_1}$$

Solving these equations for t_1 and t_2

$$t_1 = R_4C_1\ln 2$$

$$t_2 = R_5C_1\ln 2$$

These terms will have a slight error due to the fact that V_{max} is not exactly equal to 2/3 V_{CC} but is actually reduced by the diode drop to:

$$V_{max} = \frac{2}{3}\left(V_{CC} - V_{BE}\right)$$

$$\frac{1}{2(1 - V_{BE})} = e^{-t_1/R_4C_1}$$

$$\frac{1}{2(1 - V_{BE})} = e^{-t_2/R_5C_1}$$

Application Circuits (Continued)

Positive Peak Detector:

Positive peak detector is basically the comparator operated as a unit gain follower with a large holding capacitor from the output to ground. Additional transistor is added to the output to provide a low impedance current source. When the output of the comparator goes high, current is passed through the transistor to charge up the capacitor. The only discharge path will be the 1M ohm resistor shunting C1 and any load that is connected to the output. The decay time can be altered simply by changing the 1M ohm resistor. The output should be used through a high impedance follower to a avoid loading the output of the peak detector.

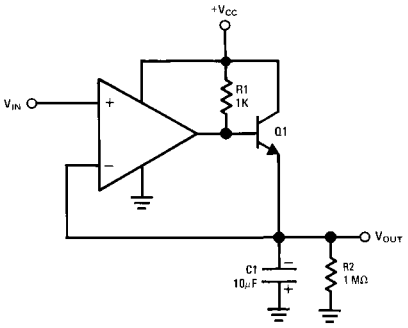


FIGURE 8. Positive Peak Detector

Negative Peak Detector:

For the negative detector, the output transistor of the comparator acts as a low impedance current sink. The only discharge path will be the 1 MΩ resistor and any load impedance used. Decay time is changed by varying the 1 MΩ resistor

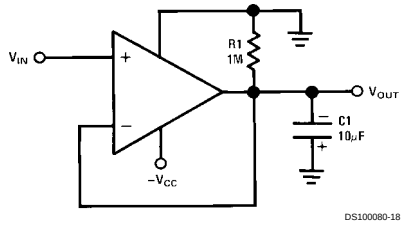


FIGURE 9. Negative Peak Detector

Driving CMOS and TTL

The comparator's output is capable of driving CMOS and TTL Logic circuits.

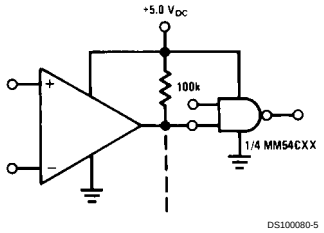


FIGURE 10. Driving CMOS

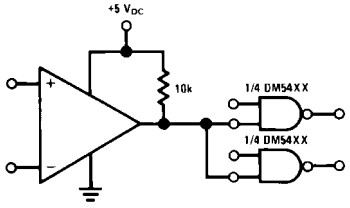


FIGURE 11. Driving TTL

AND Gates

The comparator can be used as three input AND gate. The operation of the gate is as follow:

The resistor divider at the inverting input establishes a reference voltage at that node. The non-inverting input is the sum of the voltages at the inputs divided by the voltage dividers. The output will go high only when all three inputs are high, casing the voltage at the non-inverting input to go above that at inverting input. The circuit values shown work for a ″0″ equal to ground and a ″1″ equal to 5V.

The resistor values can be altered if different logic levels are desired. If more inputs are required, diodes are recommended to improve the voltage margin when all but one of the inputs are high.

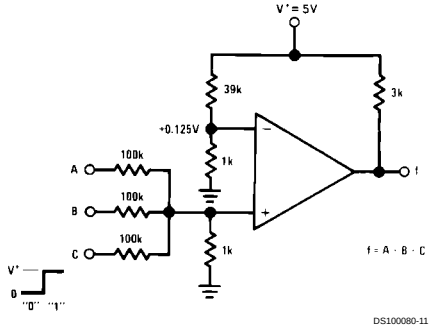


FIGURE 12. AND Gate

Application Circuits (Continued)

OR Gates

A three input OR gate is achieved from the basic AND gate simply by increasing the resistor value connected from the inverting input to V_{cc}, thereby reducing the reference voltage.

A logic "1" at any of the inputs will produce a logic "1" at the output.

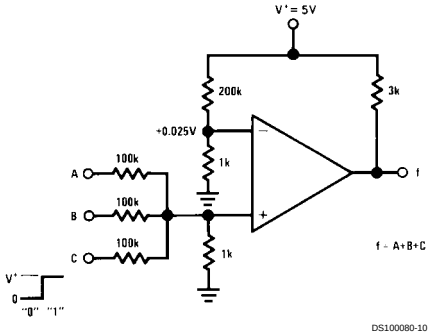


FIGURE 13. OR Gate

ORing the Output

By the inherit nature of an open collector comparator, the outputs of several comparators can be tied together with a pull up resistor to V_{cc}. If one or more of the comparators outputs goes low, the output V_o will go low.

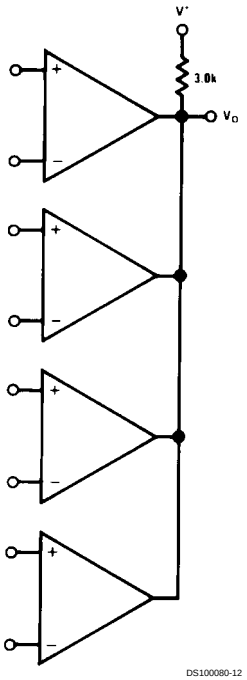


FIGURE 14. ORing the Outputs

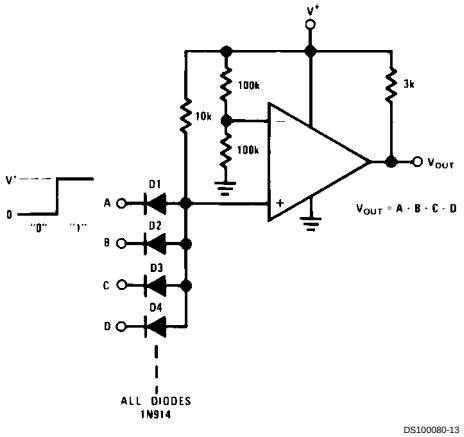
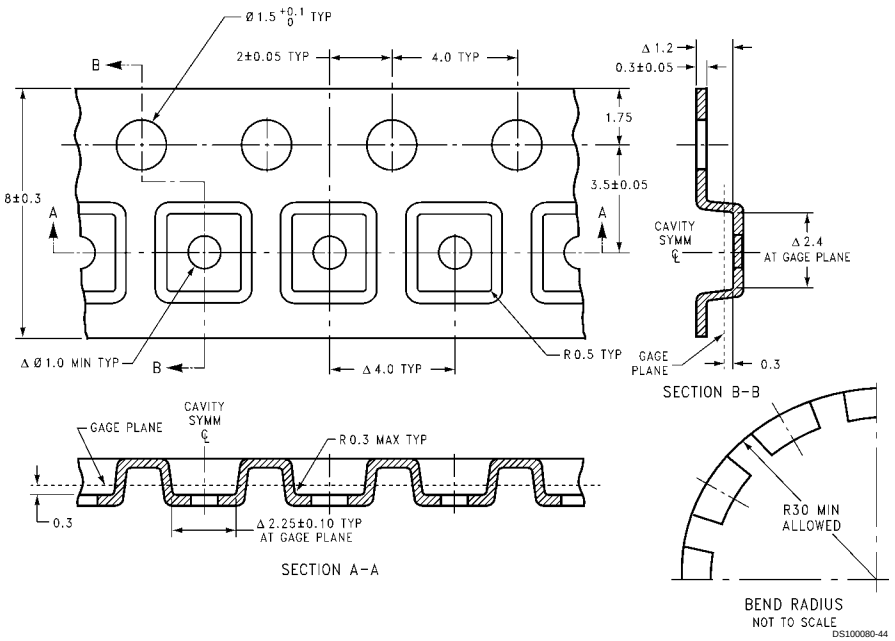


FIGURE 15. Large Fan-In AND Gate

SC70-5 Tape and Reel Specification



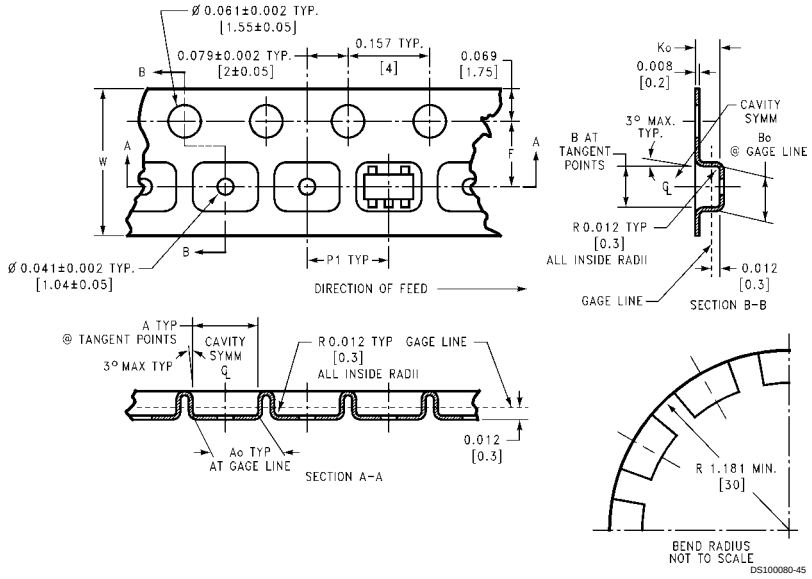
SOT-23-5 Tape and Reel Specification

TAPE FORMAT

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader	0 (min)	Empty	Sealed
(Start End)	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer	125 (min)	Empty	Sealed
(Hub End)	0 (min)	Empty	Sealed

SOT-23-5 Tape and Reel Specification (Continued)

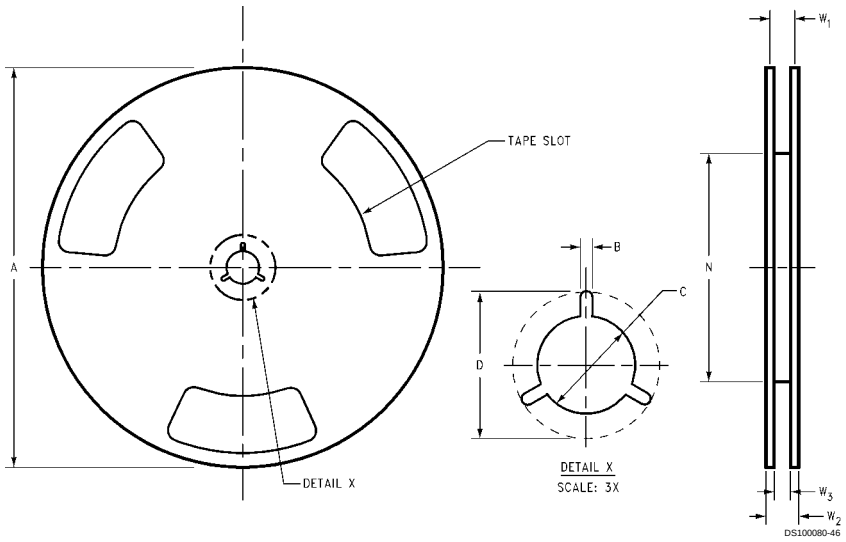
TAPE DIMENSIONS



8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ±0.002 (3.5 ±0.05)	0.055 ±0.004 (1.4 ±0.11)	0.157 (4)	0.315 ±0.012 (8 ±0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

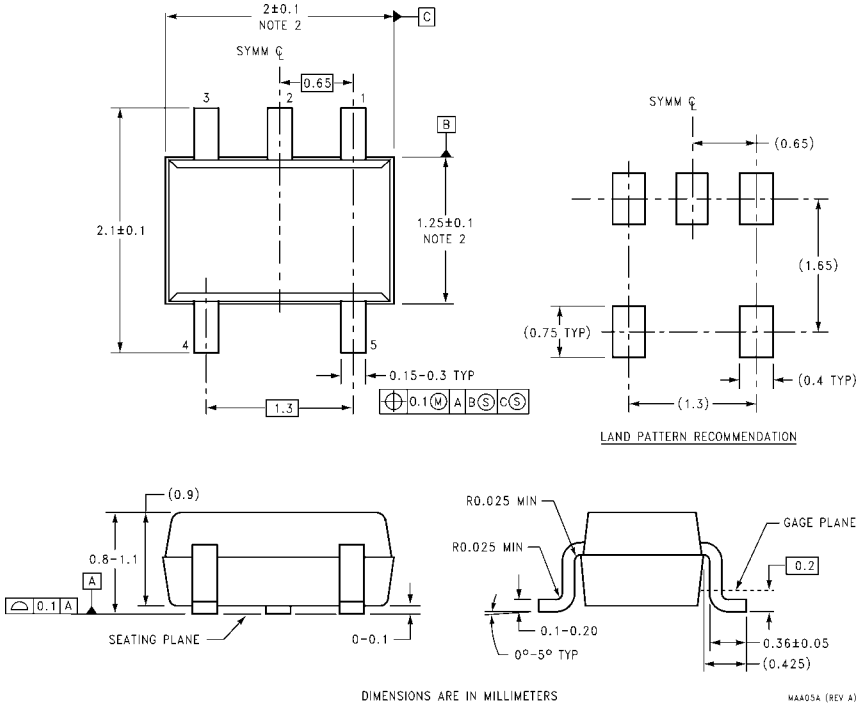
SOT-23-5 Tape and Reel Specification (Continued)

REEL DIMENSIONS



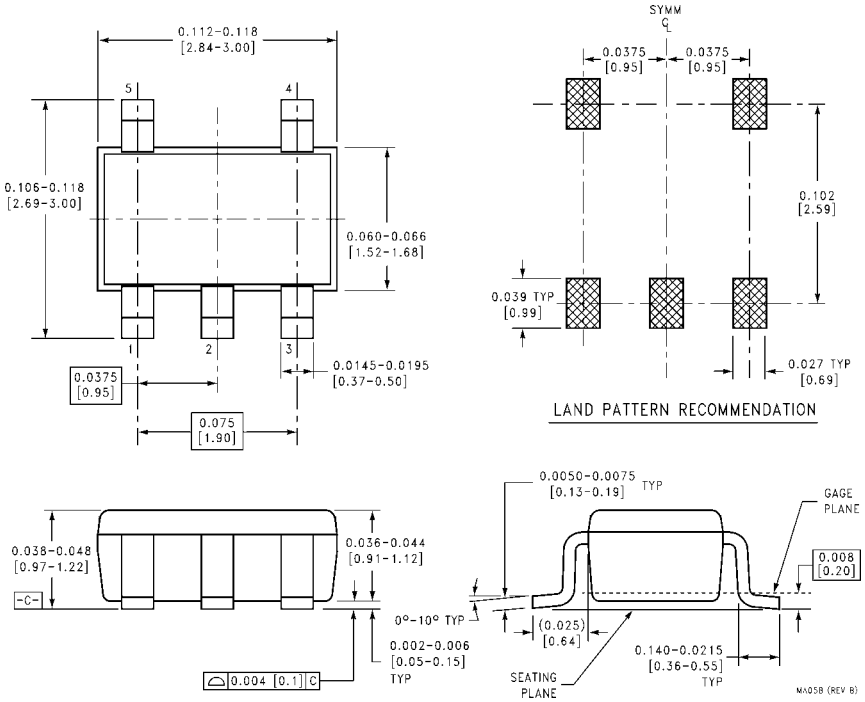
8 mm	7.00 330.00	0.059 1.50	0.512 13.00	0.795 20.20	2.165 55.00	0.331 + 0.059/−0.000 8.40 + 1.50/−0.00	0.567 14.40	W1+ 0.078/−0.039 W1 + 2.00/−1.00
Tape Size	A	B	C	D	N	W1	W2	W3

Physical Dimensions inches (millimeters) unless otherwise noted



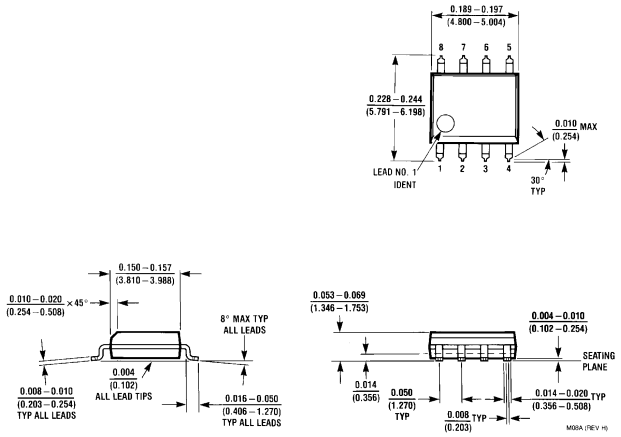
5-Pin SC70-5 Tape and Reel
Order Number LMV331M7 and LMV331M7X
NS Package Number MAA05A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



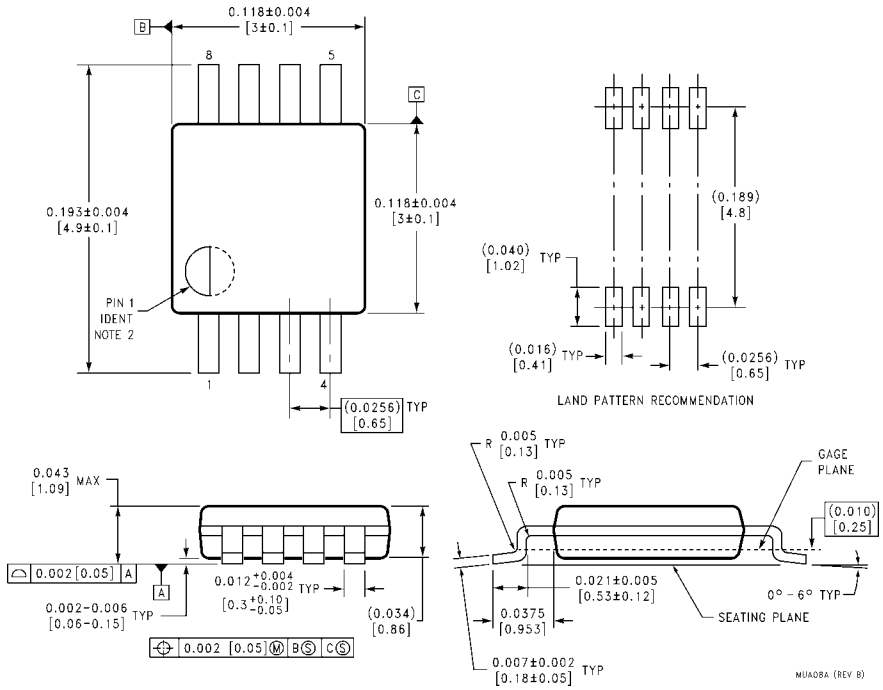
5-Pin SOT23-5 Tape and Reel
Order Number LMV331M5 and LMV331M5X
NS Package Number MA05B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



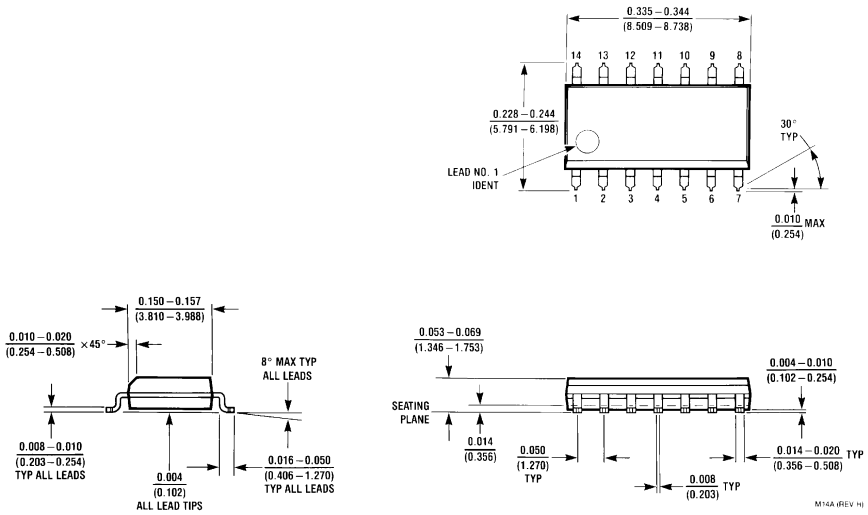
8-Pin Small Outline
Order Number LMV393M and LMV393MX
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



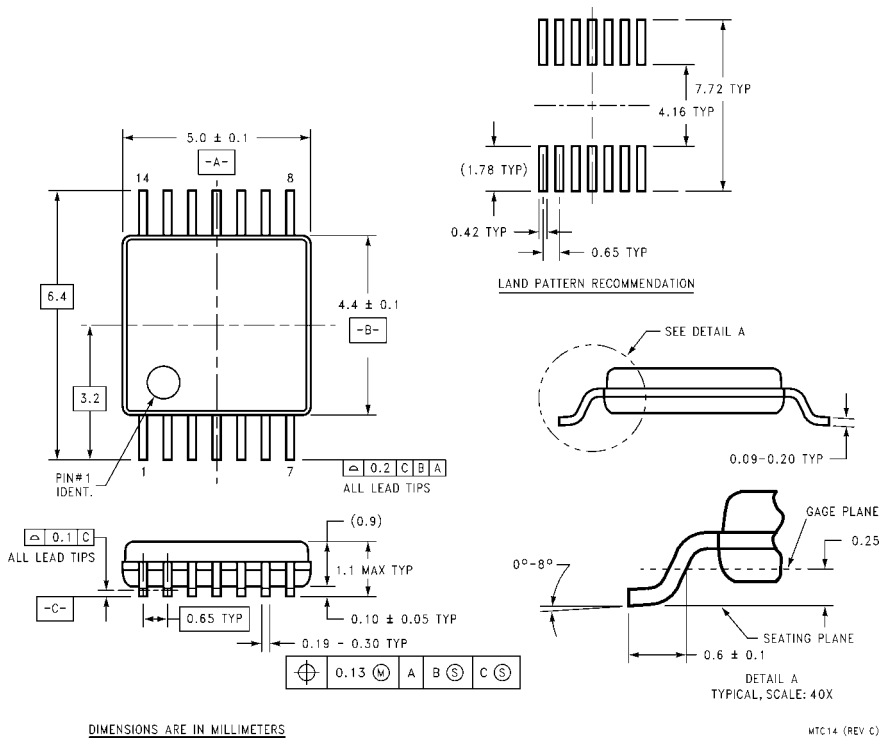
8-Pin MSOP
Order Number LMV393MM and LMV393MMX
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin Small Outline
Order Number LMV339M and LMV339MX
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin TSSOP
Order Number LMV339MT and LMV339MTX
NS Package Number MTC14

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2.1.3 LMV821/822/824 Datasheet

National Semiconductor

March 1998

LMV821 Single/ LMV822 Dual/ LMV824 Quad Low Voltage, Low Power, R-to-R Output, 5 MHz Op Amps

General Description

The LMV821/LMV822/LMV824 bring performance and economy to low voltage / low power systems. With a 5 MHz unity-gain frequency and a guaranteed 1.5 V/µs slew rate, the quiescent current is only 215 µA/amplifier (2.7 V). They provide rail-to-rail (R-to-R) output swing into heavy loads (600 Ω Guarantees). The input common-mode voltage range includes ground, and the maximum input offset voltage is 3mV (25°C, Guaranteed). They are also capable of comfortably driving large capacitive loads (refer to the application notes section).

The LMV821 (single) is available in the ultra tiny SC70-5 package, which is about half the size of the previous title holder, the SOT23-5.

Overall, the LMV821/LMV822/LMV824 (Single/Dual/Quad) are low voltage, low power, performance op amps, that can be designed into a wide range of applications, at an economical price.

Features

(For Typical, 5 V Supply Values; Unless Otherwise Noted)

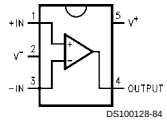
- Ultra Tiny, SC70-5 Package 2.0 x 2.0 x 1.0 mm
- Guaranteed 2.5 V, 2.7 V and 5 V Performance
- Maximum VOS 3 mV (Guaranteed)
- VOS Temp. Drift 1 uV/° C
- GBW product @ 2.7 V 5 MHz
- I_{Supply} @ 2.7 V 215 µA/Amplifier
- Minimum SR 1.5 V/us (Guaranteed)
- CMRR 90 dB
- PSRR 85 dB
- Rail-to-Rail (R-to-R) Output Swing
  - — @600 Ω Load 160 mV from rail
  - — @10 kΩ Load 55 mV from rail
- V_{CM} @ 5 V -0.3 V to 4.3 V
- Stable with High Capacitive Loads (Refer to Application Section)

Applications

- Cordless Phones
- Cellular Phones
- Laptops
- PDAs
- PCMCIA

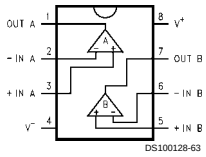
Connection Diagrams

5-Pin SC70-5/SOT23-5



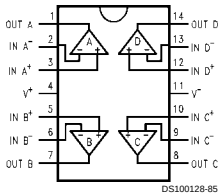
Top View

8-Pin SO/MSOP



Top View

14-Pin SO/TSSOP



Top View

2.0 DEVICE INFORMATION

Ordering Information

Package	Temperature Range Industrial −40˚C to +85˚C	Packaging Marking	Transport Media	NSC Drawing
5-Pin SC-70-5	LMV821M7	A15	250 Units Tape and Reel	MAA05
	LMV821M7X	A15	3k Units Tape and Reel	
5-Pin SOT23-5	LMV821M5	A14	250 UnitsTape and Reel	MA05B
	LMV821M5X	A14	3k Units Tape and Reel	
8-Pin SO	LMV822M	LMV822M	Rails	M08A
	LMV822MX	LMV822M	2.5k Units Tape and Reel	
8-Pin MSOP	LMV822MM	LMV822	250 Units Tape and Reel	MUA08A
	LMV822MMX	LMV822	3.5k Units Tape and Reel	
14-Pin SO	LMV824M	LMV824M	Rails	M14A
	LMV824MX	LMV824M	2.5k Units Tape and Reel	
14-Pin TSSOP	LMV824MT	LMV824MT	Rails	MTC14
	LMV824MTX	LMV824MT	2.5k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	100V
Human Body Model	
LMV822/824	2000V
LMV821	1500V
Differential Input Voltage	± Supply Voltage
Supply Voltage (V^+–V^-)	5.5V
Output Short Circuit to V^+ (Note 3)	
Output Short Circuit to V^- (Note 3)	
Mounting Temp.	
Lead Temp. (Soldering, 10 sec)	260˚C
Infrared (10 sec)	215˚C
Storage Temperature Range	−65˚C to 150˚C
Junction Temperature (Note 4)	150˚C

Operating Ratings (Note 1)

Supply Voltage	2.5V to 5.5V
Temperature Range	
LMV821, LMV822, LMV824	−40˚C ≤T_J ≤85˚C
Thermal Resistance (θ_{JA})	
Ultra Tiny SC70-5 Package	440 ˚C/W
5-Pin Surface Mount	
Tiny SOT23-5 Package 5-Pin Surface Mount	265 ˚C/W
SO Package, 8-Pin Surface Mount	190 ˚C/W
MSOP Package, 8-Pin Mini Surface Mount	235 ˚C/W
SO Package, 14-Pin Surface Mount	145 ˚C/W
TSSOP Package, 14-Pin	155 ˚C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	3	mV
				4	max
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/˚C
I_B	Input Bias Current		30	90	nA
				140	max
I_{OS}	Input Offset Current		0.5	30	nA
				50	max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.7V	85	70	dB
				68	min
+PSRR	Positive Power Supply Rejection Ratio	1.7V ≤ V^+ ≤ 4V, V^- = 1V, V_O = 0V, V_{CM} = 0V	85	75	dB
				70	min
−PSRR	Negative Power Supply Rejection Ratio	-1.0V ≤ V^- ≤ -3.3V, V^+ =1.7V, V_O= 0V, V_{CM} = 0V	85	75	dB
				70	min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2	V
					max
			2.0	1.9	V
					min
A_V	Large Signal Voltage Gain	Sourcing, R_L=600Ω to 1.35V, V_O=1.35V to 2.2V	100	90	dB
				85	min
		Sinking, R_L=600Ω to 1.35V, V_O=1.35V to 0.5V	90	85	dB
				80	min
		Sourcing, R_L=2kΩ to 1.35V, V_O=1.35V to 2.2V	100	95	dB
				90	min
		Sinking, R_L=2kΩ to 1.35, V_O=1.35 to 0.5V	95	90	dB
				85	min

2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
V_O	Output Swing	V^+=2.7V, R_L= 600Ω to 1.35V	2.58	2.50	V
				2.40	min
			0.13	0.20	V
				0.30	max
		V^+=2.7V, R_L= 2kΩ to 1.35V	2.66	2.60	V
				2.50	min
			0.08	0.120	V
				0.200	max
I_O	Output Current	Sourcing, V_O=0V	16	12	mA
					min
		Sinking, V_O=2.7V	36	20	mA
					min
I_S	Supply Current	LMV821 (Single)	0.22	0.3	mA
				0.5	max
		LMV822 (Dual)	0.45	0.6	mA
				0.8	max
		LMV824 (Quad)	0.72	1.0	mA
				1.2	max

2.5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.5V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.25V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	3	mV
				4	max
V_O	Output Swing	V^+=2.5V, R_L= 600Ω to 1.25V	2.37	2.30	V
				2.20	min
			0.13	0.20	V
				0.30	max
		V^+=2.5V, R_L= 2kΩ to 1.25V	2.46	2.40	V
				2.30	min
			0.08	0.12	V
				0.20	max

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
SR	Slew Rate	(Note 7)	1.5		V/µs
GBW	Gain-Bandwdth Product		5		MHz
Φ_m	Phase Margin		61		Deg.
G_m	Gain Margin		10		dB
	Amp-to-Amp Isolation	(Note 8)	135		dB
e_n	Input-Related Voltage Noise	f = 1 kHz, V_{CM} = 1V	28		$\frac{nV}{\sqrt{Hz}}$

2.7V AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
i_n	Input-Referred Current Noise	f = 1 kHz	0.1		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = −2, R_L = 10 kΩ, V_O = 4.1 V_{PP}	0.01		%

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 **Limit** (Note 6)	Units
V_{OS}	Input Offset Voltage		1	3	mV
				4.0	max
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/˚C
I_B	Input Bias Current		40	100	nA
				150	max
I_{OS}	Input Offset Current		0.5	30	nA
				50	max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4.0V	90	72	dB
				70	min
+PSRR	Positive Power Supply Rejection Ratio	1.7V ≤ V^+ ≤ 4V, V^- = 1V, V_O = 0V, V_{CM} = 0V	85	75	dB
				70	min
−PSRR	Negative Power Supply Rejection Ratio	-1.0V ≤ V^- ≤ -3.3V, V^+ =1.7V, V_O = 0V, V_{CM} = 0V	85	75	dB
				70	min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2	V
					max
			4.3	4.2	V
					min
A_V	Large Signal Voltage Gain	Sourcing, R_L=600Ω to 2.5V, V_O=2.5 to 4.5V	105	95	dB
				90	min
		Sinking, R_L=600Ω to 2.5V, V_O=2.5 to 0.5V	105	95	dB
				90	min
		Sourcing, R_L=2kΩ to 2.5V, V_O=2.5 to 4.5V	105	95	dB
				90	min
		Sinking, R_L=2kΩ to 2.5, V_O=2.5 to 0.5V	105	95	dB
				90	min
V_O	Output Swing	V^+=5V,R_L= 600Ω to 2.5V	4.84	4.75	V
				4.70	min
			0.17	0.250	V
				.30	max
		V^+=5V, R_L=2kΩ to 2.5V	4.90	4.85	V
				4.80	min
			0.10	0.15	V
				0.20	max

5V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
I_O	Output Current	Sourcing, V_O=0V	45	20	mA
				15	min
		Sinking, V_O=5V	40	20	mA
				15	min
I_S	Supply Current	LMV821 (Single)	0.30	0.4	mA
				0.6	max
		LMV822 (Dual)	0.5	0.7	mA
				0.9	max
		LMV824 (Quad)	1.0	1.3	mA
				1.5	max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 5V, V^- = 0V, V_{CM} = 2V, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
SR	Slew Rate	(Note 7)	2.0	1.5	V/µs min
GBW	Gain-Bandwdth Product		5.6		MHz
Φ_m	Phase Margin		67		Deg.
G_m	Gain Margin		15		dB
	Amp-to-Amp Isolation	(Note 8)	135		dB
e_n	Input-Related Voltage Noise	f = 1 kHz, V_{CM} = 1V	24		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.25		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = −2, R_L = 10 kΩ, V_O = 4.1 V_{PP}	0.01		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series wth 100 pF. Machine model, 200Ω in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of 45 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

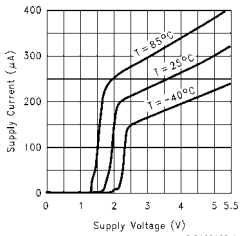
Note 7: V^+ = 5V. Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.

Note 8: Input referred, V^+ = 5V and R_L = 100 kΩ connected to 2.5V. Each amp excited in turn with 1 kHz to produce V_O = 3 V_{PP}.

5V AC Electrical Characteristics (Continued)

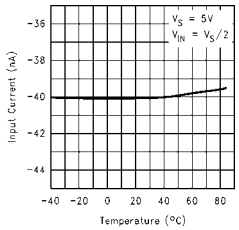
Typical Performance Characteristics Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Supply Current vs Supply Voltage (LMV821)



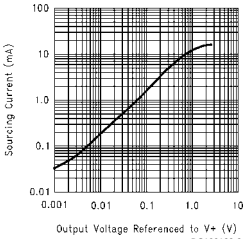
DS100128-1

Input Current vs Temperature



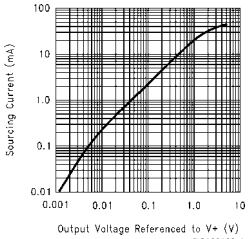
DS100128-2

Sourcing Current vs Output Voltage (V_S=2.7V)



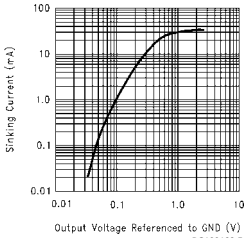
DS100128-3

Sourcing Current vs Output Voltage (V_S=5V)



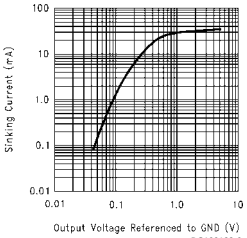
DS100128-4

Sinking Current vs Output Voltage (V_S=2.7V)



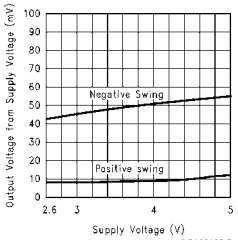
DS100128-5

Sinking Current vs Output Voltage (V_S=5V)



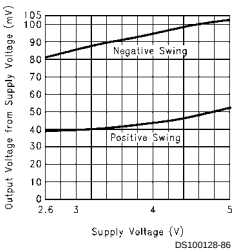
DS100128-6

Output Voltage Swing vs Supply Voltage (R_L=10kΩ)



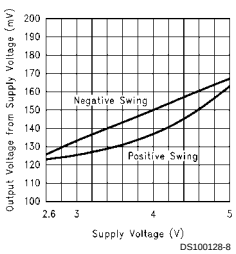
DS100128-7

Output Voltage Swing vs Supply Voltage (R_L=2kΩ)



DS100128-86

Output Voltage Swing vs Supply Voltage (R_L=600Ω)

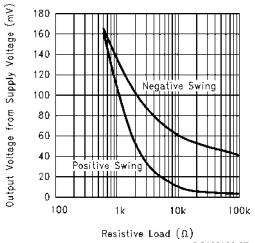


DS100128-8

Typical Performance Characteristics

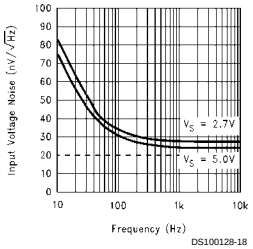
Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

Output Voltage Swing vs Load Resistance



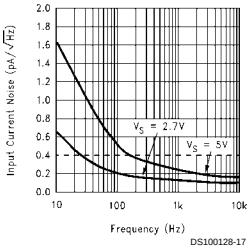
DS100128-87

Input Voltage Noise vs Frequency



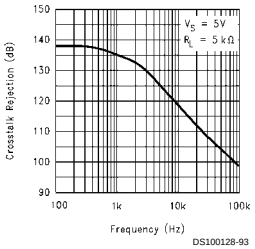
DS100128-18

Input Current Noise vs Frequency



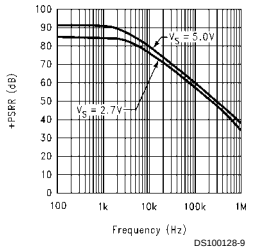
DS100128-17

Crosstalk Rejection vs Frequency



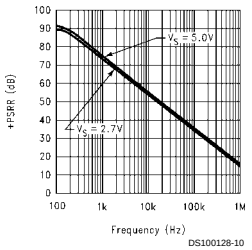
DS100128-93

+PSRR vs Frequency



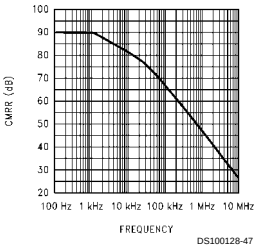
DS100128-9

-PSRR vs Frequency



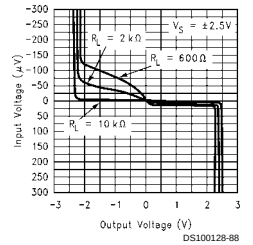
DS100128-10

CMRR vs Frequency



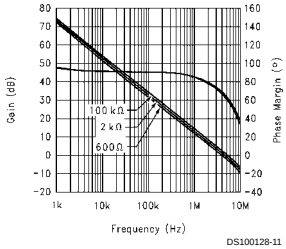
DS100128-47

Input Voltage vs Output Voltage



DS100128-88

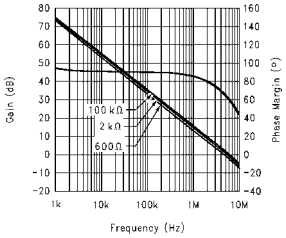
Gain and Phase Margin vs Frequency (R_L=100kΩ, 2kΩ, 600Ω) 2.7V



DS100128-11

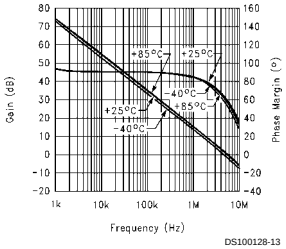
Typical Performance Characteristics Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

Gain and Phase Margin vs Frequency (R_L=100kΩ, 2kΩ, 600Ω) 5V



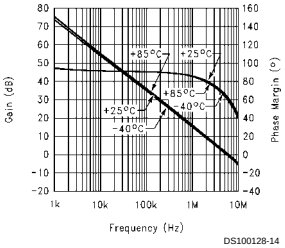
DS100128-12

Gain and Phase Margin vs Frequency (Temp.=25, -40, 85˚C, R_L= 10kΩ) 2.7V



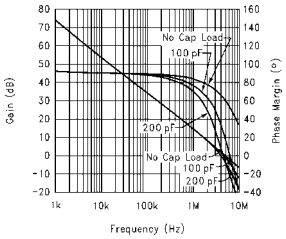
DS100128-13

Gain and Phase Margin vs Frequency (Temp.=25, -40, 85 ˚C, R_L=10kΩ) 5V



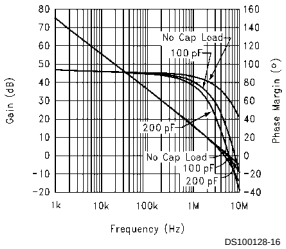
DS100128-14

Gain and Phase Margin vs Frequency (C_L=100pF, 200pF, 0pF, R_L=10kΩ)2.7V



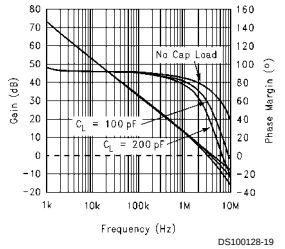
DS100128-15

Gain and Phase Margin vs Frequency (C_L=100pF,200pF,0pF R_L=10kΩ)5V



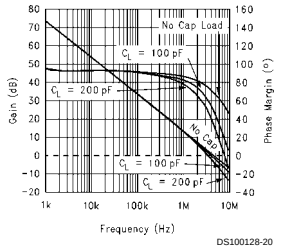
DS100128-16

Gain and Phase Margin vs Frequency (C_L=100pF,200pF,0pF R_L=600Ω)2.7V



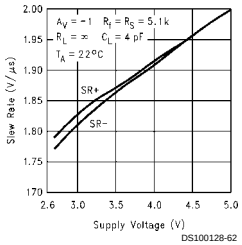
DS100128-19

Gain and Phase Margin vs Frequency (C_L=100pF,200pF,0pF R_L=600Ω)5V



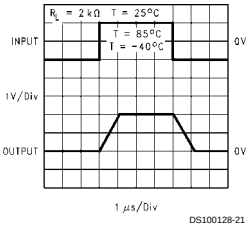
DS100128-20

Slew Rate vs Supply Voltage



DS100128-62

Non-Inverting Large Signal Pulse Response

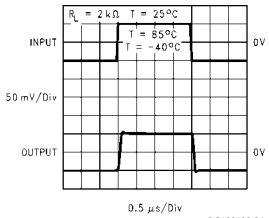


DS100128-21

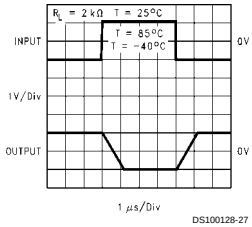
Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

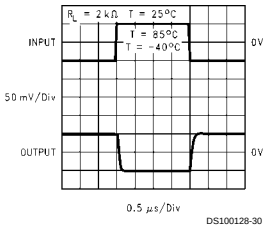
Non-Inverting Small Signal Pulse Response



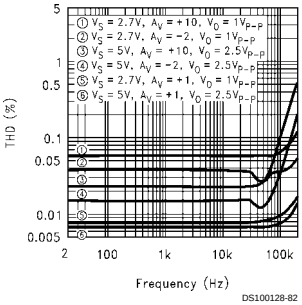
Inverting Large Signal Pulse Response



Inverting Small Signal Pulse Response



THD vs Frequency



APPLICATION NOTE

This application note is divided into two sections: design considerations and Application Circuits.

1.0 Design Considerations

This section covers the following design considerations:

1. Frequency and Phase Response Considerations
2. Unity-Gain Pulse Response Considerations
3. Input Bias Current Considerations

1.1 Frequency and Phase Response Considerations

The relationship between open-loop frequency response and open-loop phase response determines the closed-loop stability performance (negative feedback). The open-loop phase response causes the feedback signal to shift towards becoming positive feedback, thus becoming unstable. The further the output phase angle is from the input phase angle, the more stable the negative feedback will operate. Phase Margin (ϕ_m) specifies this output-to-input phase relationship at the unity-gain crossover point. Zero degrees of phase-margin means that the input and output are completely in phase with each other and will sustain oscillation at the unity-gain frequency.

The AC tables show ϕ_m for a no load condition. But ϕ_m changes with load. The Gain and Phase vs Frequency plots in the curve section can be used to graphically determine the ϕ_m for various loaded conditions. To do this, examine the phase angle portion of the plot, find the phase margin point at the unity-gain frequency, and determine how far this point is from zero degree of phase-margin. The larger the phase-margin, the more stable the circuit operation.

The bandwidth is also affected by load. The graphs of *Figure 1* and *Figure 2* provide a quick look at how various loads affect the ϕ_m and the bandwidth of the LMV821/822/824 family. These graphs show capacitive loads reducing both ϕ_m and bandwidth, while resistive loads reduce the bandwidth but increase the ϕ_m. Notice how a 600Ω resistor can be added in parallel with 220 picofarads capacitance, to increase the ϕ_m 20˚(approx.), but at the price of about a 100 kHz of bandwidth.

Overall, the LMV821/822/824 family provides good stability for loaded condition.

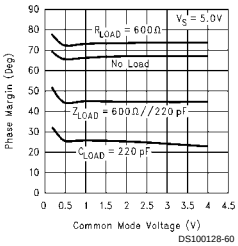


FIGURE 1. Phase Margin vs Common Mode Voltage for Various Loads

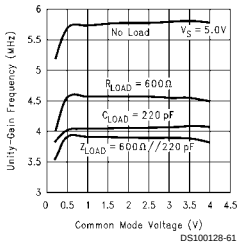


FIGURE 2. Unity-Gain Frequency vs Common Mode Voltage for Various Loads

1.2 Unity Gain Pulse Response Considerations

A pull-up resistor is well suited for increasing unity-gain, pulse response stability. For example, a 600 Ω pull-up resistor reduces the overshoot voltage by about 50%, when driving a 220 pF load. *Figure 3* shows how to implement the pull-up resistor for more pulse response stability.

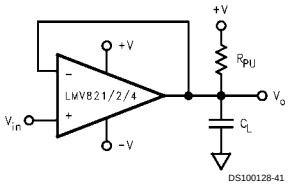


FIGURE 3. Using a Pull-up Resistor at the Output for Stabilizing Capacitive Loads

Higher capacitances can be driven by decreasing the value of the pull-up resistor, but its value shouldn't be reduced beyond the sinking capability of the part. An alternate approach is to use an isolation resistor as illustrated in *Figure 4*.

Figure 5 shows the resulting pulse response from a LMV824, while driving a 10,000pF load through a 20 Ω isolation resistor.

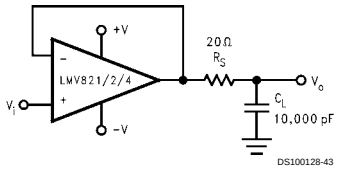
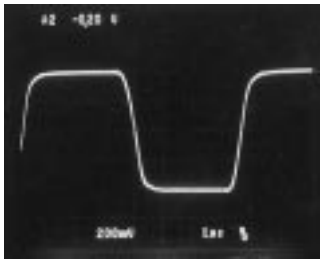


FIGURE 4. Using an Isolation Resistor to Drive Heavy Capacitive Loads

2.0 DEVICE INFORMATION

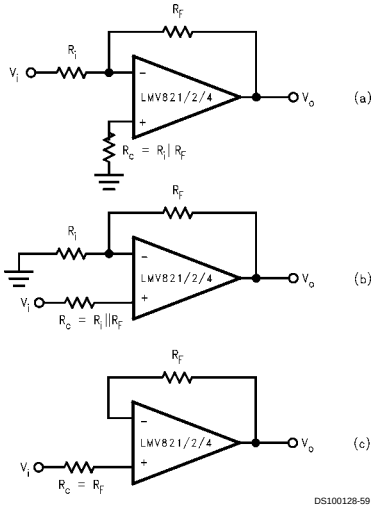


DS100128-54

FIGURE 5. Pulse Response per *Figure 4*

1.3 Input Bias Current Consideration

Input bias current (I_B) can develop a somewhat significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F. For example, if I_B is 90nA (max room) and R_F is 100 kΩ, then an offset of 9 mV will be developed (V_{OS}=I_Bx R_F).Using a compensation resistor (R_C), as shown in *Figure 6*, cancels out this affect. But the input offset current (I_{OS}) will still contribute to an offset voltage in the same manner - typically 0.05 mV at room temp.



DS100128-59

FIGURE 6. Canceling the Voltage Offset Effect of Input Bias Current

2.0 APPLICATION CIRCUITS

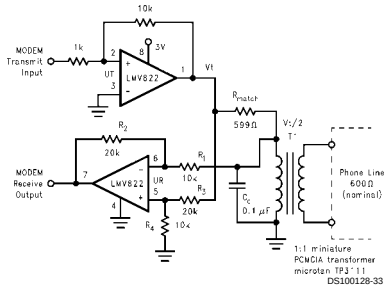
This section covers the following application circuits:

1. Telephone-Line Transceiver
2. "Simple" Mixer (Amplitude Modulator)
3. Dual Amplifier Active Filters (DAAFs)
   - a. Low-Pass Filter (LPF)
   - b. High-Pass Filter (HPF)
5. Tri-level Voltage Detector

2.1 Telephone-Line Transceiver

The telephone-line transceiver of *Figure 7* provides a full-duplexed connection through a PCMCIA, miniature transformer. The differential configuration of receiver portion (UR), cancels reception from the transmitter portion (UT). Note that the input signals for the differential configuration of UR, are the transmit voltage (Vt) and Vt/2. This is because R_{match} is chosen to match the coupled telephone-line impedance; therefore dividing Vt by two (assuming R1 >> R3). The differential configuration of UR has its resistor chosen to cancel the Vt and Vt/2 inputs according to the following equation:

$$V_O = V_T\left(\frac{R_3}{R_3+R_4}\right)\left(1+\frac{R_2}{R_1}\right) - \frac{V_T}{2}\left(\frac{R_2}{R_1}\right) = V_T\,\frac{1}{3}\,(3) - \frac{V_T}{2}(2) = 0$$



DS100128-33

FIGURE 7. Telephone-line Transceiver for a PCMCIA Modem Card

Note that Cr is included for canceling out the inadequacies of the lossy, miniature transformer. Refer to application note AN-397 for detailed explanation.

2.2"Simple" Mixer (Amplitude Modulator)

The mixer of *Figure 8* is simple and provides a unique form of amplitude modulation. Vi is the modulation frequency (F_M), while a +3V square-wave at the gate of Q1, induces a carrier frequency (F_C). Q1 switches (toggles) U1 between inverting and non-inverting unity gain configurations. Offsetting a sine wave above ground at Vi results in the oscilloscope photo of *Figure 9*.

The simple mixer can be applied to applications that utilize the Doppler Effect to measure the velocity of an object. The difference frequency is one of its output frequency components. This difference frequency magnitude (/F_M-F_C/) is the key factor for determining an object's velocity per the Doppler Effect. If a signal is transmitted to a moving object, the reflected frequency will be a different frequency. This difference in transmit and receive frequency is directly proportional to an object's velocity.

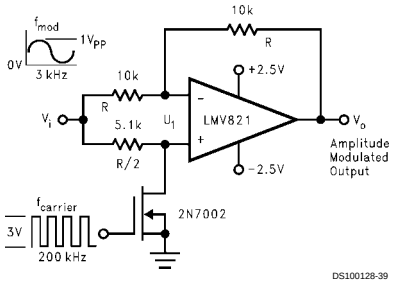


FIGURE 8. Amplitude Modulator Circuit

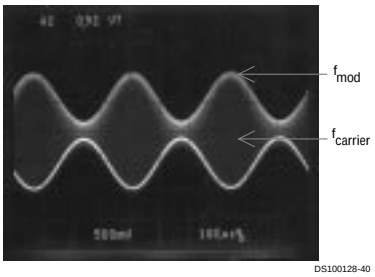


FIGURE 9. Output signal per the Circuit of *Figure 8*

2.4 Dual Amplifier Active Filters (DAAFs)

The LMV822/24 bring economy and performance to DAAFs. The low-pass and the high-pass filters of *Figure 10* and *Figure 11* (respectively), offer one key feature: excellent sensitivity performance. Good sensitivity is when deviations in component values cause relatively small deviations in a filter's parameter such as cutoff frequency (Fc). Single amplifier active filters like the Sallen-Key provide relatively poor sensitivity performance that sometimes cause problems for high production runs; their parameters are much more likely to deviate out of specification than a DAAF would. The DAAFs of *Figure 10* and *Figure 11* are well suited for high volume production.

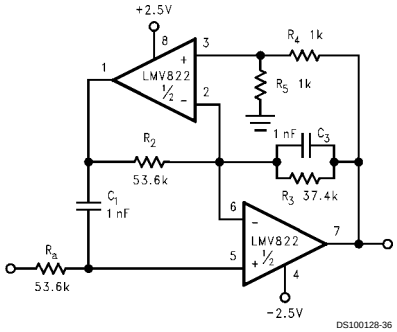


FIGURE 10. Dual Amplifier, 3 kHz Low-Pass Active Filter with a Butterworth Response and a Pass Band Gain of Times Two

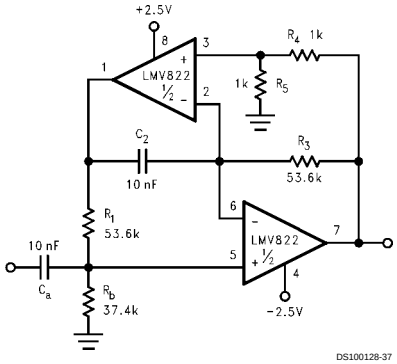


FIGURE 11. Dual Amplifier, 300 Hz High-Pass Active Filter with a Butterworth Response and a Pass Band Gain of Times Two

Table 1 provides sensitivity measurements for a 10 MΩ condition. The left column shows the passive components for the 3 kHz low-pass DAAF. The third column shows the components for the 300 Hz high-pass DAAF. Their respective sensitivity measurements are shown to the right of each component column. Their values consists of the percent change in cutoff frequency (Fc) divided by the percent change in component value. The lower the sensitivity value, the better the performance.

Each resistor value was changed by about 10 percent, and this measured change was divided into the measured change in Fc. A positive or negative sign in front of the measured value, represents the direction Fc changes relative to components' direction of change. For example, a sensitivity value of negative 1.2, means that for any 1 percent increase in component value, Fc decreases by 1.2 percent.

Note that this information provides insight on how to fine tune the cutoff frequency, if necessary. It should be also noted that R_4 and R_5 of each circuit also caused variations in

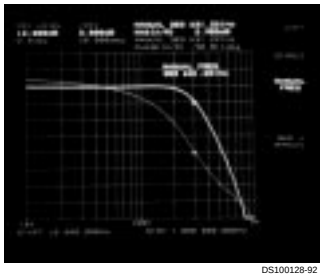
the pass band gain. Increasing R_4 by ten percent, increased the gain by 0.4 dB, while increasing R_5 by ten percent, decreased the gain by 0.4 dB.

TABLE 1

Component (LPF)	Sensitivity (LPF)	Component (HPF)	Sensitivity (HPF)
R_a	-1.2	C_a	-0.7
C_1	-0.1	R_b	-1.0
R_2	-1.1	R_1	+0.1
R_3	+0.7	C_2	-0.1
C_3	-1.5	R_3	+0.1
R_4	-0.6	R_4	-0.1
R5	+0.6	R_5	+0.1

Active filters are also sensitive to an op amp's parameters -Gain and Bandwidth, in particular. The LMV822/24 provide a large gain and wide bandwidth. And DAAFs make excellent use of these feature specifications.

Single Amplifier versions require a large open-loop to closed-loop gain ratio - approximately 50 to 1, at the Fc of the filter response. *Figure 12* shows an impressive photograph of a network analyzer measurement (hp3577A). The measurement was taken from a 300kHz version of *Figure 10*. At 300 kHz, open-loop to closed-loop gain ratio (Fc) about 5 to 1 (footnote). This is 10 times lower than the 50 to 1 "rule of thumb" for Single Amplifier Active Filters.



DS100128-92

FIGURE 12. 300 kHz, Low-Pass Filter, Butterworth Response as Measured by the HP3577A Network Analyzer

In addition to performance, DAAFs are relatively easy to design and implement. The design equations for the low-pass and high-pass DAAFs are shown below. The first two equation calculate the Fc and the circuit Quality Factor (Q) for the LPF (*Figure 10*). The second two equations calculate the Fc and Q for the HPF (*Figure 11*).

$$\text{(LPF)} \quad F_C = \frac{\sqrt{R_5}}{2\pi\sqrt{R_a}\cdot\sqrt{R_2}\cdot\sqrt{R_4}\cdot\sqrt{C_1}\cdot\sqrt{C_3}}$$

$$Q = 2\pi F_C\sqrt{C_1}\cdot\sqrt{C_3}$$

$$\text{(HPF)} \quad F_C = \frac{\sqrt{R_4}}{2\pi\sqrt{R_1}\cdot\sqrt{R_3}\cdot\sqrt{R_5}\cdot\sqrt{C_a}\cdot\sqrt{C_2}}$$

$$Q = 2\pi F_C\sqrt{C_a}\cdot\sqrt{C_2}$$

To simplify the design process, certain components are set equal to each other. Refer to *Figure 10* and *Figure 11*. These equal component values help to simplify the design equations as follows:

$$\text{(LPF)} \quad R_a = R_2 = \frac{1}{2\pi F_C\sqrt{C_1}\cdot\sqrt{C_3}}$$

$$R_3 = \frac{Q}{2\pi F_C\sqrt{C_1}\cdot\sqrt{C_3}}$$

$$\text{(HPF)} \quad R_1 = R_3 = \frac{1}{2\pi F_C\sqrt{C_a}\cdot\sqrt{C_2}}$$

$$R_b = \frac{Q}{2\pi F_C\sqrt{C_a}\cdot\sqrt{C_2}}$$

To illustrate the design process/implementation, a 3 kHz, Butterworth response, low-pass filter DAAF (*Figure 10*) is designed as follows:

1. Choose $C_1 = C_3 = C = 1$ nF
2. Choose $R_4 = R_5 = 1$ kΩ
3. Calculate R_a and R_2 for the desired Fc as follows:

$$R_a = R_2 = \frac{1}{2\pi(F_C)C}$$

$$= \frac{1}{2\pi(3\text{ kHz})1\text{nF}}$$

$$= 53.1\text{ k}\Omega$$

$$\cong 53.6\text{ k}\Omega\text{ (Practical Value)}$$

4. Calculate R_3 for the desired Q. The desired Q for a Butterworth (Maximally Flat) response is 0.707 (45 degrees into the s-plane). R_3 calculates as follows:

$$R_3 = \frac{Q}{2\pi(F_C)C}$$

$$= \frac{0.707}{2\pi(3\text{ kHz})1\text{nF}}$$

$$= 37.5\text{ k}\Omega$$

$$\cong 37.4\text{ k}\Omega\text{ (Practical Value)}$$

Notice that R_3 could also be calculated as 0.707 of R_a or R_2.

The circuit was implemented and its cutoff frequency measured. The cutoff frequency measured at 2.92 kHz.

The circuit also showed good repeatability. Ten different LMV822 samples were placed in the circuit. The corresponding change in the cutoff frequency was less than a percent.

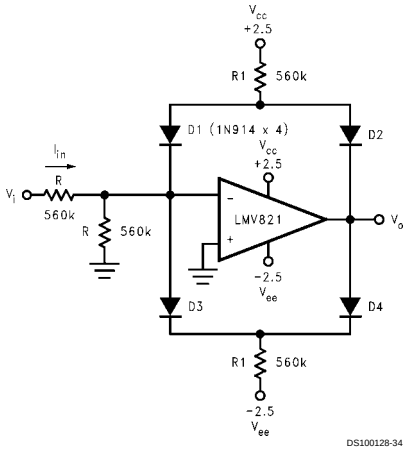
2.5 Tri-level Voltage Detector

The tri-level voltage detector of *Figure 13* provides a type of window comparator function. It detects three different input voltage ranges: Min-range, Mid-range, and Max-range. The output voltage (V_O) is at V_{CC} for the Min-range. V_O is clamped at GND for the Mid-range. For the Max-range, V_O is at V_{ee}. *Figure 14* shows a V_O vs. V_I oscilloscope photo per the circuit of .

Its operation is as follows: V_I deviating from GND, causes the diode bridge to absorb I_{IN} to maintain a clamped condition (V_O= 0V). Eventually, I_{IN} reaches the bias limit of the diode bridge. When this limit is reached, the clamping effect stops and the op amp responds open loop. The design equation directly preceding *Figure 13*, shows how to determine the clamping range. The equation solves for the input voltage band on each side GND. The mid-range is twice this voltage band.

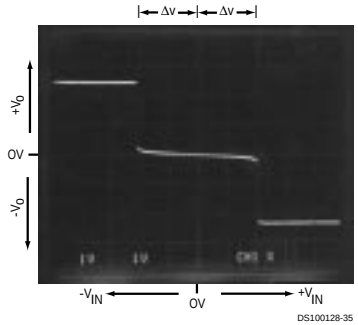
$$\Delta V = \frac{R}{R_1}(V_{CC} - V_{Diode})$$

DS100128-89



DS100128-34

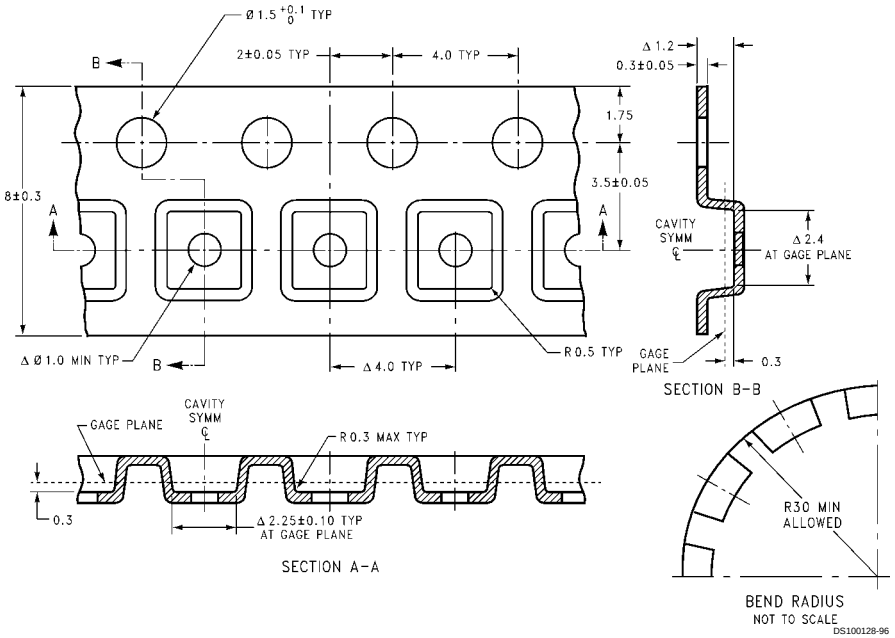
FIGURE 13. Tri-level Voltage Detector



DS100128-35

FIGURE 14. X, Y Oscilloscope Trace showing V_{OUT} vs V_{IN} per the Circuit of *Figure 13*

SC70-5 Tape and Reel Specification

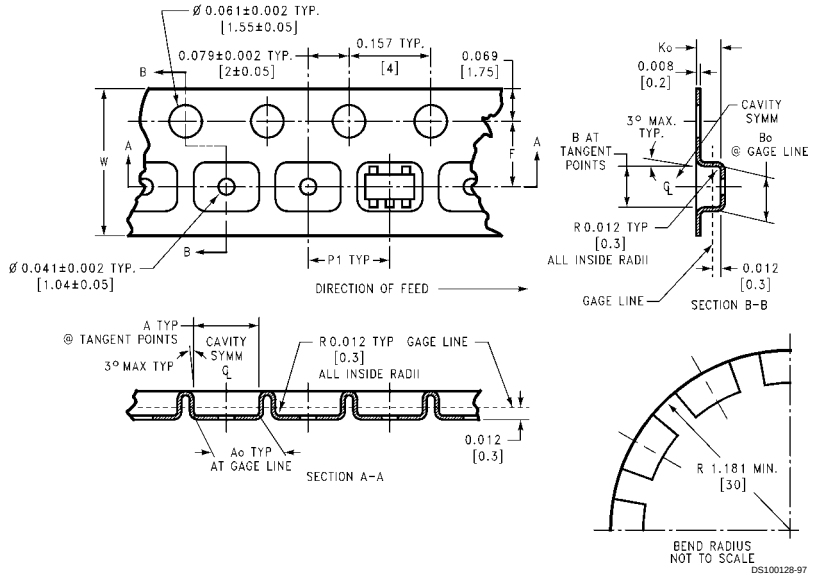


SOT-23-5 Tape and Reel Specification

Tape Format

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader	0 (min)	Empty	Sealed
(Start End)	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer	125 (min)	Empty	Sealed
(Hub End)	0 (min)	Empty	Sealed

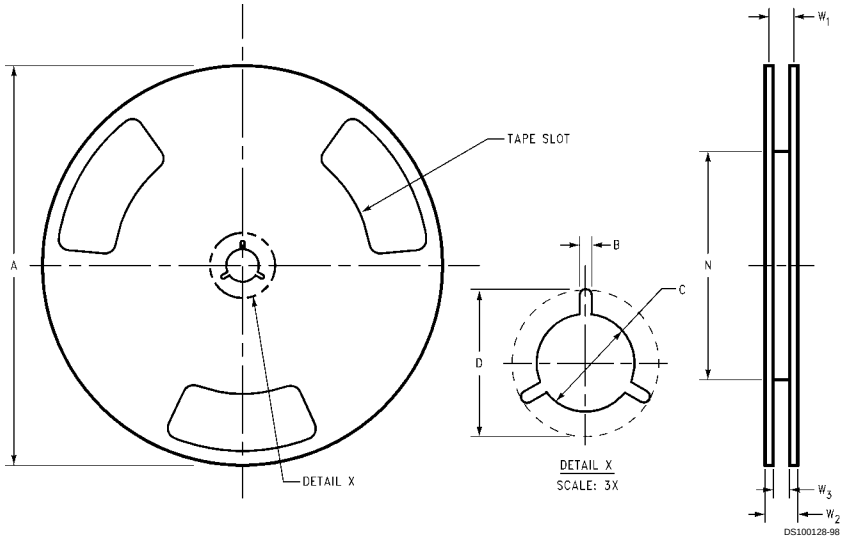
Tape Dimensions



8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ±0.002 (3.5 ±0.05)	0.055 ±0.004 (1.4 ±0.11)	0.157 (4)	0.315 ±0.012 (8 ±0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

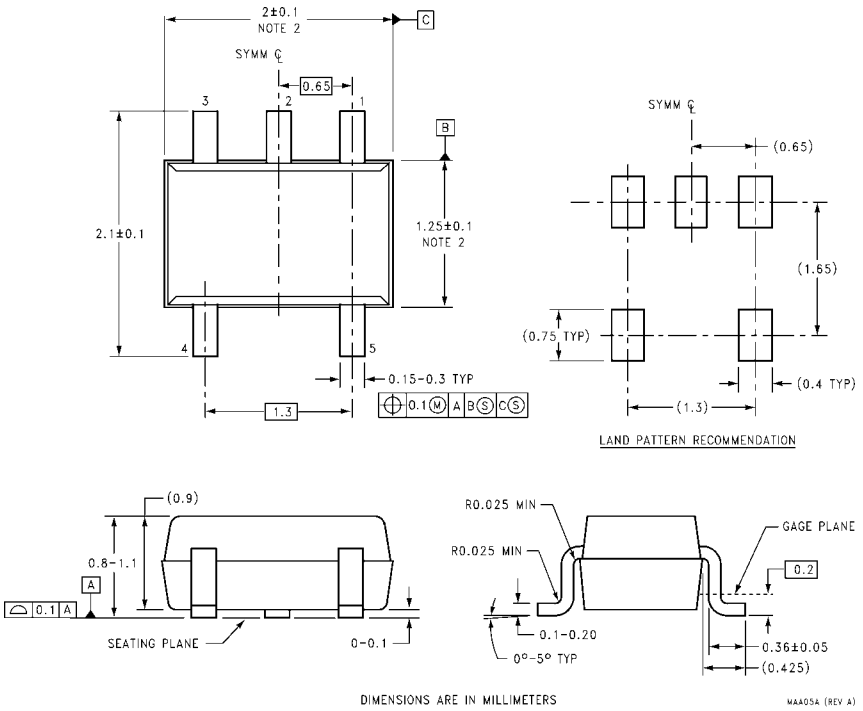
2.0 DEVICE INFORMATION

Reel Dimensions



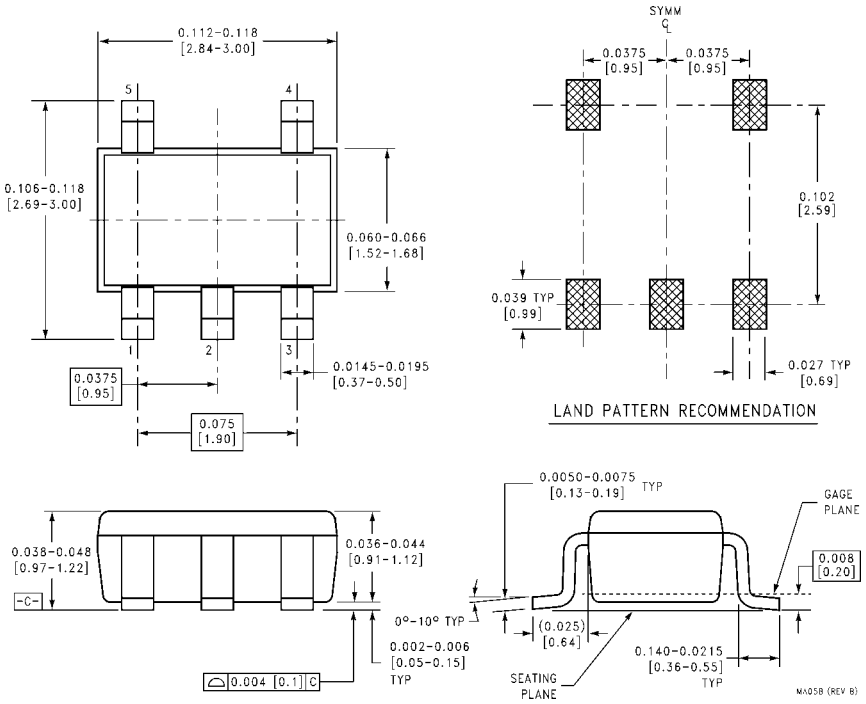
8 mm	7.00 330.00	0.059 1.50	0.512 13.00	0.795 20.20	2.165 55.00	0.331 + 0.059/−0.000 8.40 + 1.50/−0.00	0.567 14.40	W1+ 0.078/−0.039 W1 + 2.00/−1.00
Tape Size	A	B	C	D	N	W1	W2	W3

Physical Dimensions inches (millimeters) unless otherwise noted



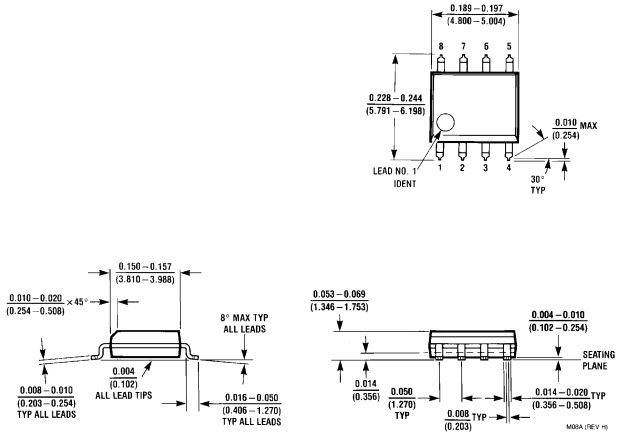
SC70-5
Order Number LMV821M7 or LMV821M7X
NS Package Number MAA05

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



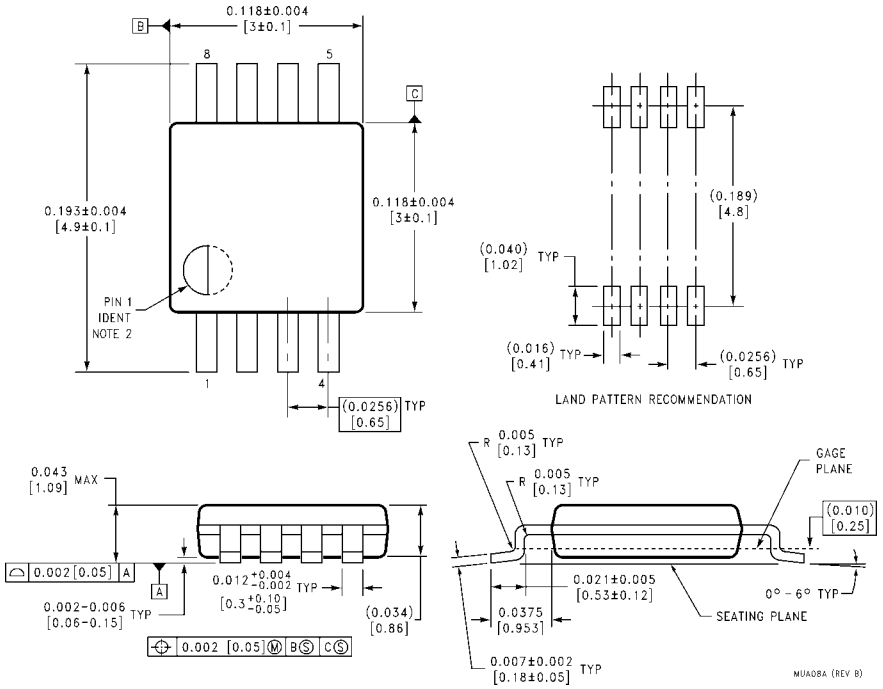
SOT 23-5
Order Number LMV821M5 or LMV821M5X
NS Package Number MA05B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



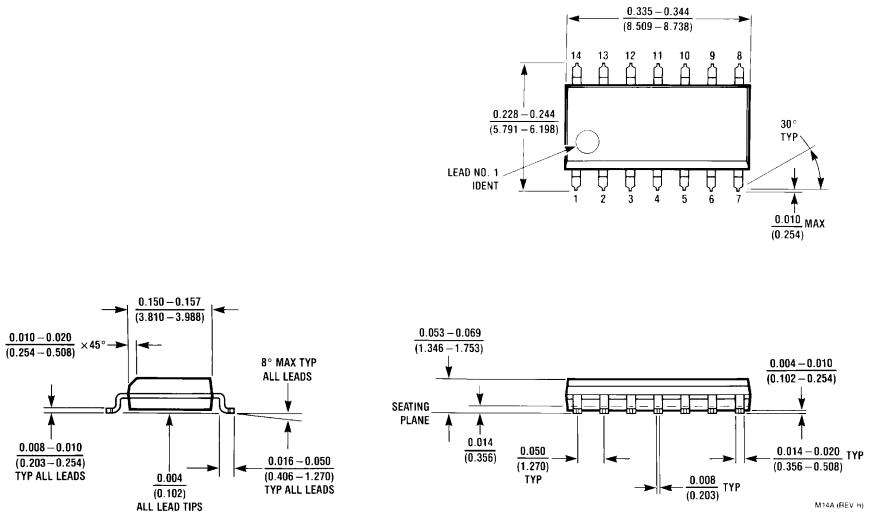
8-Pin Small Outline
Order Number LMV822M or LMV822MX
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



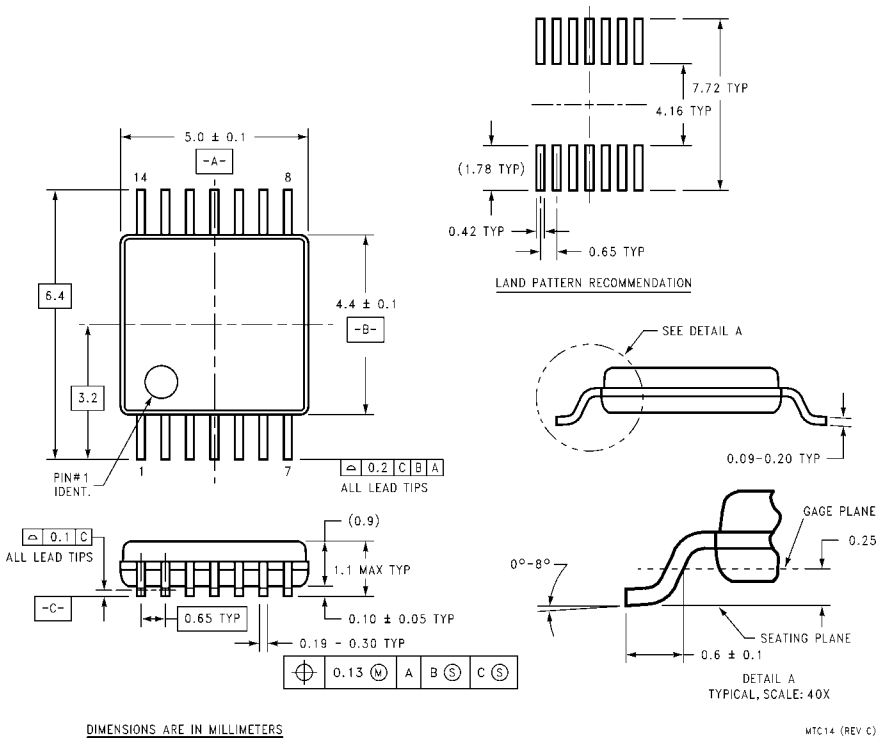
8-Pin MSOP
Order Number LMV822MM or LMV822MMX
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin Small Outline
Order Number LMV824M or LMV824MX
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin TSSOP
Order Number LMV824MTC or LMV824MTCX
NS Package Number MTC14

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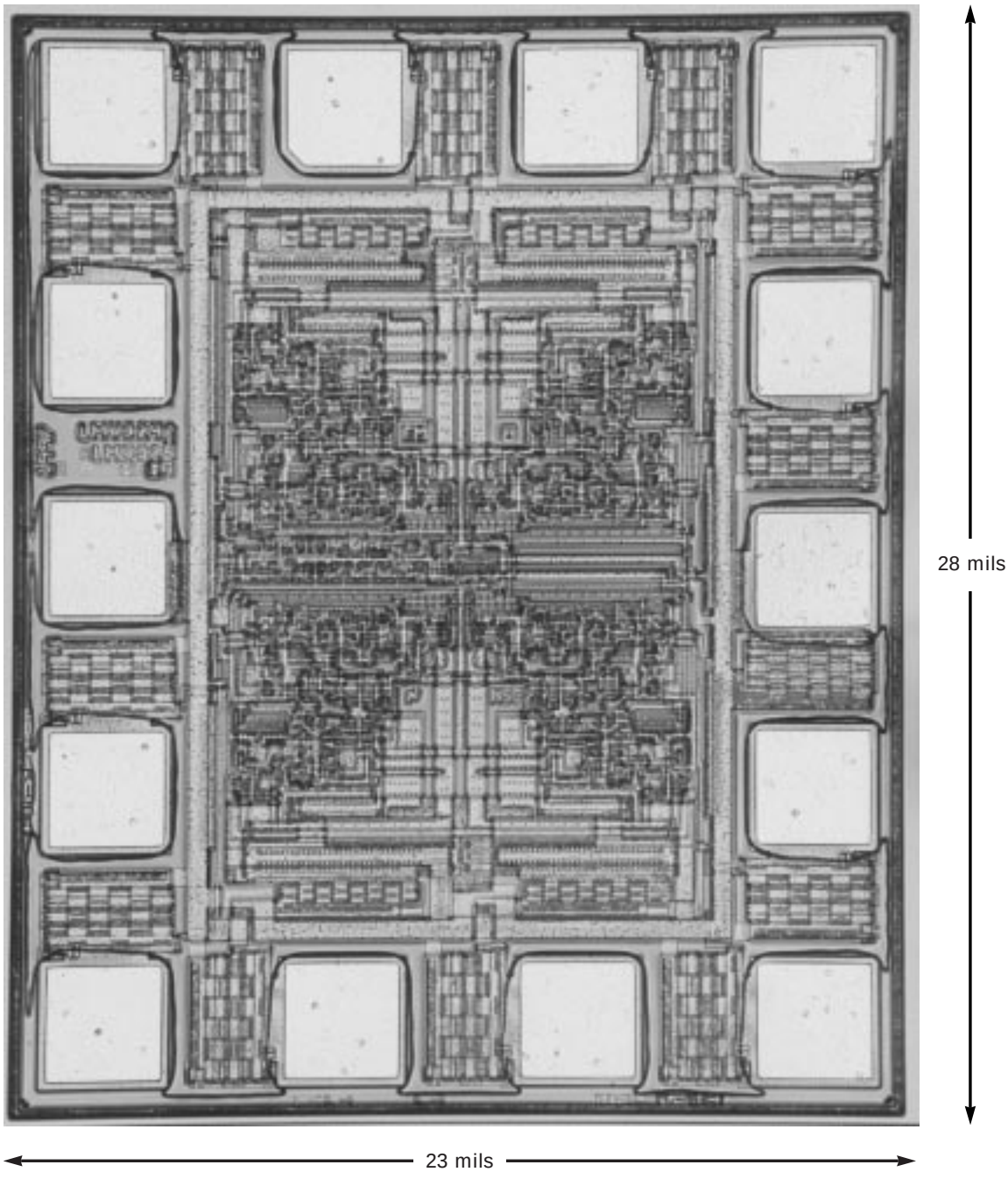
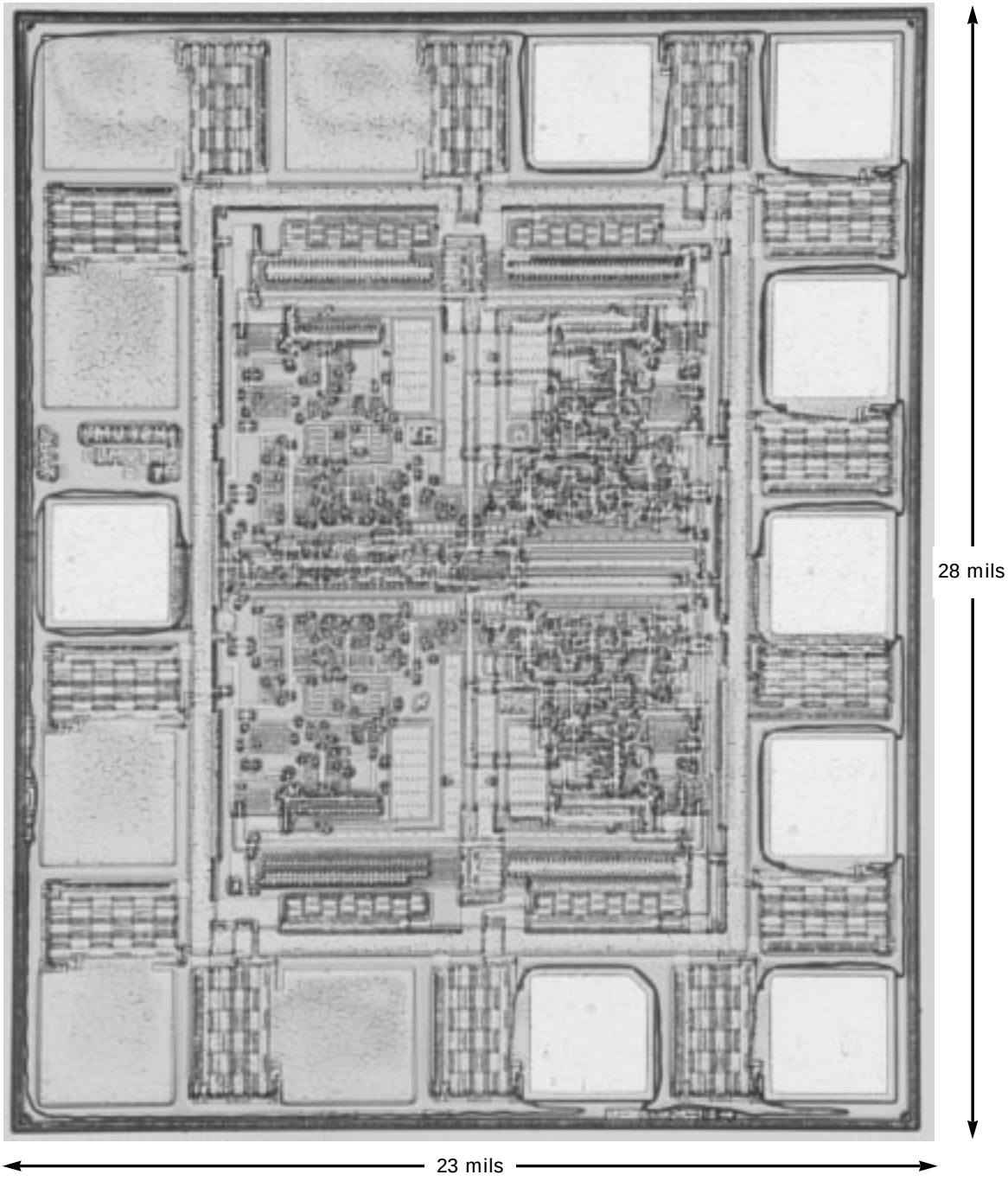
2.2 Die Photos

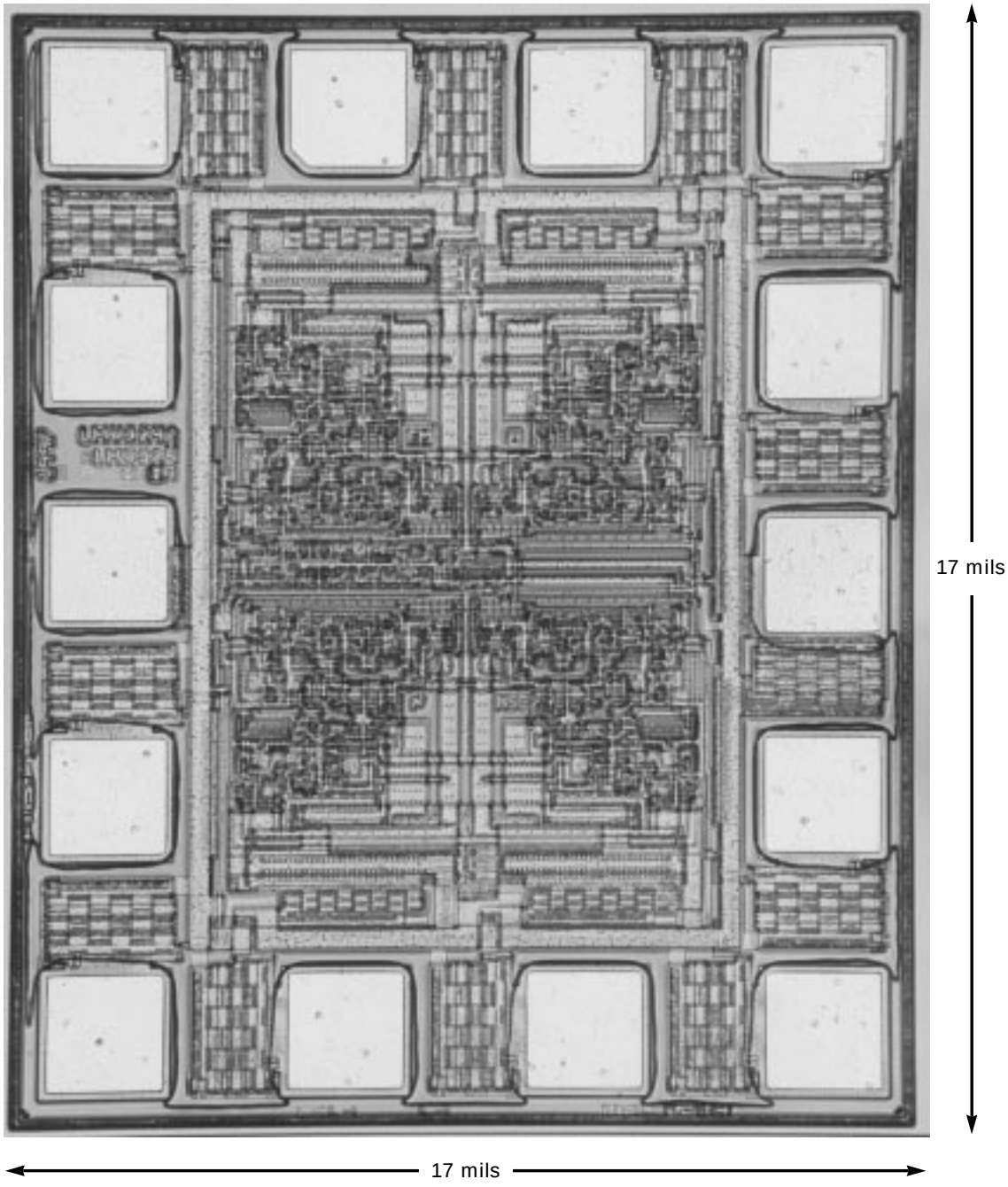
2.2.1 LMV324/339



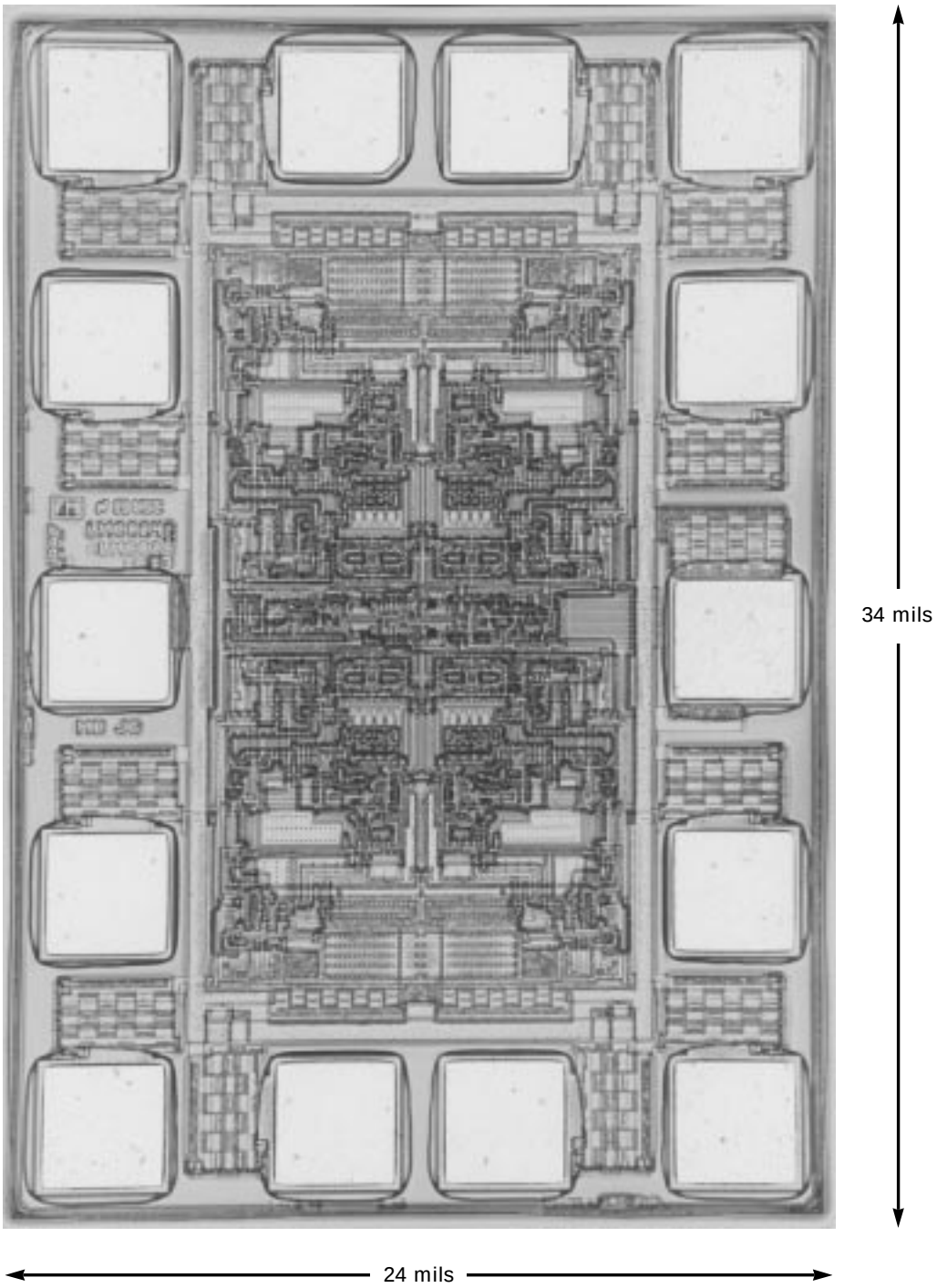
2.2.2 LMV358/393



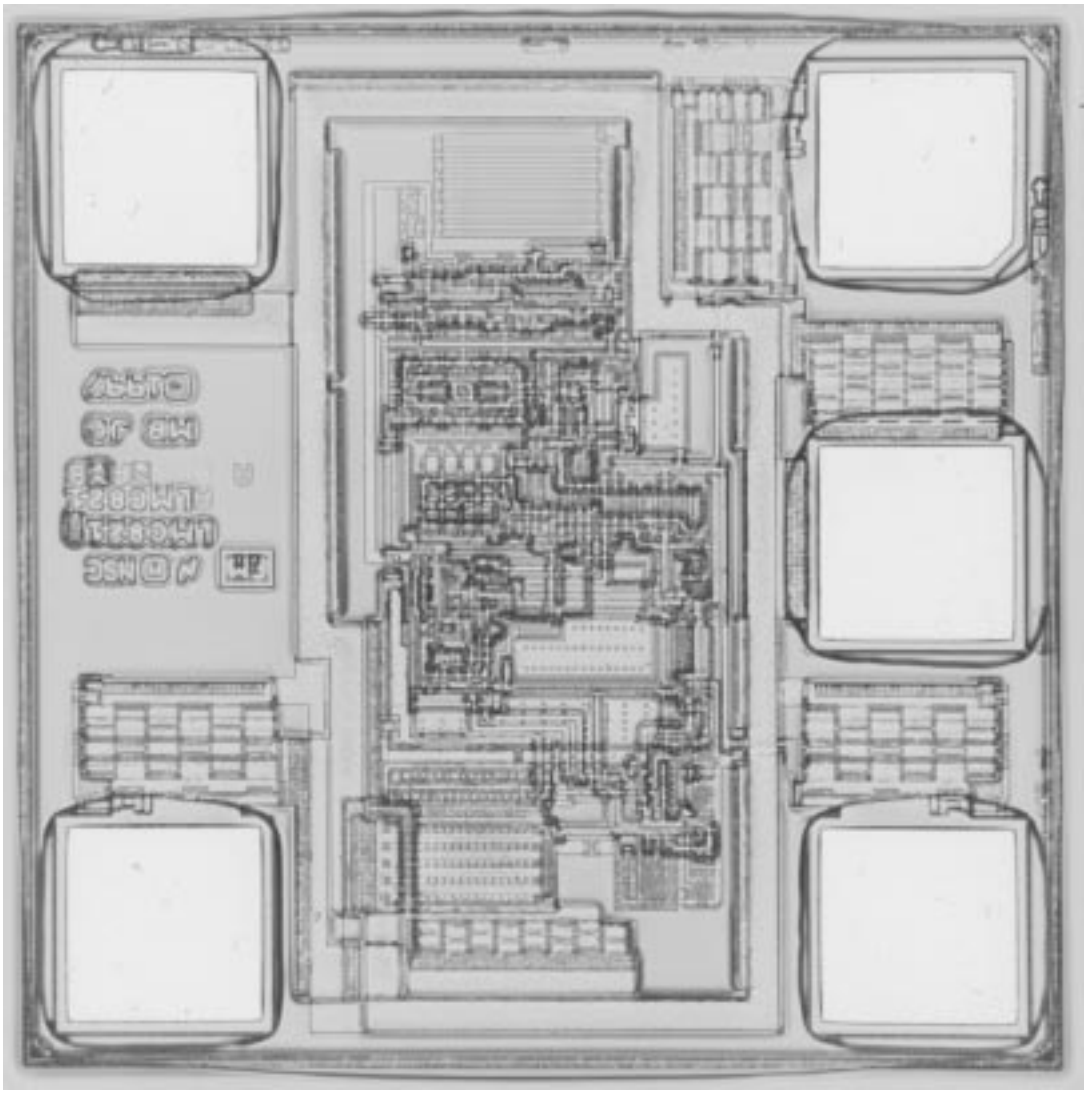
2.2.3 LMV321/331



2.2.4 LMV824/822



2.2.5 LMV821



3.0 PROCESS INFORMATION

3.1 Process Flow

Fabrication Site: South Portland Fairchild

Process Technology: CS80CBi (Submicron Silicon Gate CMOS/Bipolar)

Wafer Diameter: 6 inch

Number of Masks: 18

Metalization: 0.5% Copper, dual layer Aluminum metal,

1st layer = 7,500Å thick
2nd layer = 12,000Å thick

Top Side Passivation: Polyamide (30,000A thick)
over Nitride (11,500A thick) over Oxide (5,000A thick)

3.2 Process Detail & Masks

1: Initial Oxide
2: Trench Define & Etch
3: **Mask 0.6**, *N- Iso*
4: N- Iso Implant
5: N- Iso Drive
6: N- Iso Oxide Strip & Screen Oxide
7: **Mask 0.8,** *N+ Buried Layer*
8: N+ Buried Layer Implant
9: **Mask 0.9,** *P+ Buried Layer*
10: P+ Buried Layer Implant
11: Buried Layer Anneal
12: Epi Growth
13: Pad Oxide & Nitride
14: **Mask 1.0**, *N-Well*
15: N- Well Implant
16: Selective Oxide
17: N-Well Nitride Strip
18: P-Well Implant
19: Selective Oxide Etch
20: N- Well & P- Well Drive-In Oxide
21: Drive-In Oxide Strip
22: **Mask 2.0,** *Composite*
23: Composite Pad Oxide & Composite Nitride
24: Composite Mask Etch
25: **Mask 3.0,** *P- Field*
26: P- Field Implant
27: Iso Field Oxide
28: Active (Composite Area) Nitride Strip
29: Pad Oxide Removal & Sacrificial Oxide Growth & Vt Adjust Implant
30: Sacrificial Oxide Strip & Gate Oxide & Poly Deposition
31: Poly Dope & Poly Anneal

3.2 Process Detail & Masks (cont)

32: **Mask 4.0,** *Poly*
33: Poly Etch
34: Poly Seal Oxide
35: **Mask 4.3,** *P-LDD*
36: P-LDD Implant
37: **Mask 4.5,** *N-LDD*
38: N-LDD Implant
39: Spacer Oxide Deposit & Etch
40: **Mask 5.0,** *N+*
41: N+ Implant
42: **Mask 5.5,** *Base*
43: Base Etch & Base Implant
44: N+ Drive
45: **Mask 6.0,** *P+*
46: P+ Implant
47: Dielectric Layer1 & P+ Anneal
48: SOG
49: **Mask 7.0,** *Window*
50: Window Etch & Contact Dielectric
51: **Mask 7.1,** *Contact*
52: Contact Etch
53: Contact Plug & Etchback
54: Metal1 Deposition
55: **Mask 8.0,** *Metal1*
56: Metal1 Etch
57: Metal1 Alloy
58: Dielectric Layer2
59: **Mask 9.0,** *Via*
60: Via Etch
61: Via Deposition & Metal2 Deposit
62: **Mask 10.0,** *Metal2*
63: Metal2 Etch
64: Passivation Oxide/Nitride/Polyamide
65: **Mask 13.0,** *Passivation*
66: Passivation Etch

4.0 PACKAGING INFORMATION

4.1 PACKAGE MATERIAL & DIMENSIONS

Generic Package Type	14 Lead SOIC	14 Lead TSSOP
NS Package Number	M14A	MTC14
Package/Compound Manufacturer	Epoxy Cresol Novolac Sumitomo	Epoxy Cresol Novolac Sumitomo
Package/Compound Mfg's Designation	Sumitomo EME-1100R NSC B14	Sumitomo EME-7351LS
Lead Frame Material Manufacturer	Copper NSC-DCI	Copper
External Lead Frame Coating	Solder Plate Sn/Pb	Solder Plate Sn/Pb
Pins	Gull Wing, 9mils Thick	Gull Wing, 6mils Thick
Die Attached Method	Poly 6	Poly 6
Bond Wire	Gold, 0.9mils	Gold, 0.9mils
Bond Type	Hot Thermosonic Ball	Hot Thermosonic Ball
Package Thermal	145°C/W for LMV324 LMV824, and LMV339	155°C/W for LMV324, LMV824, and LMV339

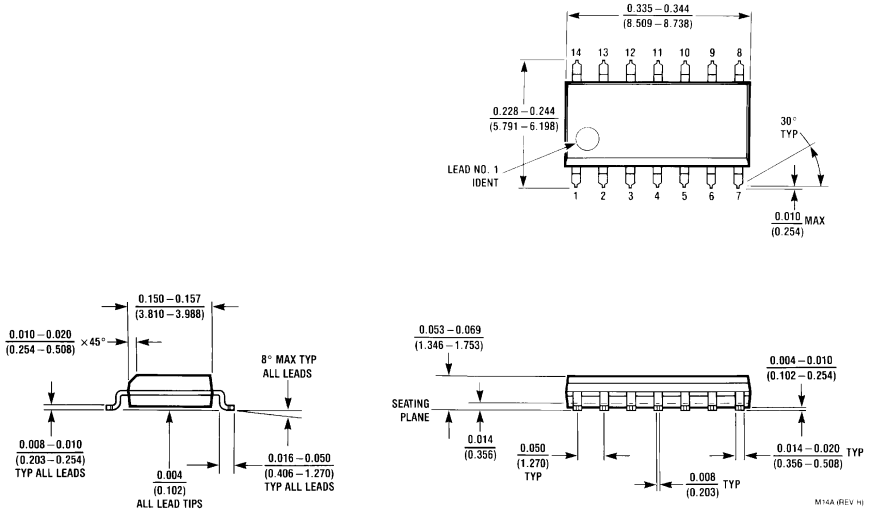
4.1 PACKAGE MATERIAL & DIMENSIONS (cont)

Generic Package Type	8 Lead SOIC	8 Lead MSOP
NS Package Number	M08A	MUA08A
Package/Compound Manufacturer	Epoxy Cresol Novolac Sumitomo	Epoxy Cresol Novolac Nitto Denko
Package/Compound Mfg's Designation	Sumitomo EME-1100R NSC B14	Nitto MP-7400
Lead Frame Material Manufacturer	Copper NSC-DCI	Copper
External Lead Frame Coating	Solder Plate Sn/Pb	Solder Plate Sn/Pb
Pins	Gull Wing, 9mils Thick	Gull Wing, 7mils Thick
Die Attached Method	Poly 6	Epoxy
Bond Wire	Gold, 0.9mils	Gold, 0.9mils
Bond Type	Hot Thermosonic Ball	Hot Thermosonic Ball
Package Thermal	190°C/W for LMV358, LMV 322, and LMV393	235°C/W for LMV358 LMV 322, and LMV393

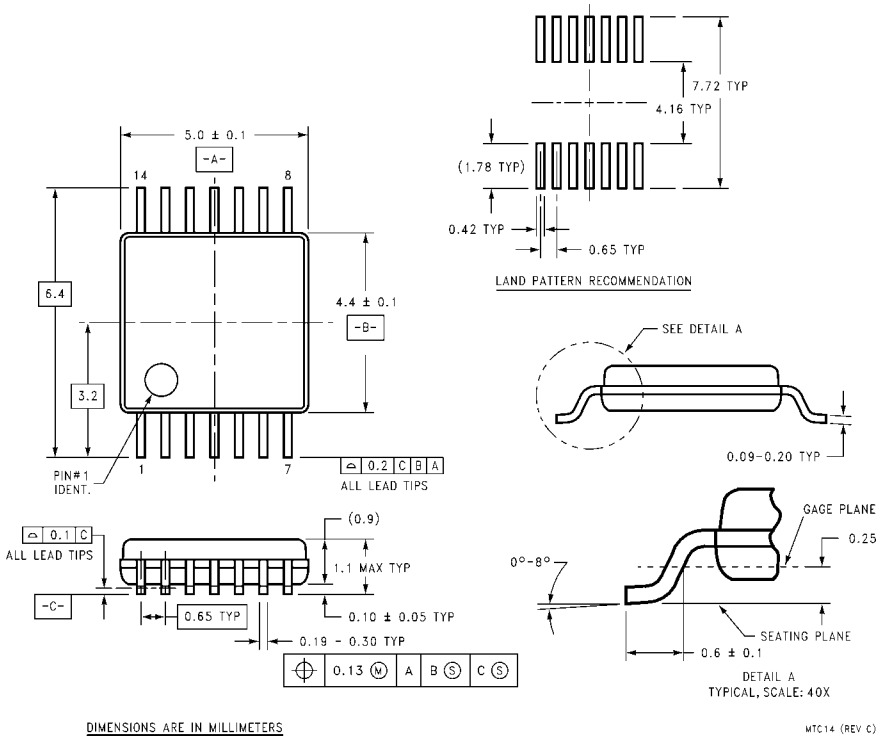
4.1 PACKAGE MATERIAL & DIMENSIONS (cont)

Generic Package Type	5 Lead SOT-23	5 Lead SC70
NS Package Number	MA05B	MAA05A
Package/Compound Manufacturer	Epoxy Cresol Novolac Sumitomo	Epoxy Cresol Novolac Nitto Denko
Package/Compound Mfg's Designation	Sumitomo EME-6710 NSC B18	Nitto MP-8000C
Lead Frame Material Manufacturer	Copper NSC-DCI	Copper Enomoto
External Lead Frame Coating	Solder Plate Sn/Pb	Solder Plate Sn/Pb
Pins	Gull Wing, 6mils Thick	Gull Wing, 6mils Thick
Die Attached Method	Eutectic, Crr/Ag/Sn	Eutectic, Crr/Ag/Sn
Bond Wire	Gold, 1.0mils	Gold, 1.0mils
Bond Type	Hot Thermosonic Ball	Hot Thermosonic Ball
Package Thermal	265°C/W for LMV321, LMV821, and LMV331	478°C/W for LMV321 LMV821, and LMV331

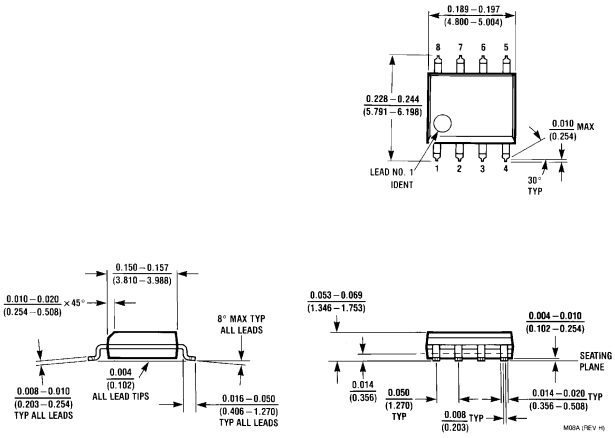
4.0 PACKAGING INFORMATION



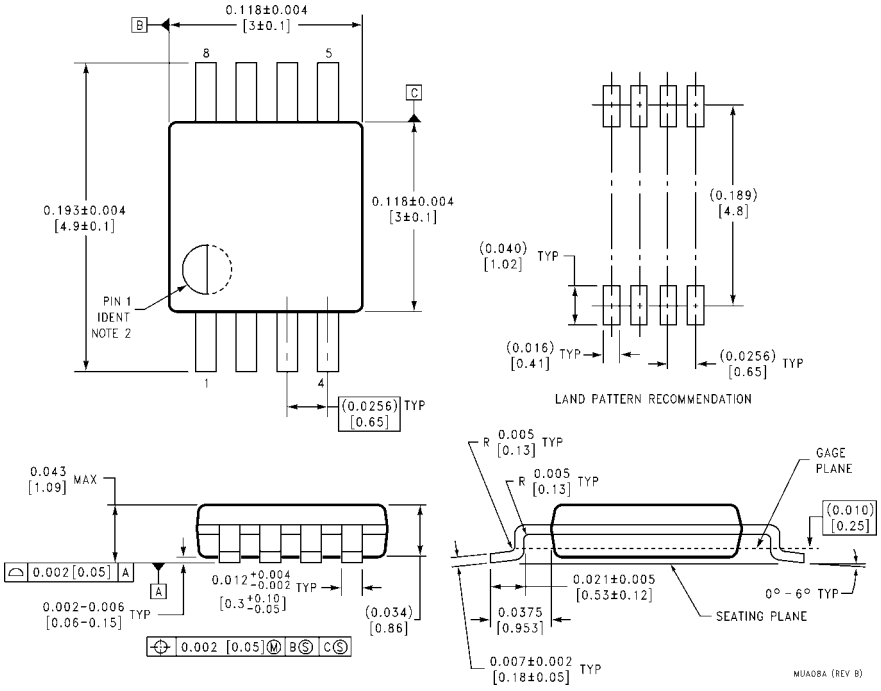
14 Pin Small Outline
Order Number LMV324M, LMV324MX, LMV339M, LMV339MX, LMV824M and LMV824MX
NS Package Number M14A



14 Pin TSSOP
Order Number LMV324MT, LMV324MTX, LMV339TM, LMV339MTX, LMV824MT and LMV824MTX
NS Package Number MTC14

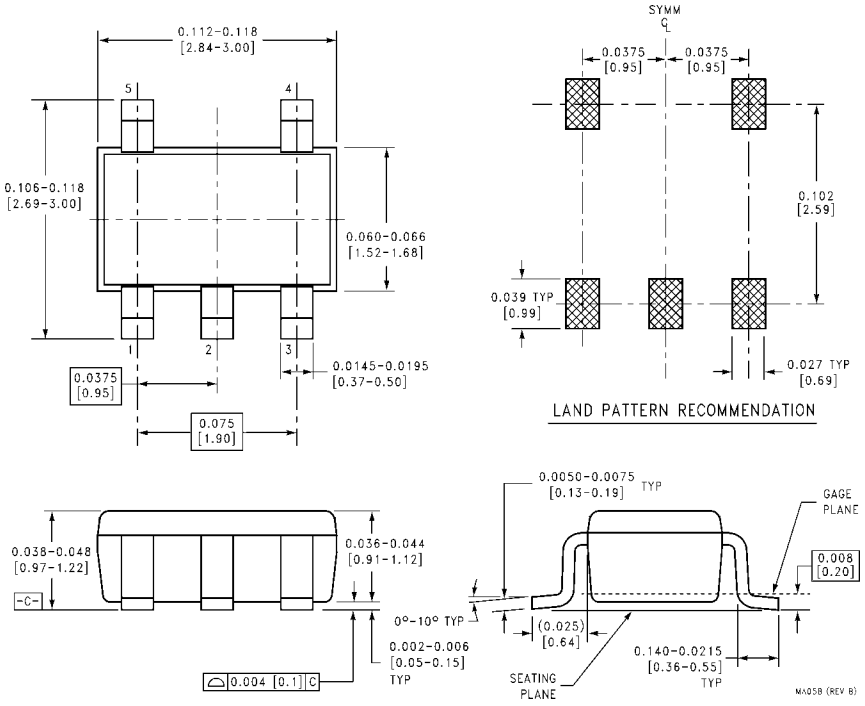


8 Pin Small Outline
Order Number LMV358M, LMV358MX, LMV393M, LMV393MX, LMV822M, and LMV822MX
NS Package Number M08A

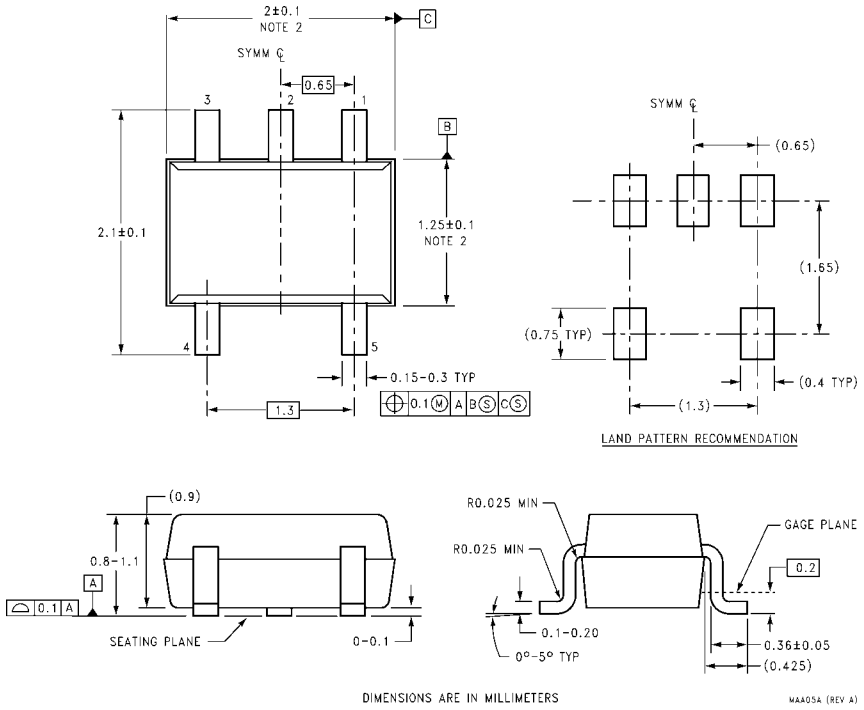


8 Pin MSOP
Order Number LMV358MM, LMV358MMX, LMV393MM, LMV393MMX, LMV822MM and LMV822MMX
NS Package Number MUA08A

4.0 PACKAGING INFORMATION

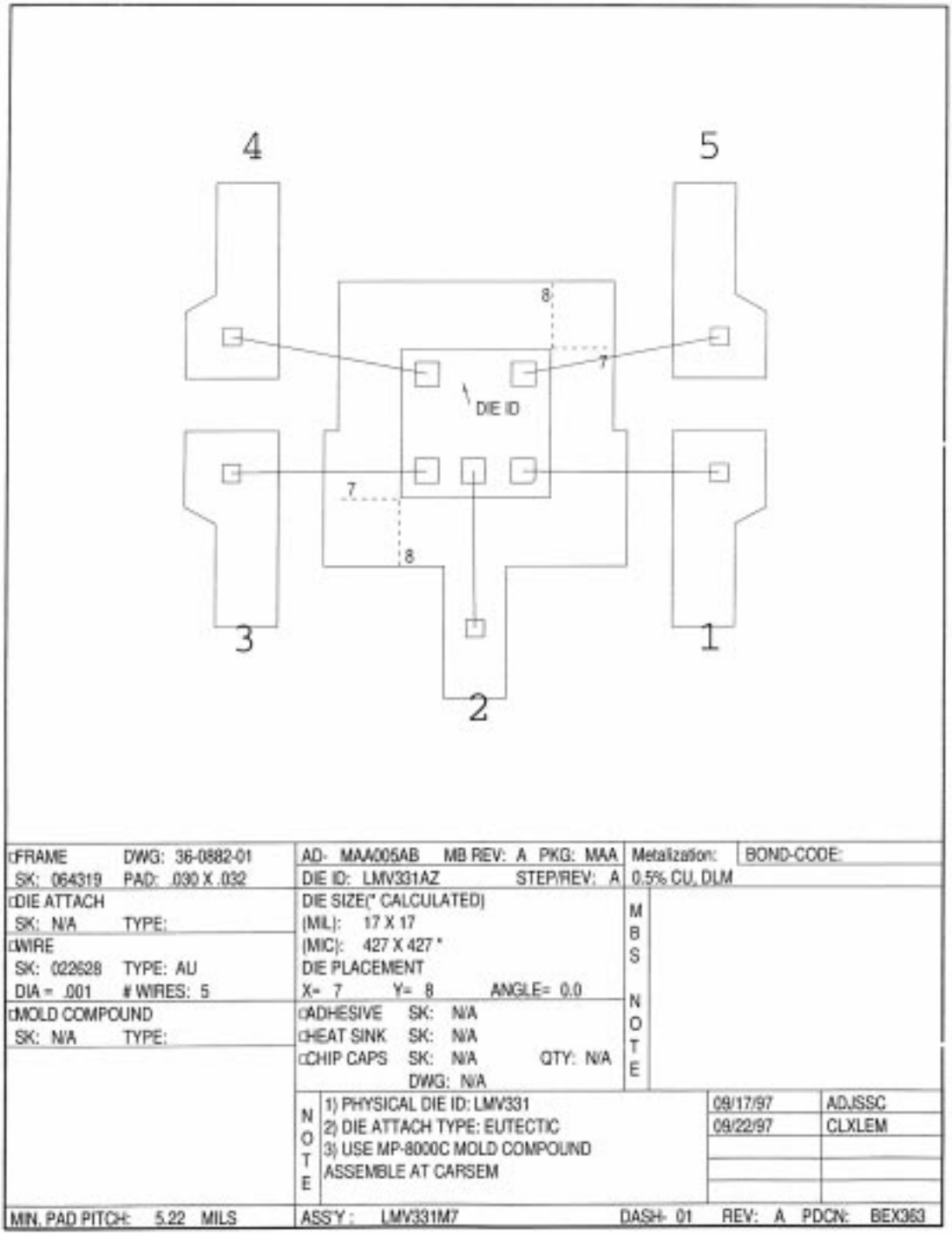


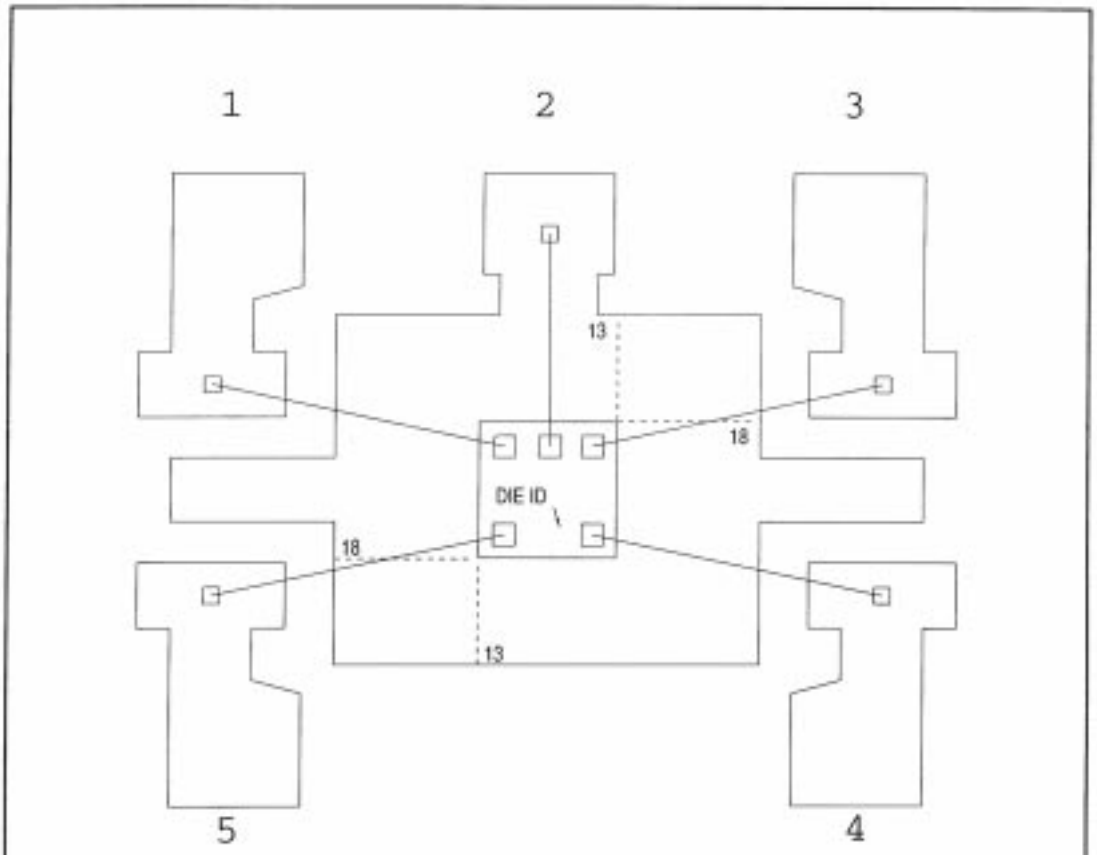
5 Pin SOT23-5 Tape and Reel
Order Number LMV321M5, LMV321M5X, LMV331M5, LMV331M5X, LMV821M5, and LMV821M5X
NS Package Number MA05B



5 Pin SC70-5 Tape and Reel
Order Number LMV321M7, LMV321M7X, LMV331M7, LMV331M7X, LMV821M7, and LMV821M7X
NS Package Number MAA05A

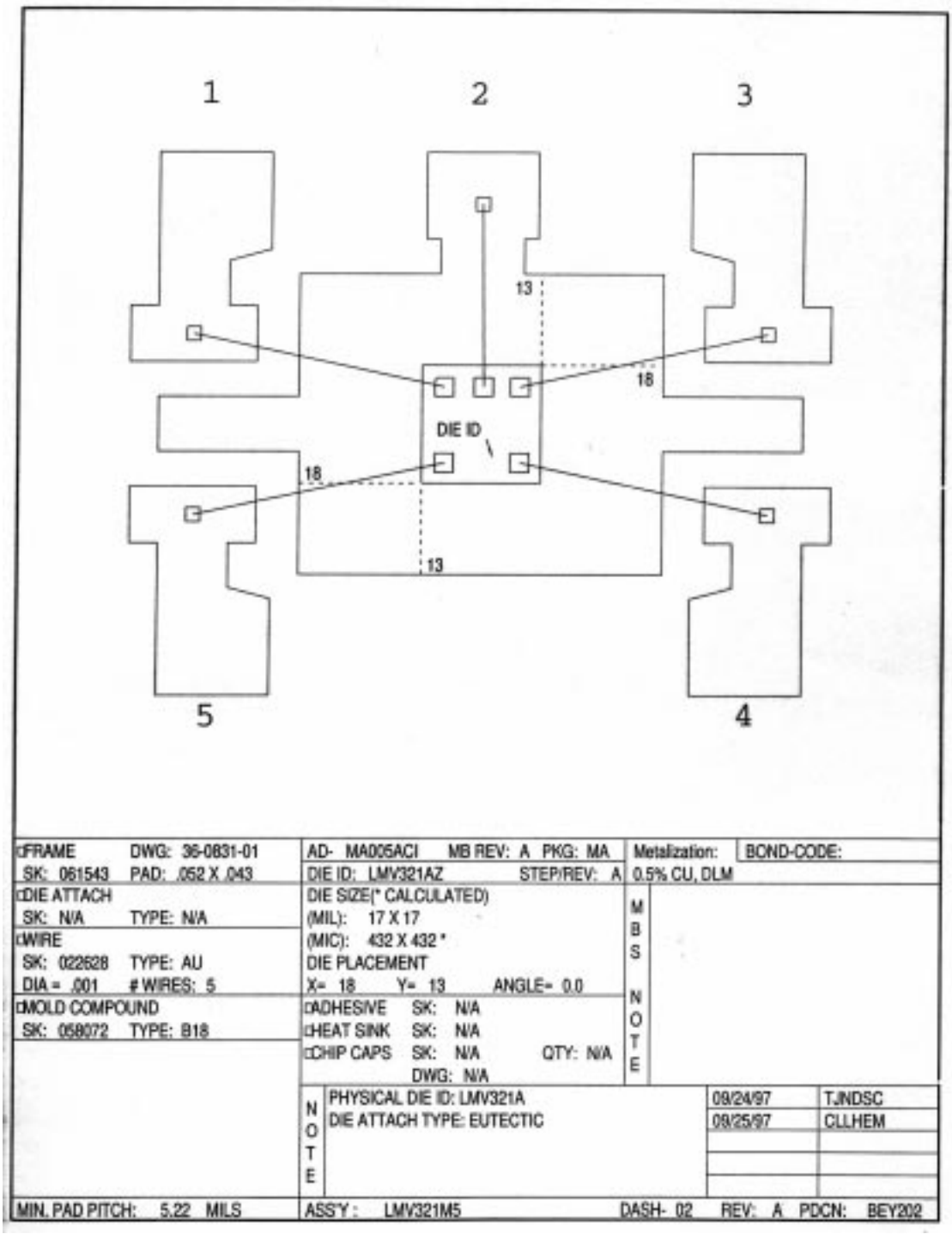
4.2 BONDING DIAGRAMS

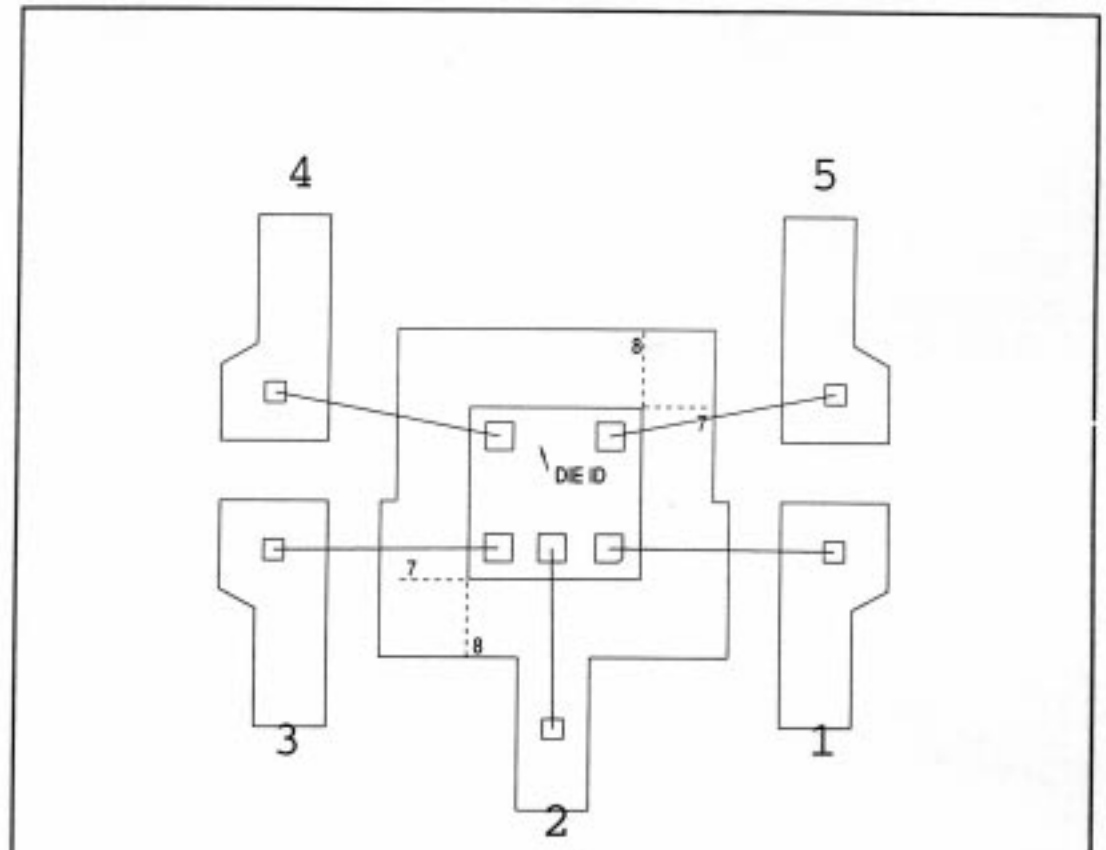




□FRAME SK: 061543	DWG: 36-0831-01 PAD: .052 X .043	AD- MA005ACI DIE ID: LMV331AZ	MB REV: A PKG: MA STEP/REV: A	Metallization: 0.5% CU, DLM	BOND-CODE:
□DIE ATTACH SK: N/A	TYPE: N/A	DIE SIZE(* CALCULATED) (MIL): 17 X 17		MBS NOTE	
□WIRE SK: 022628 DIA = .001	TYPE: AU # WIRES: 5	(MIC): 427 X 427 * DIE PLACEMENT X= 18 Y= 13	ANGLE= 0.0		
□MOLD COMPOUND SK: 058072	TYPE: B18	□ADHESIVE SK: N/A □HEAT SINK SK: N/A □CHIP CAPS SK: N/A DWG: N/A	QTY: N/A		
		NOTE 1) PHYSICAL DIE ID: LMV331 2) DIE ATTACH TYPE: EUTECTIC		09/12/97 ADJSSC 09/23/97 CLLHEM	
MIN. PAD PITCH: 5.22 MILS		ASS'Y : LMV331M5		DASH- 01 REV: A PDCN: BEX362	

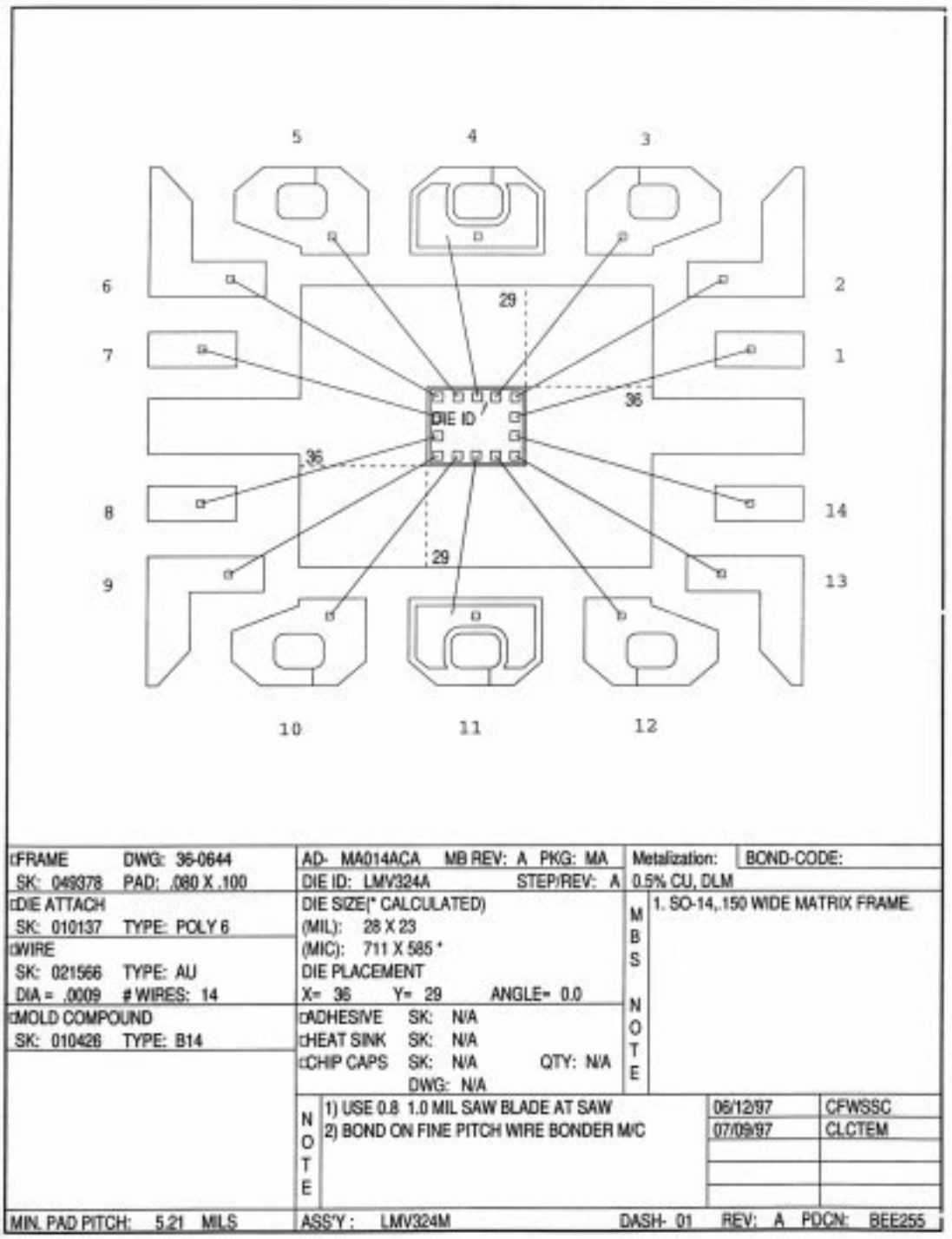
4.0 PACKAGING INFORMATION

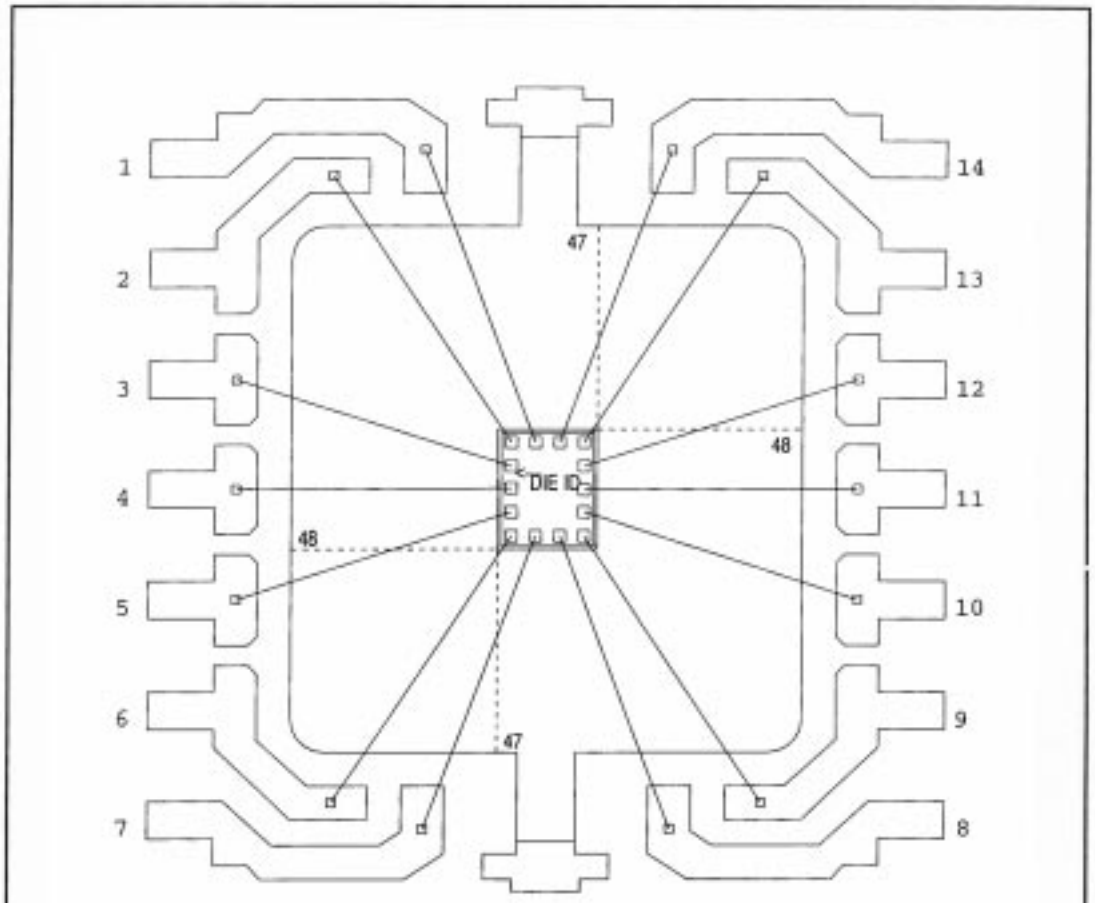




□FRAME DWG: 36-0882-01 SK: 064319 PAD: .030 X .032	AD- MAA005AB MB REV: A PKG: MAA DIE ID: LMV321AZ STEP/REV: A	Metalization: 0.5% CU, DLM	BOND-CODE:
□DIE ATTACH SK: N/A TYPE:	DIE SIZE(* CALCULATED) (MIL): 17 X 17 (MIC): 427 X 427 *	MBS NOTE	
□WIRE SK: 022628 TYPE: AU DIA = .001 # WIRES: 5	DIE PLACEMENT X= 7 Y= 8 ANGLE= 0.0		
□MOLD COMPOUND SK: N/A TYPE:	□ADHESIVE SK: N/A □HEAT SINK SK: N/A □CHIP CAPS SK: N/A QTY: N/A DWG: N/A		
	NOTE 1) PHYSICAL DIE ID: LMV321A 2) DIE ATTACH TYPE: EUTECTIC 3) USE MP-8000C MOLD COMPOUND ASSEMBLE AT CARSEM	09/17/97 TJINDSC 09/18/97 CLXLEM	
MIN. PAD PITCH: 5.22 MILS	ASS'Y: LMV321M7	DASH- 01 REV: A PDCN: BEY313	

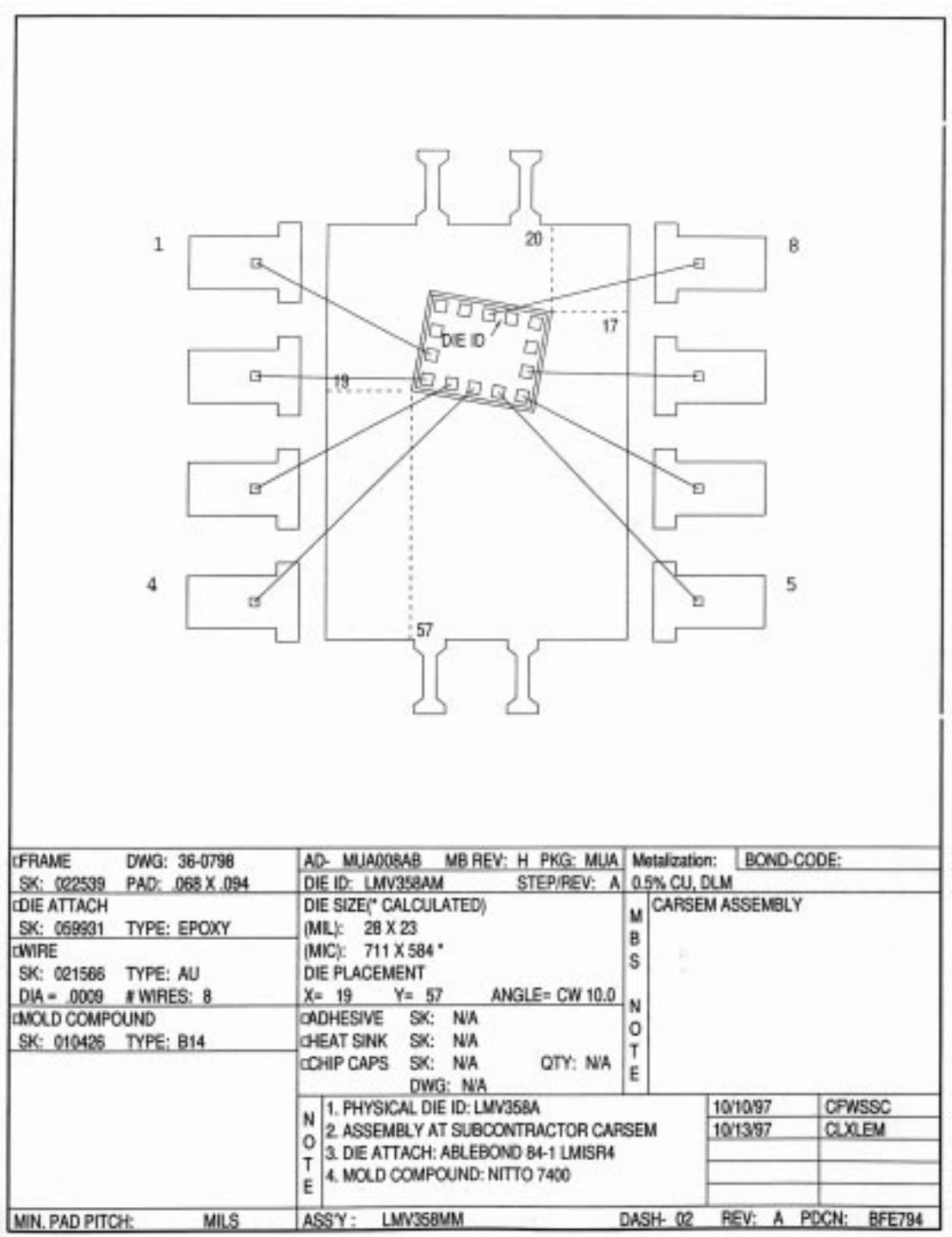
4.0 PACKAGING INFORMATION



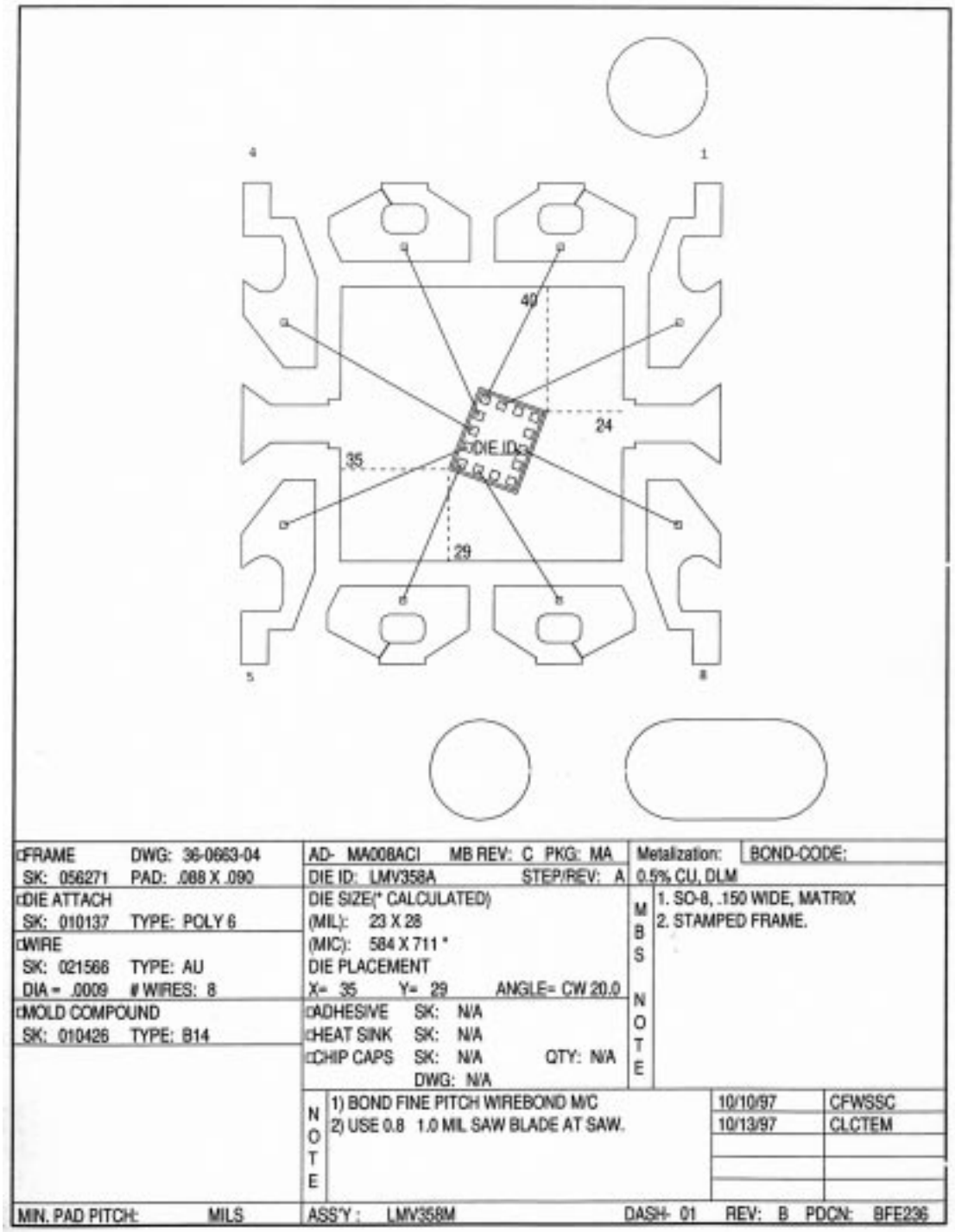


□FRAME DWG: 35283100 SK: 022539 PAD: .118 X .122	AD- MTC014BB MB REV: A PKG: MTC DIE ID: LMV324AMT STEP/REV: A	Metalization: BOND-CODE: 0.5% CU, DLM	
□DIE ATTACH SK: 010137 TYPE: POLY 6	DIE SIZE(* CALCULATED) (MIL): 23 X 28 (MIC): 584 X 711 *	MBS NOTE	1. SUBCONTRACTOR ANAM
□WIRE SK: 021566 TYPE: AU DIA = .0009 # WIRES: 14	DIE PLACEMENT X= 48 Y= 47 ANGLE= 0.0		
□MOLD COMPOUND SK: 050546 TYPE: B26	□ADHESIVE SK: N/A □HEAT SINK SK: N/A □CHIP CAPS SK: N/A QTY: N/A DWG: N/A		
	NOTE PHYSICAL DIE ID: LMV324A BOND PAD SIZE : 2.7 X 2.7 SAW STREET : 2 MILS	09/25/97 CFWSSC 10/13/97 CLXLEM	
MIN. PAD PITCH: 5.21 MILS	ASS'Y : LMV324MT DASH- 01 REV: A PDCN: BFE976		

4.0 PACKAGING INFORMATION

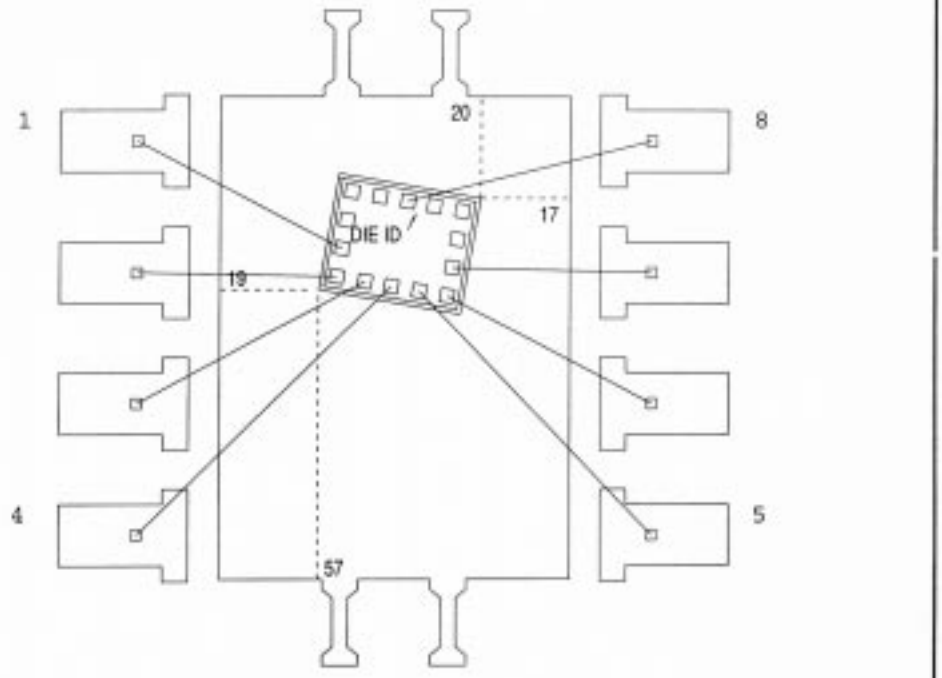


□FRAME DWG: 36-0798 SK: 022539 PAD: .068 X .094	AD- MUA008AB MB REV: H PKG: MUA DIE ID: LMV358AM STEP/REV: A	Metalization: BOND-CODE: 0.5% CU, DLM	
□DIE ATTACH SK: 059931 TYPE: EPOXY	DIE SIZE(* CALCULATED) (MIL): 28 X 23 (MIC): 711 X 584 *	MBS NOTE	CARSEM ASSEMBLY
□WIRE SK: 021566 TYPE: AU DIA = .0009 # WIRES: 8	DIE PLACEMENT X= 19 Y= 57 ANGLE= CW 10.0		
□MOLD COMPOUND SK: 010426 TYPE: B14	□ADHESIVE SK: N/A □HEAT SINK SK: N/A □CHIP CAPS SK: N/A QTY: N/A DWG: N/A		
	NOTE 1. PHYSICAL DIE ID: LMV358A 2. ASSEMBLY AT SUBCONTRACTOR CARSEM 3. DIE ATTACH: ABLEBOND 84-1 LMISR4 4. MOLD COMPOUND: NITTO 7400	10/10/97 CFWSSC 10/13/97 CLXLEM	
MIN. PAD PITCH: MILS	ASS'Y: LMV358MM DASH- 02 REV: A PDCN: BFE794		



□FRAME SK: 056271	DWG: 36-0663-04 PAD: .088 X .090	AD- MA08ACI DIE ID: LMV358A	MB REV: C PKG: MA STEP/REV: A	Metalization: 0.5% CU, DLM	BOND-CODE:
□DIE ATTACH SK: 010137	TYPE: POLY 6	DIE SIZE(* CALCULATED) (MIL): 23 X 28 (MIC): 584 X 711 *		MBS NOTE	1. SO-8, .150 WIDE, MATRIX 2. STAMPED FRAME.
□WIRE SK: 021566 DIA = .0009	TYPE: AU # WIRES: 8	DIE PLACEMENT X= 35 Y= 29	ANGLE= CW 20.0		
□MOLD COMPOUND SK: 010426	TYPE: B14	□ADHESIVE SK: N/A □HEAT SINK SK: N/A □CHIP CAPS SK: N/A DWG: N/A	QTY: N/A		
		NOTE 1) BOND FINE PITCH WIREBOND M/C 2) USE 0.8 1.0 MIL SAW BLADE AT SAW.		10/10/97 10/13/97	CFWSSC CLCTEM
MIN. PAD PITCH: MILS		ASS'Y : LMV358M	DASH- 01	REV: B	PDCN: BFE236

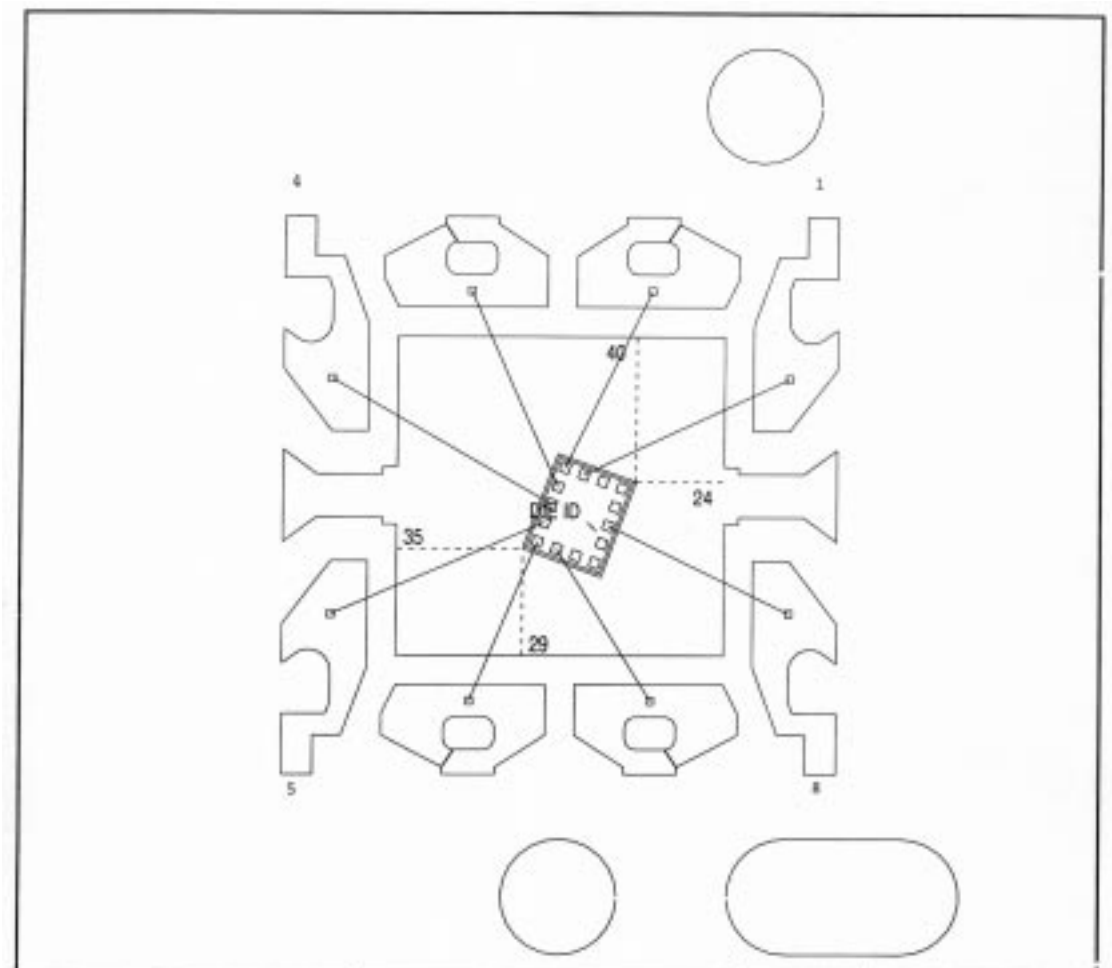
4.0 PACKAGING INFORMATION



□FRAME	DWG: 36-0798	AD- MUA008AB	MB REV: H	PKG: MUA	Metalization: 0.5% CU, DLM	BOND-CODE:
SK: 022539	PAD: .068 X .094	DIE ID: LMV393AM		STEP/REV: A		
□DIE ATTACH		DIE SIZE(* CALCULATED)			MBS NOTE	CARSEM ASSEMBLY
SK: 059931	TYPE: EPOXY	(MIL): 28 X 23				
□WIRE		(MIC): 711 X 584 *				
SK: 021566	TYPE: AU	DIE PLACEMENT				
DIA = .0009	# WIRES: 8	X= 19	Y= 57	ANGLE= CW 10.0		
□MOLD COMPOUND		□ADHESIVE	SK: N/A			
SK: 010426	TYPE: B14	□HEAT SINK	SK: N/A			
		□CHIP CAPS	SK: N/A	QTY: N/A		
			DWG: N/A			

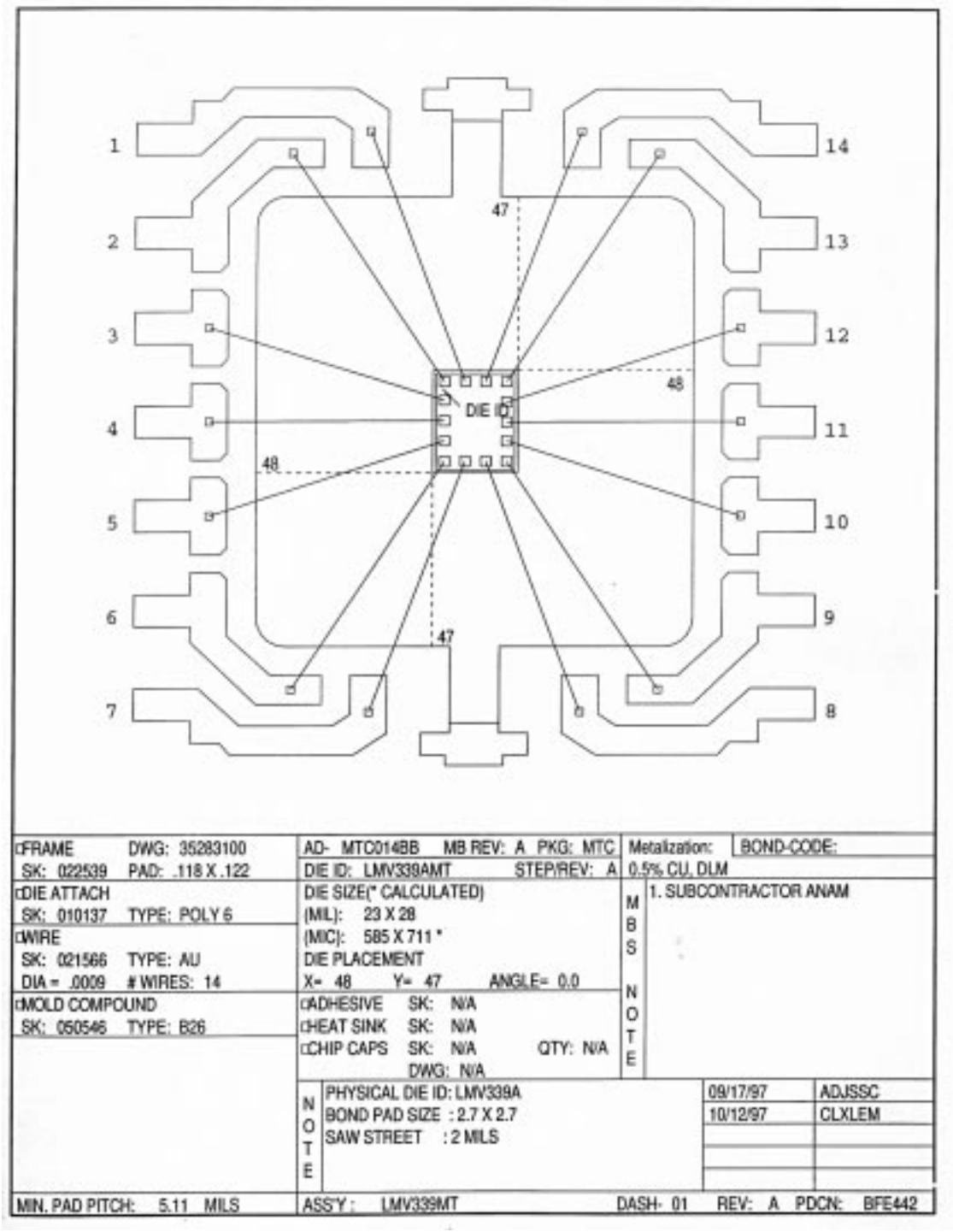
NOTE			
	1. PHYSICAL DIE ID: LMV393	10/14/97	ADJSSC
	2. ASSEMBLY AT SUBCONTRACTOR CARSEM	10/16/97	CLXLEM
	3. DIE ATTACH: ABLEBOND 84-1 LMISR4		
	4. MOLD COMPOUND: NITTO 7400		

MIN. PAD PITCH:	MILS	ASS'Y : LMV393MM	DASH- 02	REV: A	PDCN: BFF396

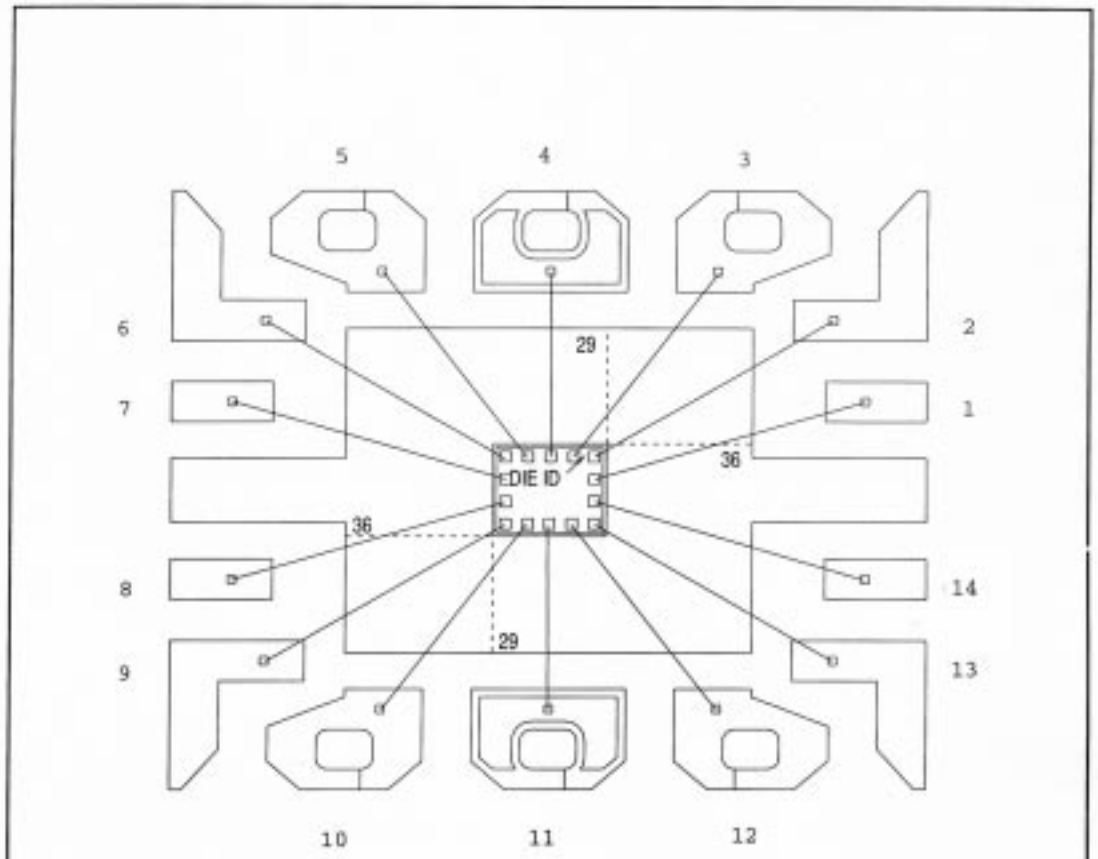


□FRAME SK: 056271	DWG: 36-0663-04 PAD: .088 X .090	AD- MA008ACI MB REV: C PKG: MA		Metalization: 0.5% CU, DLM	BOND-CODE:
		DIE ID: LMV393A	STEP/REV: A		
□DIE ATTACH SK: 010137	TYPE: POLY 6	DIE SIZE(" CALCULATED) (MIL): 23 X 28 (MIC): 584 X 711 *		MBS NOTE	1. SO-8, .150 WIDE, MATRIX 2. STAMPED FRAME.
□WIRE SK: 021566	TYPE: AU	DIE PLACEMENT			
DIA = .0009	# WIRES: 8	X= 35 Y= 29	ANGLE= CW 20.0		
□MOLD COMPOUND SK: 010426	TYPE: B14	□ADHESIVE SK: N/A			
		□HEAT SINK SK: N/A			
		□CHIP CAPS SK: N/A	QTY: N/A		
		DWG: N/A			
		NOTE 1) BOND FINE PITCH WIREBOND M/C		10/10/97	ADJSSC
		2) USE 0.8 1.0 MIL SAW BLADE AT SAW.		10/13/97	CLCTEM
		3) PHYSICAL DIE ID: LMV393			
		4) " FOR ENGINEERING USE ONLY "			
MIN. PAD PITCH:	MILS	ASS'Y : LMV393M	DASH- 01	REV: B	PDCN: BFE234

4.0 PACKAGING INFORMATION

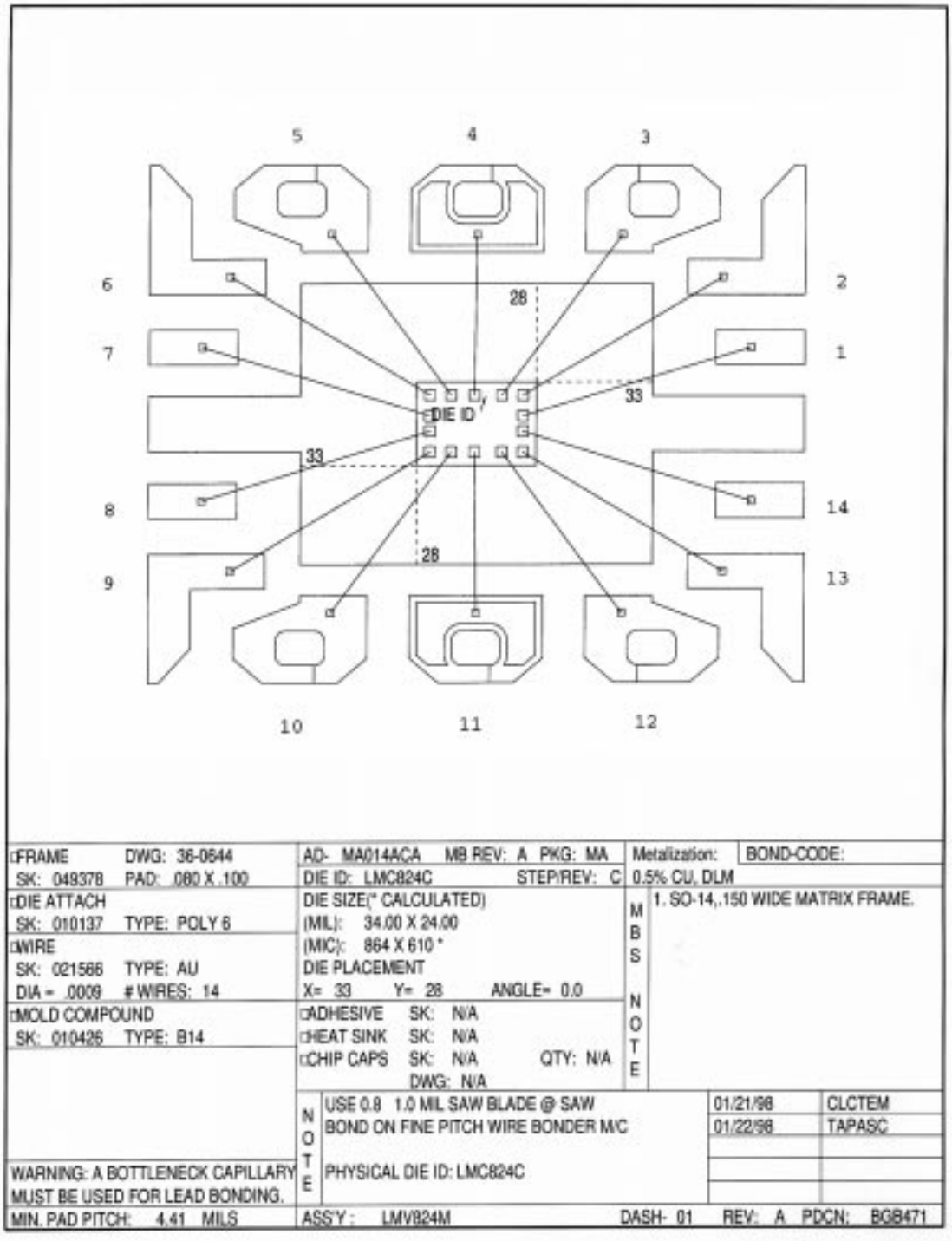


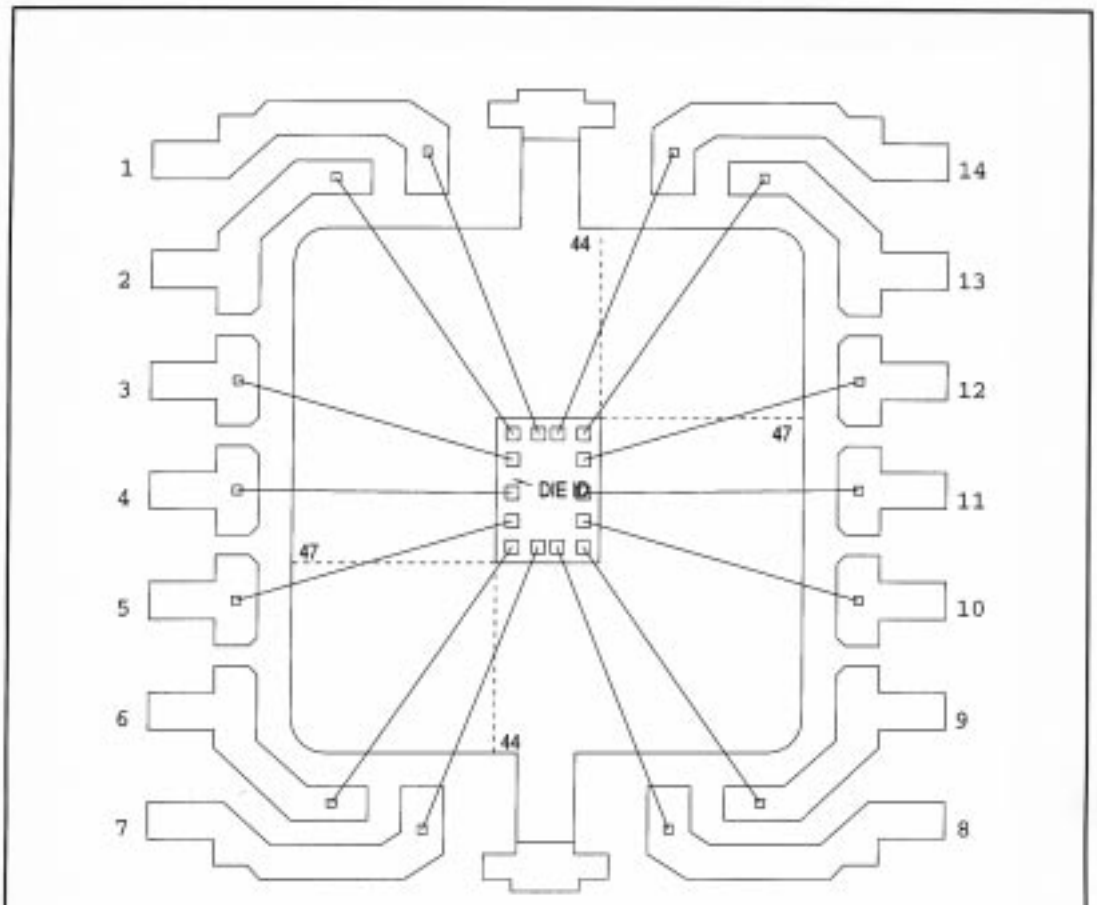
□FRAME DWG: 35283100 SK: 022539 PAD: .118 X .122	AD- MTC014BB MB REV: A PKG: MTC DIE ID: LMV339AMT STEP/REV: A	Metalization: 0.5% CU, DLM	BOND-CODE:
□DIE ATTACH SK: 010137 TYPE: POLY 6	DIE SIZE(* CALCULATED) (MIL): 23 X 28 (MIC): 585 X 711 *	MBS NOTE	1. SUBCONTRACTOR ANAM
□WIRE SK: 021566 TYPE: AU DIA = .0009 # WIRES: 14	DIE PLACEMENT X= 48 Y= 47 ANGLE= 0.0		
□MOLD COMPOUND SK: 050546 TYPE: B26	□ADHESIVE SK: N/A □HEAT SINK SK: N/A □CHIP CAPS SK: N/A QTY: N/A DWG: N/A		
	NOTE: PHYSICAL DIE ID: LMV339A BOND PAD SIZE : 2.7 X 2.7 SAW STREET : 2 MILS	09/17/97 10/12/97	ADJSSC CLXLEM
MIN. PAD PITCH: 5.11 MILS	ASS'Y : LMV339MT DASH- 01 REV: A PDCN: BFE442		



□FRAME DWG: 36-0644 SK: 049378 PAD: .080 X .100	AD- MA014ACA MB REV: A PKG: MA DIE ID: LMV339A STEP/REV: A	Metalization: BOND-CODE: 0.5% CU, DLM	
□DIE ATTACH SK: 010137 TYPE: POLY 6	DIE SIZE(* CALCULATED) (MIL): 28 X 29 (MIC): 711 X 585 *	MBS NOTE	1. SO-14,.150 WIDE MATRIX FRAME.
□WIRE SK: 021566 TYPE: AU DIA = .0009 # WIRES: 14	DIE PLACEMENT X= 36 Y= 29 ANGLE= 0.0		
□MOLD COMPOUND SK: 010426 TYPE: B14	□ADHESIVE SK: N/A □HEAT SINK SK: N/A □CHIP CAPS SK: N/A QTY: N/A DWG: N/A		
	NOTE 1) USE 0.8 1.0 MIL SAW BLADE AT SAW. 2) BOND ON FINE PITCH WIRE BONDER M/C 3) FOR ENGINEERING USED ONLY	09/17/97 ADJSSC 09/19/97 CLCTEM	
MIN. PAD PITCH: 5.11 MILS	ASS'Y : LMV339M DASH- 01 REV: A PDCN: BEW969		

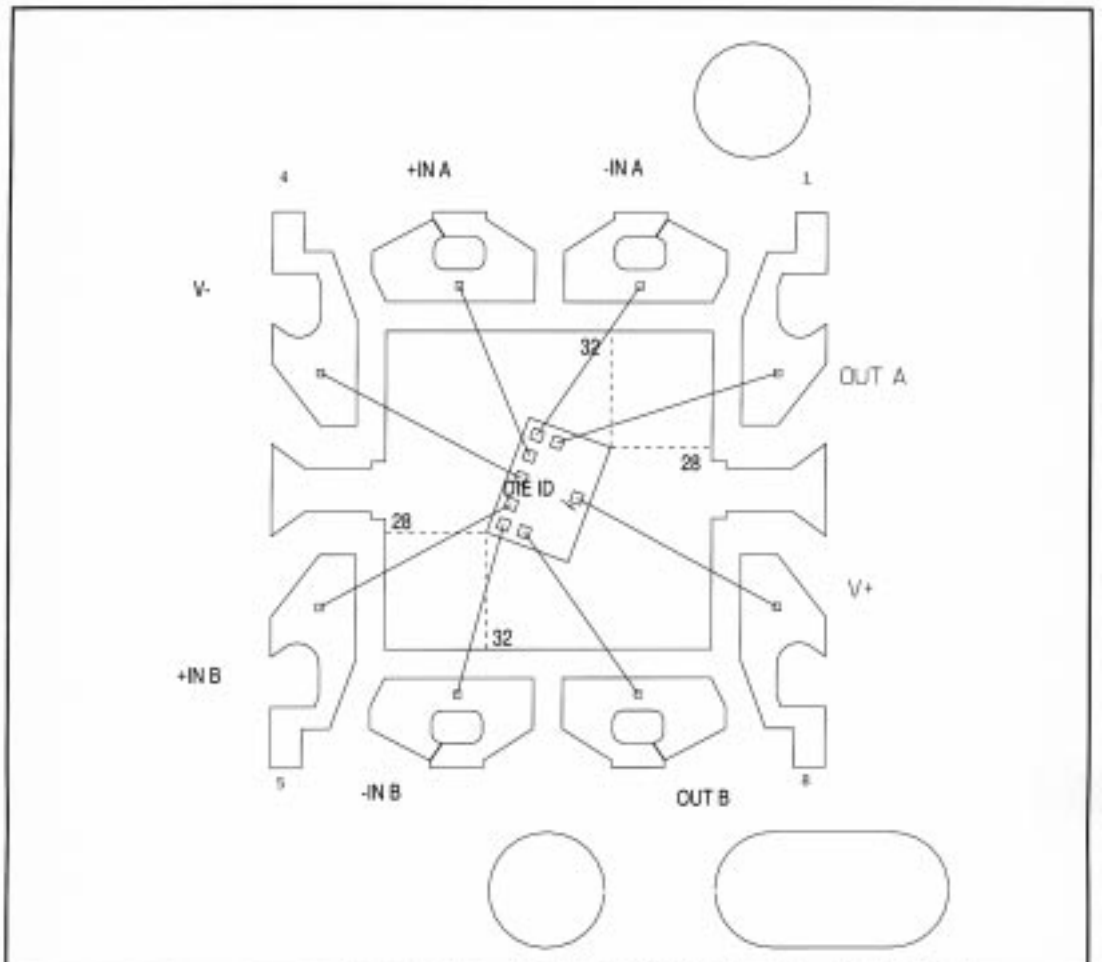
4.0 PACKAGING INFORMATION



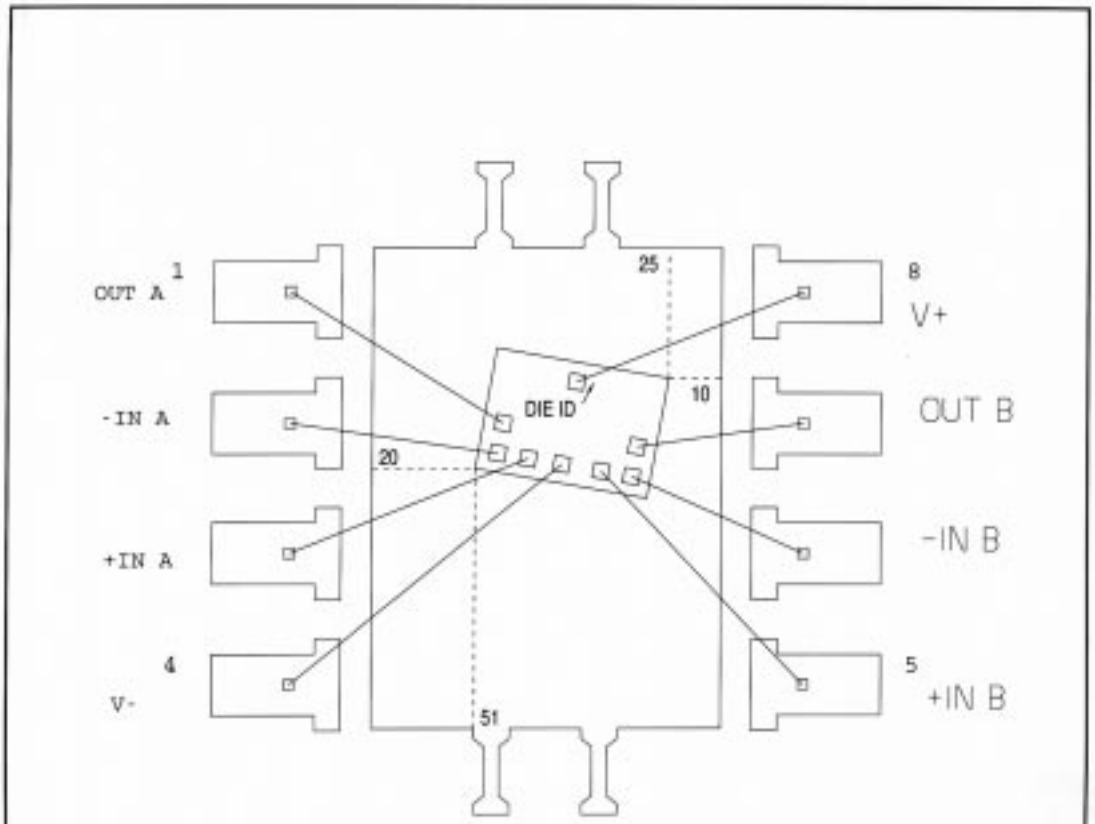


□FRAME SK: 022539	DWG: 35283100 PAD: .118 X .122	AD- MTC014BB MB REV: A PKG: MTC		Metalization: 0.5% CU, DLM	BOND-CODE:
		DIE ID: LMC824CMT	STEP/REV: C		
□DIE ATTACH SK: 010137	TYPE: POLY 6	DIE SIZE(* CALCULATED) (MIL): 24.00 X 34.00 (MIC): 610 X 864 *		MBS NOTE	1. SUBCONTRACTOR ANAM
□WIRE SK: 021566 DIA = .0009	TYPE: AU # WIRES: 14	DIE PLACEMENT X= 47 Y= 44 ANGLE= 0.0			
□MOLD COMPOUND SK: 050546	TYPE: B26	□ADHESIVE SK: N/A			
		□HEAT SINK SK: N/A			
		□CHIP CAPS SK: N/A DWG: N/A	QTY: N/A		
		NOTE PHYSICAL DIE ID: LMC824C		10/15/97	CLXLEM
		BOND PAD SIZE:3.1 X 3.1		10/15/97	CLXLEM
		SAW STREET :3 MILS		10/16/97	CKHPSC
WARNING: A BOTTLENECK CAPILLARY MUST BE USED FOR LEAD BONDING.					
MIN. PAD PITCH: 4.41 MILS		ASS'Y : LMC824MTC	DASH- 02	REV: A	PDCN: BFF822

4.0 PACKAGING INFORMATION

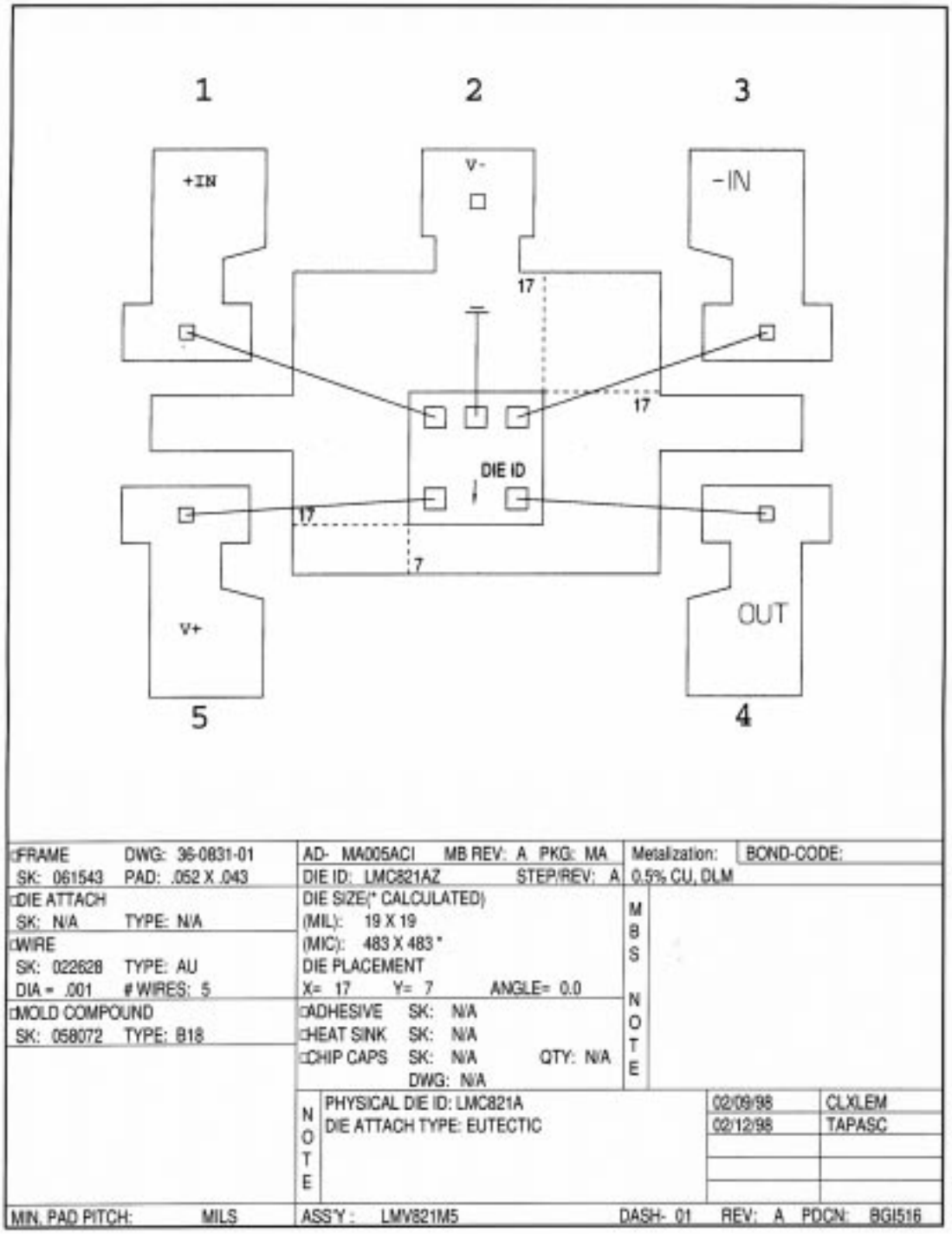


□FRAME SK: 056271	DWG: 36-0663-04 PAD: .088 X .090	AD- MA008ACI DIE ID: LMC822C	MB REV: C PKG: MA STEP/REV: C	Metalization: 0.5% CU, DLM	BOND-CODE:
□DIE ATTACH SK: 010137	TYPE: POLY 6	DIE SIZE(* CALCULATED) (MIL): 24.00 X 34.00 (MIC): 610 X 864 * DIE PLACEMENT X= 28 Y= 32 ANGLE= CW 20.0		MBS NOTE	1. SO-8, .150 WIDE, MATRIX 2. STAMPED FRAME.
□WIRE SK: 021566 DIA = .0009	TYPE: AU # WIRES: 8				
□MOLD COMPOUND SK: 010426	TYPE: B14	□ADHESIVE SK: N/A □HEAT SINK SK: N/A □CHIP CAPS SK: N/A DWG: N/A	QTY: N/A		
		NOTE: USE 0.8 1.0 MIL SAW BLADE AT SAW BOND FINE PITCH WIREBOND M/C PHYSICAL DIE ID: LMC822C		01/21/98 CLCTEM 01/22/98 TAPASC	
MIN. PAD PITCH: 6.01 MILS		ASS'Y : LMV822M	DASH- 01	REV: A	PDCN: BGB467

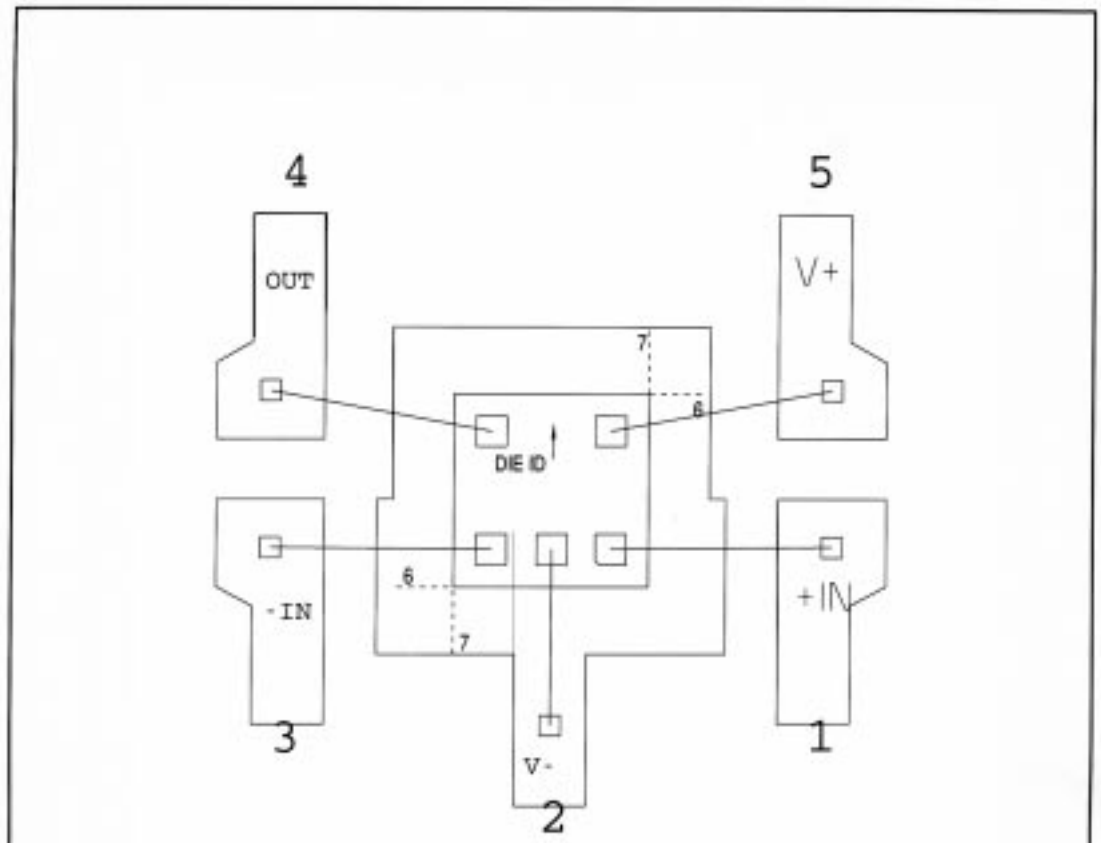


□FRAME SK: 022539	DWG: 36-0798 PAD: .068 X .094	AD- MUA008AB MB REV: H PKG: MUA		Metalization: 0.5% CU, DLM	BOND-CODE:
		DIE ID: LMC822CM	STEP/REV: C		
□DIE ATTACH SK: 010137	TYPE: POLY 6	DIE SIZE(* CALCULATED)		MBS NOTE	CARSEM ASSEMBLY
		(MIL): 34.0 X 24.0			
□WIRE SK: 021566	TYPE: AU	(MIC): 864 X 610 *			
		DIE PLACEMENT			
DIA = .0009	# WIRES: 8	X= 20 Y= 51	ANGLE= CW 10.0		
□MOLD COMPOUND SK: 010426	TYPE: B14	□ADHESIVE SK: N/A			
		□HEAT SINK SK: N/A			
		□CHIP CAPS SK: N/A	QTY: N/A		
		DWG: N/A			
		NOTE: PHYSICAL DIE ID: LMC822C		02/09/98	CLXLEM
		SUBCONTRACTOR ASSEMBLY		02/12/98	TAPASC
		DIE ATTACH: ABLEBOND 84-1 LMISR4			
		MOLD COMPOUND: NITTO 7400			
MIN. PAD PITCH:	MILS	ASS'Y: LMV822MM	DASH- 01	REV: A	PDCN: BGI517

4.0 PACKAGING INFORMATION



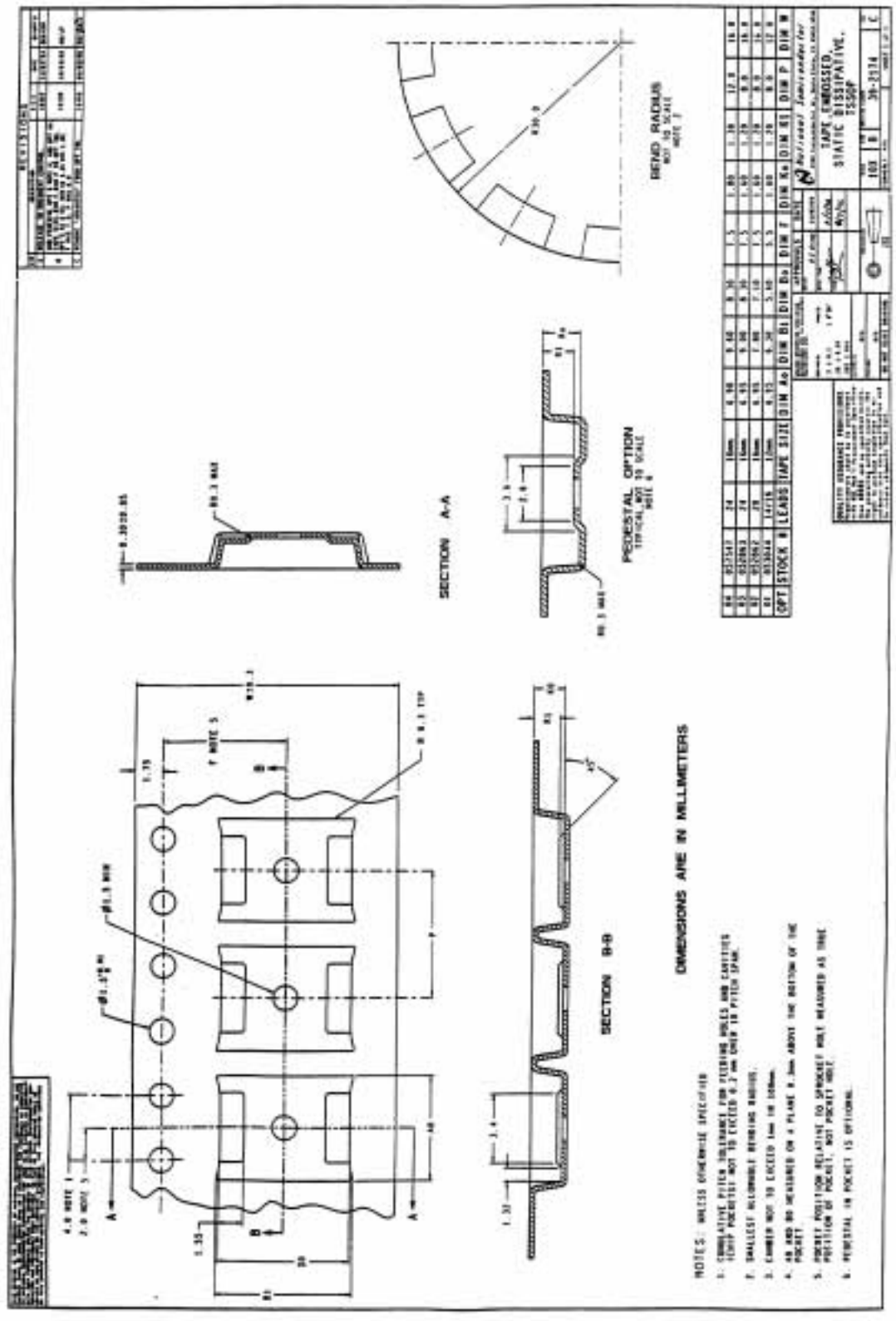
□FRAME SK: 061543	DWG: 36-0831-01 PAD: .052 X .043	AD- MA005ACI MB REV: A PKG: MA DIE ID: LMC821AZ STEP/REV: A	Metalization: 0.5% CU, DLM	BOND-CODE:
□DIE ATTACH SK: N/A	TYPE: N/A	DIE SIZE(* CALCULATED) (MIL): 19 X 19 (MIC): 483 X 483 *	MBS NOTE	
□WIRE SK: 022628 DIA = .001	TYPE: AU # WIRES: 5	DIE PLACEMENT X= 17 Y= 7 ANGLE= 0.0		
□MOLD COMPOUND SK: 058072	TYPE: B18	□ADHESIVE SK: N/A □HEAT SINK SK: N/A □CHIP CAPS SK: N/A QTY: N/A DWG: N/A		
		NOTE: PHYSICAL DIE ID: LMC821A DIE ATTACH TYPE: EUTECTIC	02/09/98 02/12/98	CLXLEM TAPASC
MIN. PAD PITCH: MILS		ASS'Y : LMV821M5	DASH- 01 REV: A	PDCN: BGI516



□FRAME DWG: 36-0682-01 SK: 064319 PAD: .030 X .032	AD- MAA005AB MB REV: A PKG: MAA DIE ID: LMC821AZ STEP/REV: A	Metalization: 0.5% CU, DLM	BOND-CODE:
□DIE ATTACH SK: N/A TYPE: N/A	DIE SIZE(* CALCULATED) (MIL): 19 X 19 (MIC): 483 X 483 *	MBS NOTE	
□WIRE SK: 021566 TYPE: AU DIA = .001 # WIRES: 5	DIE PLACEMENT X= 6 Y= 7 ANGLE= 0.0		
□MOLD COMPOUND SK: N/A TYPE: N/A	□ADHESIVE SK: N/A □HEAT SINK SK: N/A □CHIP CAPS SK: N/A QTY: N/A DWG: N/A		
	NOTE: PHYSICAL DIE ID: LMC821A DIE ATTACH TYPE: EUTECTIC USE MP-8000CMOLD COMPOUND ASSEMBLE AT CARSEM	02/09/98 CLXLEM 02/12/98 TAPASC	
MIN. PAD PITCH: 5.74 MILS	ASS'Y: LMV821M7	DASH- 01 REV: A PDCN: BGI515	

4.3 TAPE AND REEL DIAGRAMS

For 14 lead TSSOP look at dimensions in table for OPT01 (STOCK #053044)


SECTION A-A
SECTION B-B
PEDESTAL OPTION
BEND RADIUS
DIMENSIONS ARE IN MILLIMETERS
NOTES:
TAPE EMBOSSED
STATIC DISSIPATIVE

4.0 PACKAGING INFORMATION

For 8 lead SOIC look at dimensions in table for OPT01 (STOCK #025349)
For 14 lead SOIC look at dimensions in table for OPT02 (STOCK #025350)
For 8 lead MSOP look at dimensions in table for OPT17 (STOCK #060860)

OPT	STOCK #	PKG TYPE	TAPE	DIM A	DIM Ao	DIM B	DIM Bo	DIM C	DIM Co	DIM D	DIM Do	DIM L	DIM F	DIM F'	DIM Go	DIM H	DIM Ho	DIM Ko	DIM K1	DIM P1	DIM W
17	[illegible]	[illegible]	12mm	.213 (5.4)	.209 (5.3)	.138 (3.5)	.134 (3.4)	N/A	N/A	N/A	N/A	N/A	.217 (5.5)	N/A	N/A	N/A	N/A	.055 (1.4)	N/A	.315 (8)	.472 (12)
16	[illegible]	SO-16N	16mm	.262 (6.65)	.256 (6.5)	.411 (10.45)	.406 (10.3)	.172 (4.3)	.138 (3.5)	.090 (2.3)	.051 (1.3)	.260 (6.6)	.295 (7.5)	N/A	N/A	N/A	N/A	.091 (2.3)	.071 (1.8)	.315 (8)	.630 (16)
15	[illegible]	SO-14N	16mm	.262 (6.65)	.256 (6.5)	.380 (9.65)	.374 (9.5)	.172 (4.3)	.138 (3.5)	.090 (2.3)	.051 (1.3)	.260 (6.6)	.295 (7.5)	N/A	N/A	N/A	N/A	.091 (2.3)	.071 (1.8)	.315 (8)	.630 (16)
14	[illegible]	SO-08N	12mm	.276 (7.05)	.272 (6.9)	.219 (5.55)	.213 (5.4)	N/A	N/A	N/A	N/A	N/A	.217 (5.5)	N/A	N/A	N/A	N/A	.079 (2)	.067 (1.7)	.315 (8)	.472 (12)
13	[illegible]	SO-28W	24mm	.435 (11.05)	.429 (10.9)	.726 (18.45)	.720 (18.3)	.285 (7.2)	.244 (6.2)	.126 (3.2)	.087 (2.2)	.543 (13.8)	.453 (11.5)	N/A	N/A	N/A	N/A	.126 (3.2)	.106 (2.7)	.472 (12)	.945 (24)
12	[illegible]	SO-24W	24mm	.431 (10.95)	.425 (10.8)	.632 (16.05)	.626 (15.9)	N/A	N/A	N/A	N/A	N/A	.453 (11.5)	.307 (7.8)	.276 (7)	.175 (4.45)	.159 (4.05)	.126 (3.2)	.110 (2.8)	.472 (12)	.945 (24)
11	[illegible]	SO-20W	24mm	.441 (11.2)	.429 (10.9)	.535 (13.6)	.524 (13.3)	N/A	N/A	N/A	N/A	N/A	.453 (11.5)	.323 (8.2)	.276 (7)	.142 (3.6)	.118 (3)	.126 (3.2)	.106 (2.7)	.472 (12)	.945 (24)
10	[illegible]	SO-16W	16mm	.435 (11.05)	.429 (10.9)	.429 (10.9)	.421 (10.7)	.283 (7.2)	.244 (6.2)	.098 (2.5)	.059 (1.5)	.354 (9)	.295 (7.5)	N/A	N/A	N/A	N/A	.126 (3.2)	.106 (2.7)	.472 (12)	.630 (16)
09	[illegible]	SO-14W	16mm	.435 (11.05)	.429 (10.9)	.380 (9.65)	.374 (9.5)	.283 (7.2)	.244 (6.2)	.098 (2.5)	.059 (1.5)	.307 (7.8)	.295 (7.5)	N/A	N/A	N/A	N/A	.126 (3.2)	.106 (2.7)	.472 (12)	.630 (16)
08	[illegible]	SO-28W	24mm	.431 (10.95)	.429 (10.9)	.726 (18.45)	.720 (18.3)	N/A	N/A	N/A	N/A	N/A	.453 (11.5)	N/A	N/A	N/A	N/A	.118 (3)	N/A	.472 (12)	.945 (24)
07	[illegible]	SO-24W	24mm	.435 (11.05)	.429 (10.9)	.630 (16)	.626 (15.9)	N/A	N/A	N/A	N/A	N/A	.453 (11.5)	N/A	N/A	N/A	N/A	.126 (3.2)	N/A	.472 (12)	.945 (24)
06	[illegible]	SO-20W	24mm	.435 (11.05)	.429 (10.9)	.530 (13.45)	.524 (13.3)	N/A	N/A	N/A	N/A	N/A	.453 (11.5)	N/A	N/A	N/A	N/A	.118 (3)	N/A	.472 (12)	.945 (24)
05	[illegible]	SO-16W	16mm	.435 (11.05)	.429 (10.9)	.430 (10.95)	.421 (10.7)	N/A	N/A	N/A	N/A	N/A	.295 (7.5)	N/A	N/A	N/A	N/A	.118 (3)	N/A	.472 (12)	.630 (16)
04	[illegible]	SO-14W	16mm	.435 (11.05)	.429 (10.9)	.380 (9.65)	.374 (9.5)	N/A	N/A	N/A	N/A	N/A	.295 (7.5)	N/A	N/A	N/A	N/A	.118 (3)	N/A	.472 (12)	.630 (16)
03	[illegible]	SO-16N	16mm	.262 (6.65)	.256 (6.5)	.411 (10.45)	.406 (10.3)	N/A	N/A	N/A	N/A	N/A	.295 (7.5)	N/A	N/A	N/A	N/A	.083 (2.1)	N/A	.315 (8)	.630 (16)
02	[illegible]	SO-14N	16mm	.262 (6.65)	.256 (6.5)	.380 (9.65)	.374 (9.5)	N/A	N/A	N/A	N/A	N/A	.295 (7.5)	N/A	N/A	N/A	N/A	.083 (2.1)	N/A	.315 (8)	.630 (16)
01	[illegible]	SO-08N	12mm	.244 (6.2)	.256 (6.5)	.213 (5.4)	.209 (5.3)	N/A	N/A	N/A	N/A	N/A	.217 (5.5)	N/A	N/A	N/A	N/A	.083 (2.1)	N/A	.315 (8)	.472 (12)

DESIGN A

NOTES: UNLESS OTHERWISE SPECIFIED

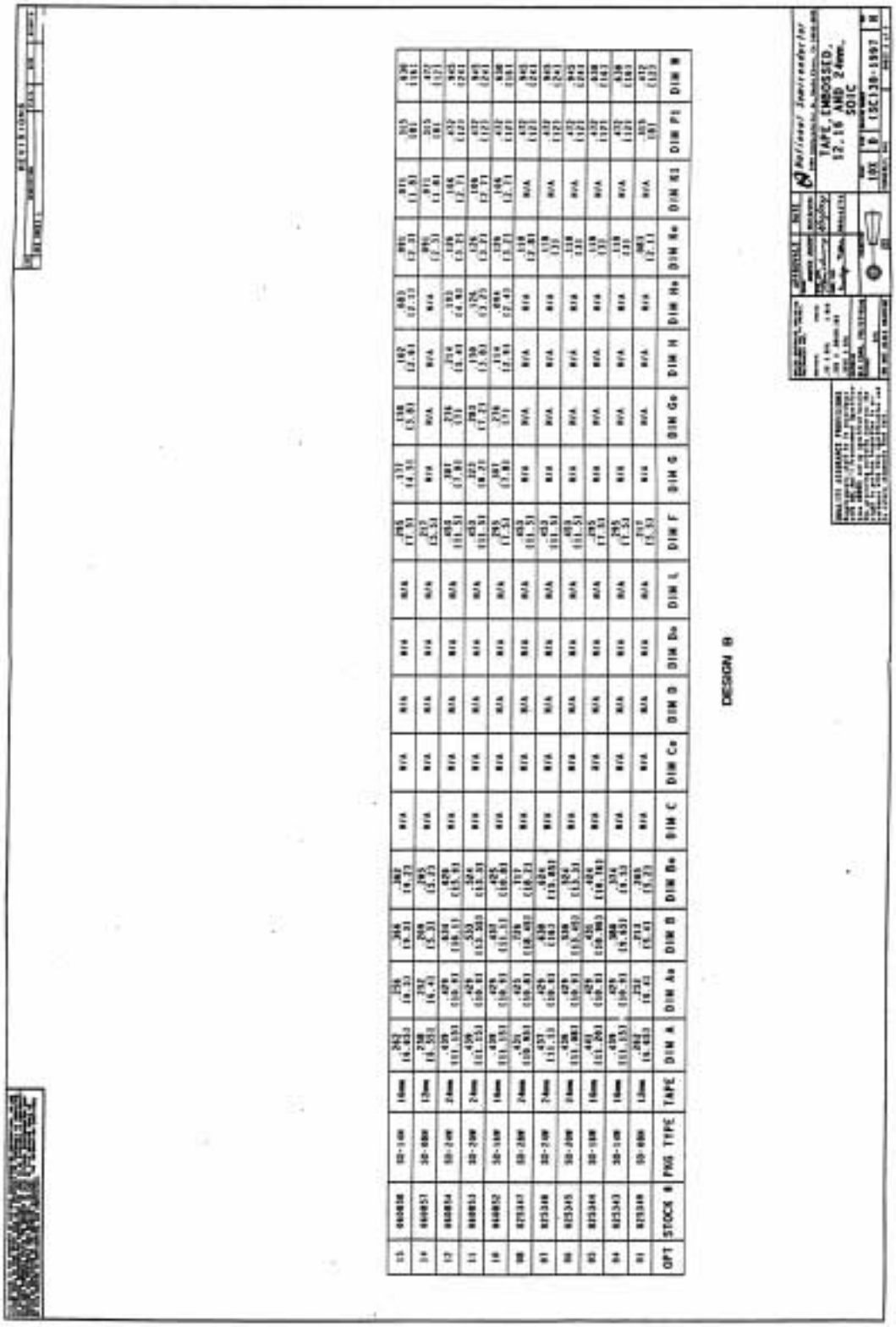
1. CUMMULATIVE PITCH TOLERANCE FOR FEEDING HOLES AND CAVITIES (CHIP POCKETS) NOT TO EXCEED .008(0.20) OVER 10 PITCH SPAN.
2. SMALLEST ALLOWABLE BENDING RADIUS.
3. THRU HOLE INSIDE CAVITY IS CENTERED WITHIN CAVITY.
4. TOLERANCE IS [illegible] FOR THESE DIMENSIONS ON ALL 12mm TAPES.
5. Ao AND Bo MEASURED ON A PLANE [illegible] ABOVE THE BOTTOM OF THE POCKET.
6. Ko MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER.
7. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
8. CONTROLLING DIMENSION IS MILLIMETER, DIMENSIONS IN INCHES ROUNDED.

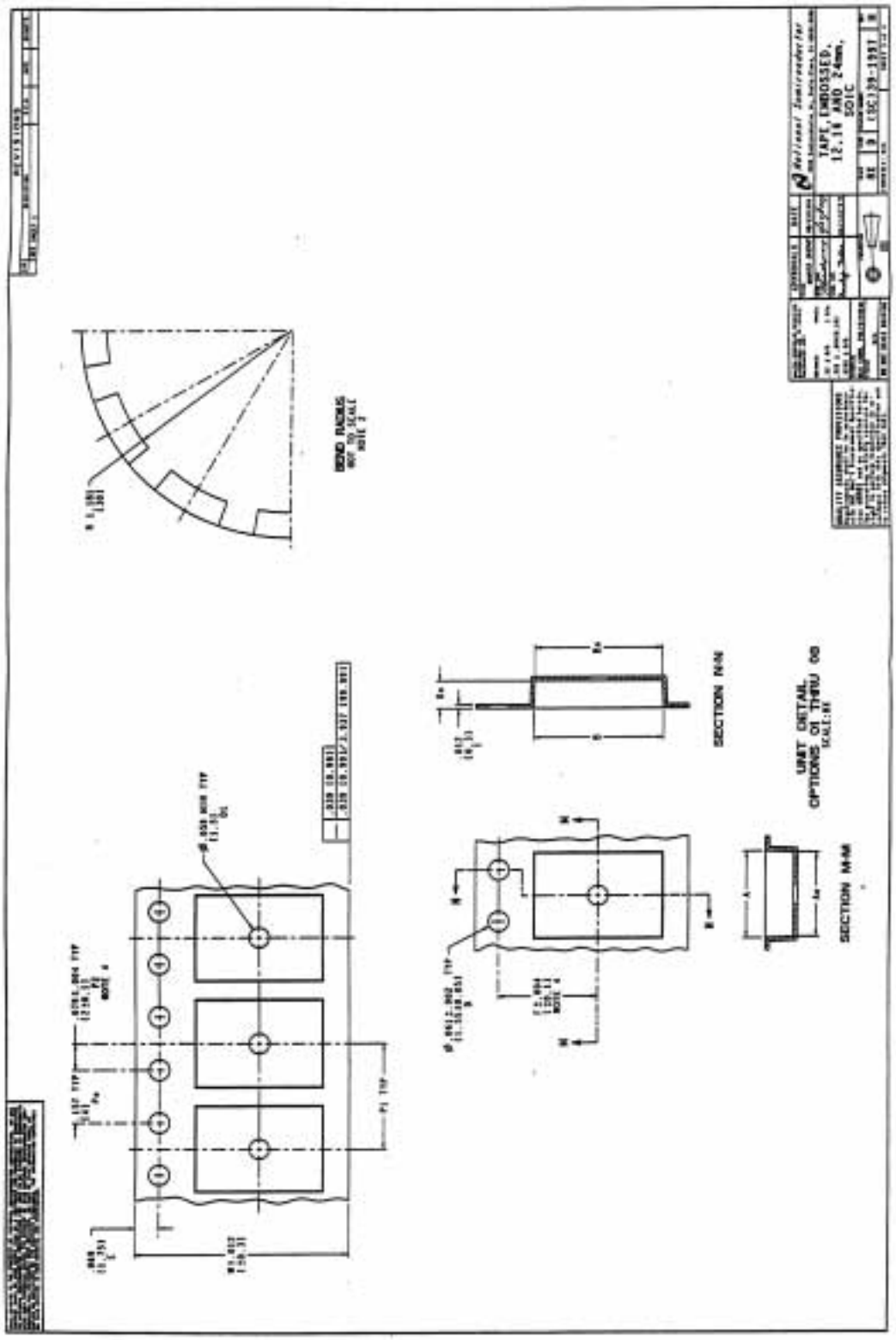
National Semiconductor

TAPE, EMBOSSED, 12,16 AND 24mm, SOIC

TDC136-1997

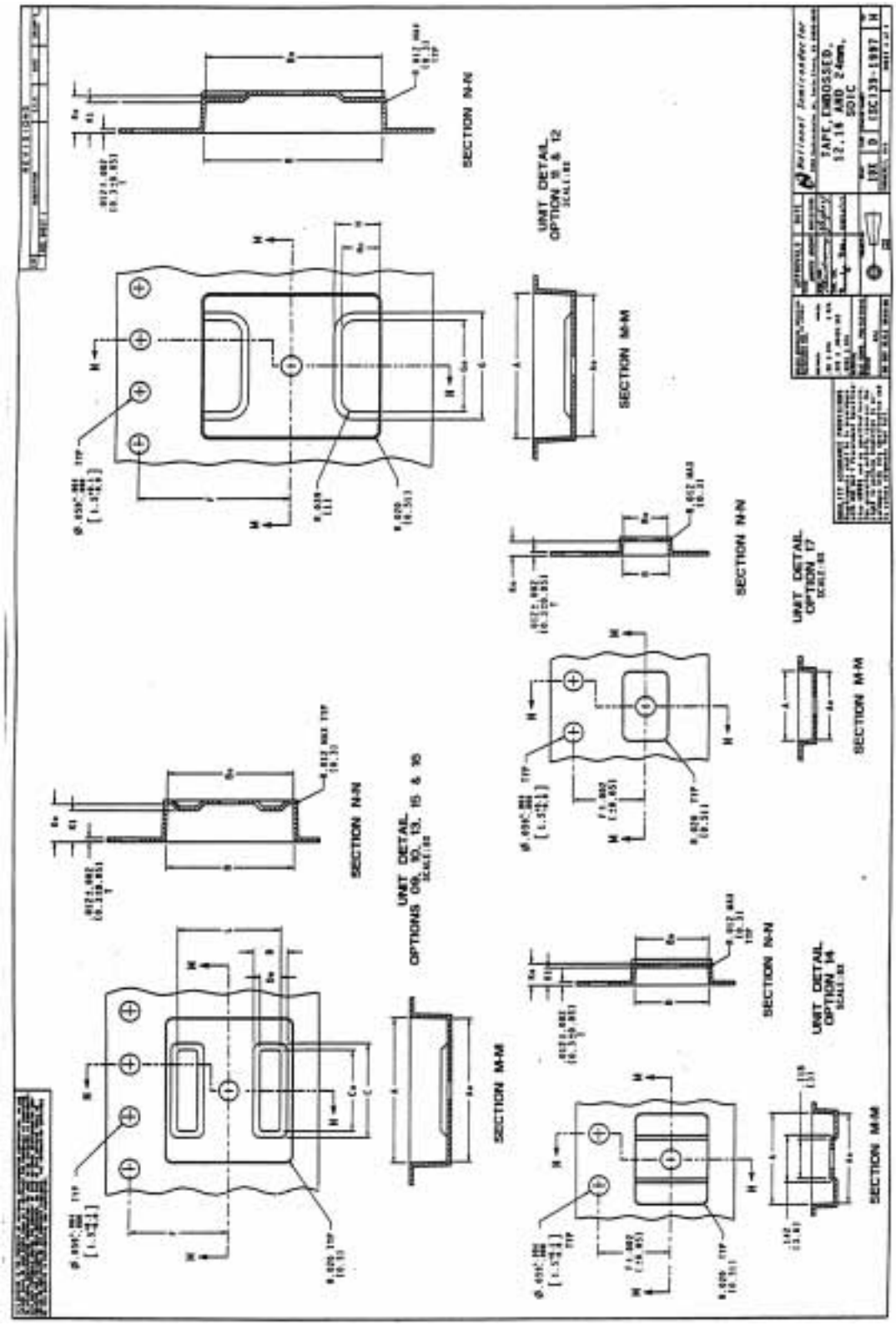
4.0 PACKAGING INFORMATION



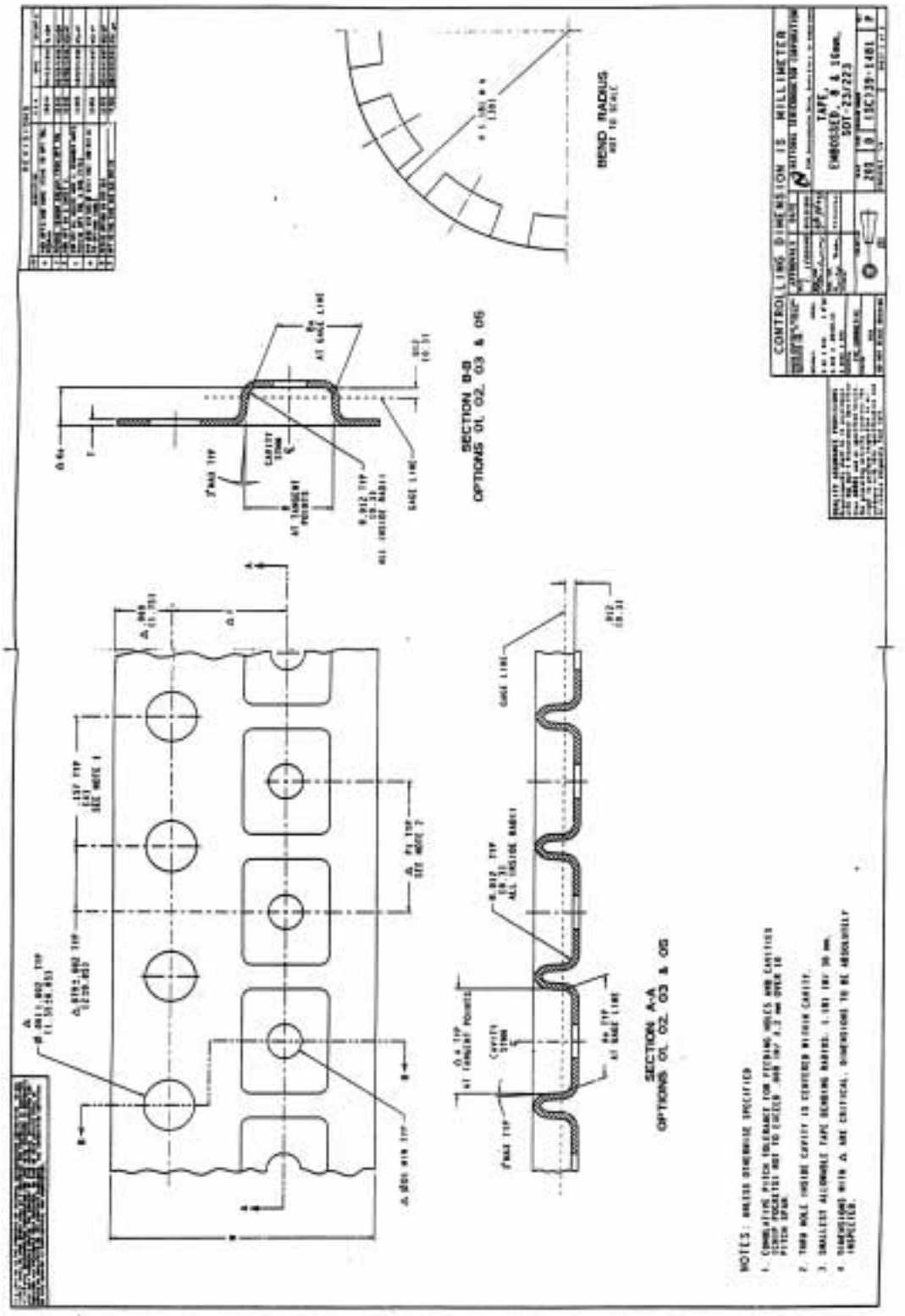

TAPE, EMBOSSED,
12.1V AND 24mm,
SOIC
BEND RADIUS
SECTION N-N
UNIT DETAIL
OPTIONS 01 THRU 05
SECTION M-M

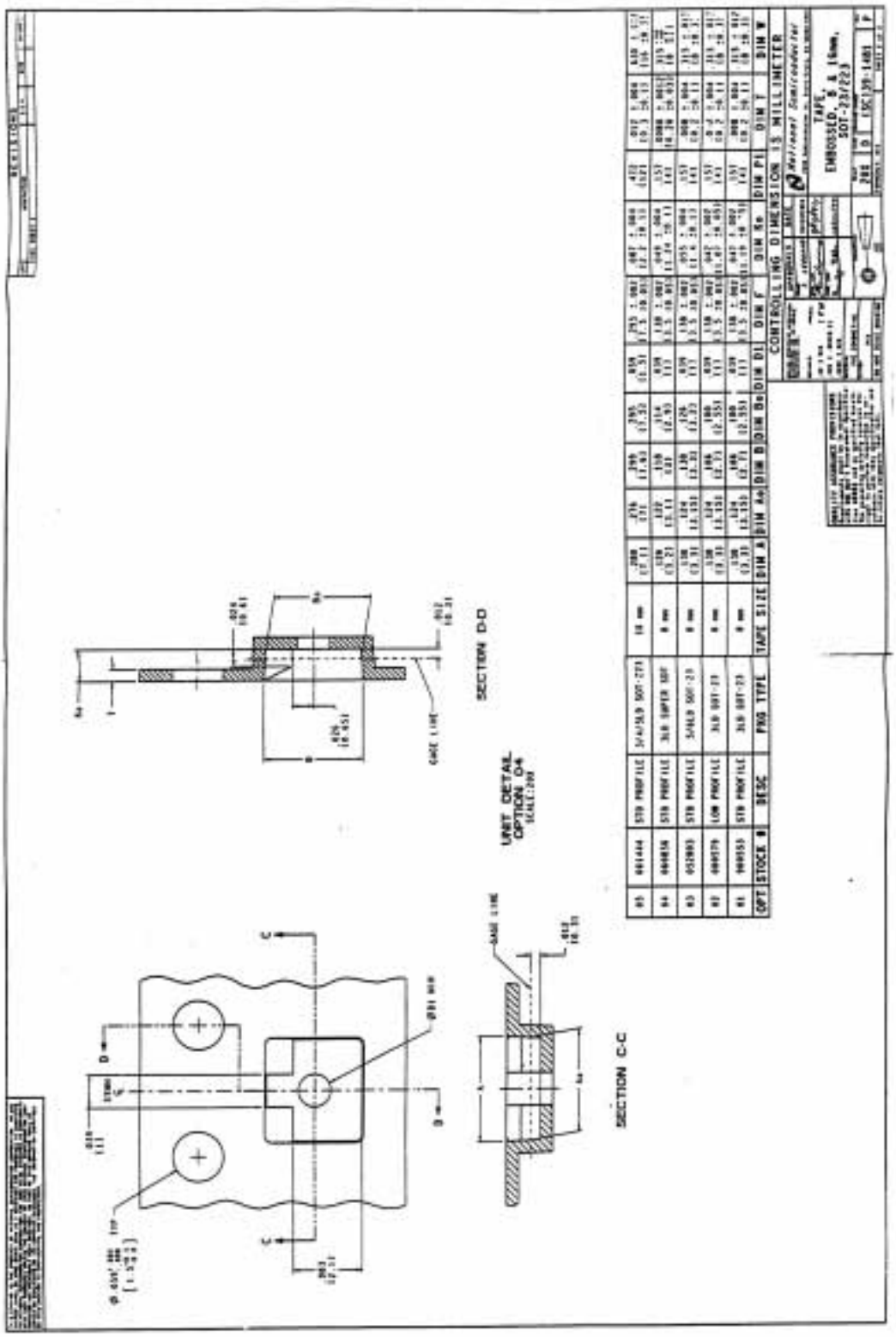
4.0 PACKAGING INFORMATION

For 5 lead SOT-23 look at dimensions in table for OPT03 (STOCK #052803)


TAPE, EMBOSSED, 12.16 AND 24mm, SOIC
SECTION N-N
SECTION M-M
UNIT DETAIL OPTION 16 & 12
UNIT DETAIL OPTIONS 09, 13, 15 & 35
UNIT DETAIL OPTION 17
UNIT DETAIL OPTION 14

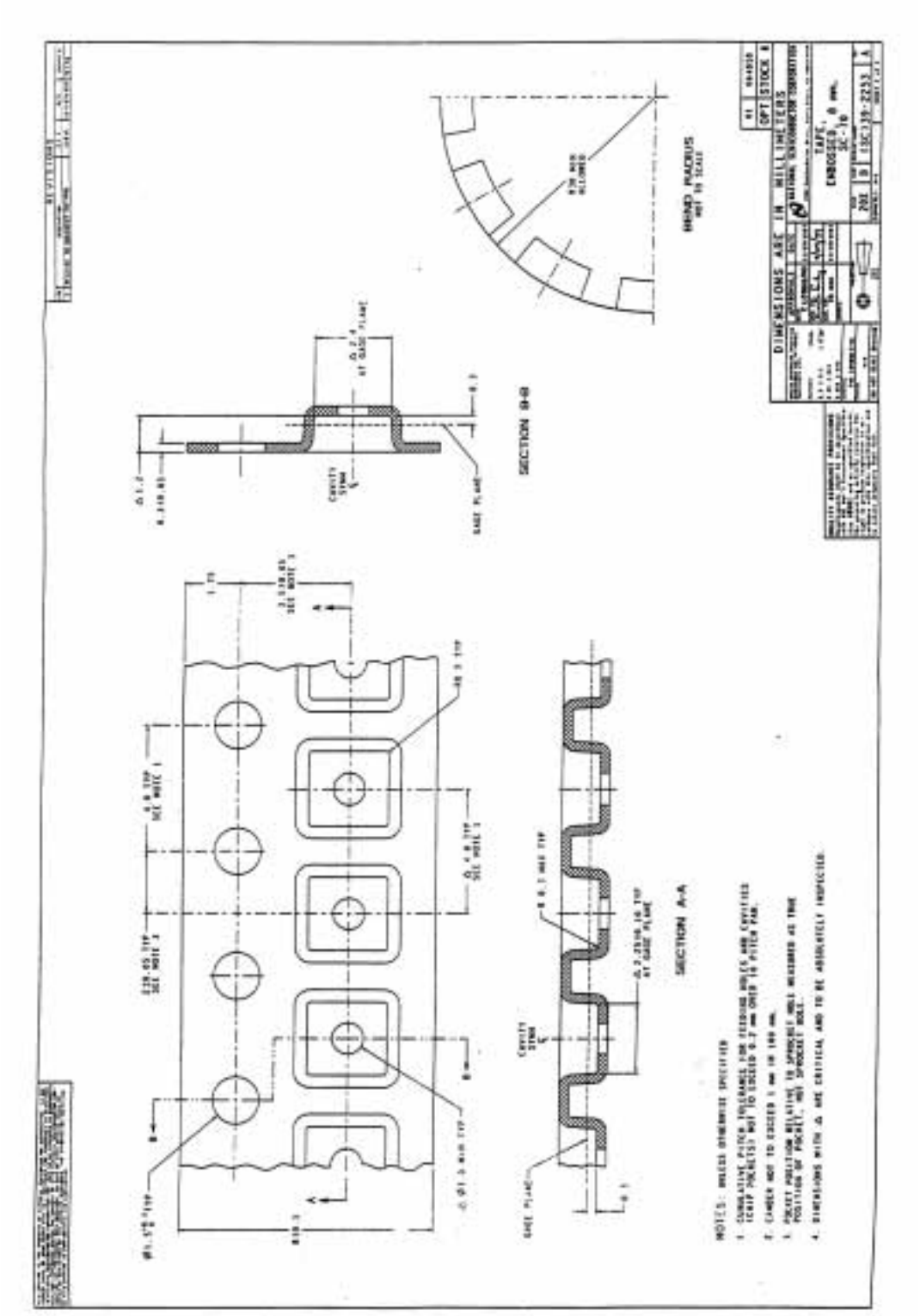
4.0 PACKAGING INFORMATION




SECTION D-D
SECTION C-C
UNIT DETAIL
OPTION 04
CONTROLLING DIMENSION IS MILLIMETER
TAPE,
EMBOSSED, 8 & 16mm,
SOT-23/223

4.0 PACKAGING INFORMATION

For SC70 Package



5.0 RELIABILITY DATA

5.1 Reliability Reports for LMV3xx

National Semiconductor

Reliability Test Report

File Number:
FSC19970377
Originator:
Raj Subramoniam
Date:October 8, 1997

Purpose

THE LMV324/LMV358 NEW DEVICE QUALIFICATIONS

Approvals

Reliability Engineer — Date: 3-16-98

Mgr. Rel. Engineering — Date: 3-16-98

Reference File Numbers

RSC199701567
RSC199701566
RSC199701565
Q19960592

Distribution List

Std. Analog: Frank Smoot, Sharon Ignaut, Tuc Doan
Rel Engineering: Nick Stanco, Al Sezen
File

Abstract

The LMV324 is a new device that will be fabricated with CS80CBI process in the 6 inch fab line in NSFM. This device is a high performance, low voltage quad operational amplifier that will be available in both SOIC 14 leads and TSSOP 14 leads packages. The LMV358 is a dual operational amplifier, and is metal mask option of the LMV324. The LMV358 will be available in both MSOP-8 and SOIC-8 packages.

The reliability testing was completed successfully as per the qualification plan. Based on the excellent results obtained, the LMV324 (in TSSOP-14 and SOIC-14) and LMV358 (in MSOP-8 and SOIC-8) is now fully qualified and released to production.

Human Body and Machine model ESD characterizations were performed on LMV324, and was found to be rated at 2.25KV and 100V, respectively. The LMV358 also passed Latch-up test (+/- 300mA over-current and 10V over-voltage condition) as per JEDEC Standard 17.

Description

Test Request	Device Name	Sbop	Wafer Die Run	Fab Loc	Fab Line	Pkg Code	# Leads	Assy Loc	Date Cd	Mold Cmpd
RSC199701565	LMV324M	A		FM	6 INCH	SOIC	14	EM	9718	B14
RSC199701566	LMV358MM	A		FM	6 INCH	MSOP	8	EM		N7400
RSC199701567	LMV324MTC	A		FM	6 INCH	TSSOP	14	AN*	9724	KMV184H

* AMKOR, Philippines

Tests Performed

Test: Autoclave Test with Level 1 Preconditioning (ACLV)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199701565	LMV324M	A	100	15	121	0
RSC199701566	LMV358MM	A	100	15	121	0
RSC199701567	LMV324MTC	A	100	15	121	0

Timepoints:

Test Request	TP	Duration
RSC199701565/1566/1567	1	168
RSC199701565/1566/1567	2	336

Test: Operating Life Test (Static) (SOPL, bias condition +/- 2.75V))

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp	Board Number
RSC199701565	LMV324M	A	0	0	150	0	5010RE
RSC199701566	LMV358MM	A	0	0	150	0	5256RE
RSC199701567	LMV324MTC	A	0	0	150	0	5531RE

Timepoints:

Test Request	TP	Duration
RSC199701565/1566/1567	1	168
RSC199701565/1566/1567	2	500
RSC199701565/1566/1567	3	1000

Test: Temperature Cycle with Level 1 Preconditioning (TMCL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199701565	LMV324M	A	0	0	150	-65
RSC199701566	LMV358MM	A	0	0	150	-65
RSC199701567	LMV324MTC	A	0	0	150	-65

Timepoints:

Test Request	TP	Duration
RSC199701565/1566/1567	1	500
RSC199701565/1566/1567	2	1000

Test: Temperature Humidity Bias Test with level 1 Preconditioning (THBT, bias condition +/-2.75V)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp	Board Number
RSC199701565	LMV324M	A	85	0	85	0	5011RE
RSC199701566	LMV358MM	A	85	0	85	0	5257RE
RSC199701567	LMV324MTC	A	85	0	85	0	5532RE

Timepoints:

Test Request	TP	Duration
RSC199701565	1	168
RSC199701565	2	500
RSC199701565	3	1000
RSC199701567	1	168
RSC199701567	2	500
RSC199701567	3	524
RSC199701567	4	1024
RSC199701566	1	168
RSC199701566	2	500
RSC199701566	3	644
RSC199701566	4	1000

Note:
Level 1 Preconditioning: 85°C/85%RH moisture soak for 168 hrs. followed by 3 passes of 235°C IR reflow.

Results/Discussion

Test: Autoclave Test (ACLV)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199701565	LMV324M	A	1	168	77	0
RSC199701565	LMV324M	A	2	336	77	0
RSC199701566	LMV358MM	A	1	168	77	0
RSC199701566	LMV358MM	A	2	336	77	0
RSC199701567	LMV324MT	A	1	168	77	0
RSC199701567	LMV324MT	A	2	336	77	0

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199701565	LMV324M	A	1	168	77	0
RSC199701565	LMV324M	A	2	500	77	0
RSC199701565	LMV324M	A	3	1000	77	0
RSC199701566	LMV358MM	A	1	168	77	0
RSC199701566	LMV358MM	A	2	500	77	0
RSC199701566	LMV358MM	A	3	1000	77	0
RSC199701567	LMV324MT	A	1	168	77	0
RSC199701567	LMV324MT	A	2	500	77	0
RSC199701567	LMV324MT	A	3	1000	77	0

Test: Temperature Humidity Bias Test (THBT)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199701565	LMV324M	A	1	168	77	0
RSC199701565	LMV324M	A	2	500	77	0
RSC199701565	LMV324M	A	3	1000	77	0
RSC199701566	LMV358MM	A	1	168	77	0
RSC199701566	LMV358MM	A	2	500	77	0
RSC199701566	LMV358MM	A	3	544	77	0
RSC199701566	LMV358MM	A	4	1000	77	0
RSC199701567	LMV324MT	A	1	168	77	0
RSC199701567	LMV324MT	A	2	500	76*	0
RSC199701567	LMV324MT	A	3	524	76	0
RSC199701567	LMV324MT	A	4	1024	76	0

Test: Temperature Cycle (TMCL)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199701565	LMV324M	A	1	500	77	0
RSC199701565	LMV324M	A	2	1000	77	0
RSC199701566	LMV358MM	A	1	500	77	0
RSC199701566	LMV358MM	A	2	1000	76*	0
RSC199701567	LMV324MT	A	1	500	76	0
RSC199701567	LMV324MT	A	2	1000	76	0

ESD Human body Model

Device	Voltage	Sample Size	Rejects
LMV324MT	1250V	5	0
LMV324MT	1500V	5	0
LMV324MT	1750V	5	0
LMV324MT	2000V	5	0
LMV324MT	2250V	5	0

ESD Machine Model

Device	Voltage	Sample Size	Rejects
LMV324MT	100V	5	0
LMV324MT	150V	5	3

Latch-up test

Device	Sample Size	Rejects
LMV324MT	6	0

Note: * One unit lost in the oven.

Conclusion

The estimated failure rate of the LMV324 family of devices is 18.211 FITS, and an MTBF of 5,4909,836 hours. The calculation was based on a 60% confidence factor and an activation energy of 0.7eV derated to 55C operating temperature.

The LMV324 (in TSSOP-14 and SOIC-14) and LMV358 (in MSOP-8 and SOIC-8) are now fully qualified and released to production.

National Semiconductor

Reliability Test Report

File Number:
FEM19970494
Originator:
Kumar Suresh
Date:December 29, 1997

Purpose

LMV321 SC70-5 PACKAGE QUALIFICATION

Approvals

Reliability Engineer — Date: 2-3-98

Mgr, Prod. Engineering — Date: 2-3-98

Reference File Numbers

REM199702597
Q19970103

Distribution List

KK SIOW, ANTHONY LAW, CSTEOH, RAJ SUBRAMANIAM, NICK STANCO

Abstract

The LMV321 is a single OP-AMP version based on the design of LMV324. This is a completely new layout incorporating only a single OP-AMP in a die size of 17X17 mils. The die will be fabricated with CS80CBI process and will be assembled in 5 lead SC70 package. In order to qualify the device in SC-70 package, 1 lot of OPL and 3 lots of BAKE, ACLV, TMCL, and THBT. Qualification of the die is achieved by combining this qualification plan and Q1997245.

Description

Test Request	Device Name	Sbgp	Wafer Dia Run	Fab Loc	Fab Line	Pkg Code	# Leads	Assy Loc	Date Cd	Mold Cmpnd
REM199702597	LMV321 SC(5)	A	b0053cg2	FM	6 INCH	MTC45	5	B8	9742	MP-8000C
REM199702597	LMV321 SC(5)	B	b0053g3	FM	6 INCH	MTC45	5	B8	9742	MP-8000C
REM199702597	LMV321 SC(5)	C	b0053de0	FM	6 INCH	MTC45	5	B8	9742	MP-8000C

Tests Performed

Test: Autoclave Test (ACLV)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
REM199702597	LMV321 SC(5)	A	100	15	121	0
REM199702597	LMV321 SC(5)	B	100	15	121	0
REM199702597	LMV321 SC(5)	C	100	15	121	0

Test: High Temperature Storage test (BAKE)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
REM199702597	LMV321 SC(5)	A	0	0	150	0
REM199702597	LMV321 SC(5)	B	0	0	150	0
REM199702597	LMV321 SC(5)	C	0	0	150	0

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
REM199702597	LMV321 SC(5)	A	0	0	150	0
REM199702597	LMV321 SC(5)	B	0	0	150	0
REM199702597	LMV321 SC(5)	C	0	0	150	0

Test: Temperature Cycle (TMCL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
REM199702597	LMV321 SC(5)	A	0	0	150	-65
REM199702597	LMV321 SC(5)	B	0	0	150	-65
REM199702597	LMV321 SC(5)	C	0	0	150	-65

Test: Temperature Humidity Bias Test (THBT)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
REM199702597	LMV321 SC(5)	A	85	0	85	0
REM199702597	LMV321 SC(5)	B	85	0	85	0
REM199702597	LMV321 SC(5)	C	85	0	85	0

PRECONDITIONING: All TMCL, ACLV, and THBT units were preconditioned using a Level 1 moisture soak and IR at 235C.

Results/Discussion

Test: Autoclave Test (ACLV)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
REM199702597	LMV321 SC(5)	A	1	168	77	0
REM199702597	LMV321 SC(5)	B	1	168	77	0
REM199702597	LMV321 SC(5)	C	1	168	77	0

Test: High Temperature Storage test (BAKE)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
REM199702597	LMV321 SC(5)	A	1	168	77	0
REM199702597	LMV321 SC(5)	A	2	500	77	0
REM199702597	LMV321 SC(5)	A	3	1000	77	0
REM199702597	LMV321 SC(5)	B	1	168	77	0
REM199702597	LMV321 SC(5)	B	2	500	77	0
REM199702597	LMV321 SC(5)	B	3	1000	77	0
REM199702597	LMV321 SC(5)	C	1	168	77	0
REM199702597	LMV321 SC(5)	C	2	500	77	0
REM199702597	LMV321 SC(5)	C	3	1000	77	0

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
REM199702597	LMV321 SC(5)	A	1	168	77	0
REM199702597	LMV321 SC(5)	A	2	500	77	0
REM199702597	LMV321 SC(5)	A	3	1000	77	0
REM199702597	LMV321 SC(5)	B	1	168	77	0
REM199702597	LMV321 SC(5)	B	2	500	77	0
REM199702597	LMV321 SC(5)	B	3	1000	77	0
REM199702597	LMV321 SC(5)	C	1	168	77	0
REM199702597	LMV321 SC(5)	C	2	500	77	0
REM199702597	LMV321 SC(5)	C	3	1000	77	0

Test: Temperature Humidity Bias Test (THBT)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
REM199702597	LMV321 SC(5)	A	1	168	77	0
REM199702597	LMV321 SC(5)	A	2	500	77	0
REM199702597	LMV321 SC(5)	A	3	1000	77	0
REM199702597	LMV321 SC(5)	B	1	168	77	0
REM199702597	LMV321 SC(5)	B	2	500	77	0
REM199702597	LMV321 SC(5)	B	3	1000	77	0
REM199702597	LMV321 SC(5)	C	1	168	77	0
REM199702597	LMV321 SC(5)	C	2	500	77	0
REM199702597	LMV321 SC(5)	C	3	1000	77	0

Test: Temperature Cycle (TMCL)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
REM199702597	LMV321 SC(5)	A	1	500	77	0
REM199702597	LMV321 SC(5)	A	2	1000	77	0
REM199702597	LMV321 SC(5)	A	3	2000	77	0
REM199702597	LMV321 SC(5)	B	1	500	77	0
REM199702597	LMV321 SC(5)	B	2	1000	77	0
REM199702597	LMV321 SC(5)	B	3	2000	77	0
REM199702597	LMV321 SC(5)	C	1	500	77	0
REM199702597	LMV321 SC(5)	C	2	1000	77	0
REM199702597	LMV321 SC(5)	C	3	2000	77	0

ASSEMBLY TESTS:	Sbgrp	Sample Size	Rejects
Physical Dimension	A	10	0
	B	10	0
	C	10	0
Lead Integrity	A	45 Leads	0
	B	45 Leads	0
	C	45 Leads	0
Bond Pull	A	30 Bonds	0
	B	30 Bonds	0
	C	30 Bonds	0
Bond Shear	A	30 Bonds	0
	B	30 Bonds	0
	C	30 Bonds	0
Solderability	A	15	0
	B	15	0
	C	15	0
Resistance to solder	A	25	0
	B	25	0
	C	30	0

ESD			
Human Body Model	500v	5	0
	1.0Kv	5	4
	1.5Kv	5	0
	2.0Kv	5	2
	2.5Kv	5	1
Machine Model	50v	5	0
	100v	5	0
	150v	5	0

Conclusion

The LMV321 in the new SC70 package has successfully passed all required reliability tests through their release timepoints. The LMV321 is now qualified to be built in the SC70 package.

National Semiconductor

Reliability Test Report

File Number:
FSC19970440
Originator:
Raj Subramoniam
Date:November 18, 1997

Purpose

TO QUALIFY THE NEW DEVICE, LMV321 IN SOT23-5 PACKAGE.

Approvals

S. Rajman 11/18/97
Reliability Engineer Date

Mgr. Prod. Engineering 11/18/97
Date

Reference File Numbers

RSC199702511
RSC199702489
RSC199702407
Q19970245

Distribution List

Rel Engineering: Al Sezen, Nick Stanco
Amplifiers: Jim Dreyfus, Brian Baker, Sharon Ignaut

Abstract

The LMV321 is a single OP-AMP version based on the design of LMV324. This is a completely new layout incorporating only a single OP-AMP in a die size of 17X17 mils. The die will be fabricated with CS80CBI process and will be assembled in 5 lead SOT-23 package. Qualification of the LMV321 in SOT23-5 package was achieved by running 1 lot each of BAKE, ACLV, TMCL and THBT, and 3 lots of OPL. Based on the excellent results obtained so far, the device is conditionally released to complete 500 hrs. on the last 2 lots of OPL.

The LMV321 is rated 500V Human Body Model ESD and 150V Machine Model ESD.

Description

Test Request	Device Name	Sbgp	Wafer Die Run	Fab Loc	Fab Line	Pkg Code	# Leads	Assy Loc	Date Cd	Mold C
RSC199702407	LMV321M5	A	B0083CG2 W#1	FM	6 INCH	TITG23	5	EM		B18
RSC199702489	LMV321M5	A	B0083CG3 W#1	FM	6 INCH	TITG23	5	EM		B18
RSC199702511	LMV321M5	A	B0083DE0 W#6	FM	6 INCH	TITG23	5	EM		B18

Tests Performed

Test: Autoclave (ACLV) with Level 1 preconditioning*

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199702407	LMV321M5	A	100	15psi	121	0

Timepoints:	Test Request	TP	Duration
	RSC199702407	1	96
	RSC199702407	2	168

Test: High Temperature Storage test (BAKE)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp

	RSC199702407	1	168
	RSC199702407	2	500
	RSC199702407	3	1000

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199702407	LMV321M5	A	0	0	150	0
RSC199702489	LMV321M5	A	0	0	150	0
RSC199702511	LMV321M5	A	0	0	150	0

Timepoints:	Test Request	TP	Duration
	RSC199702407/2489/2511	1	168
	RSC199702407/2489/2511	2	500
	RSC199702407/2489/2511	3	1000

Test: Temperature Cycle (TMCL) with Level 1 preconditioning*

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199702407	LMV321M5	A	0	0	150	-65

Timepoints:	Test Request	TP	Duration
	RSC199702407	1	500
	RSC199702407	2	1000

Test: Temperature Humidity Bias Test (THBT) with Level 1 preconditioning*

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199702407	LMV321M5	A	85	0	85	0

Timepoints:	Test Request	TP	Duration
	RSC199702407	1	168
	RSC199702407	2	500
	RSC199702407	3	1000

Note:

- Level 1 preconditioning Sequence: 85°C/85%RH moisture soak for 168 hrs. followed by 3 passes of 235°C IR reflow.

Results/Discussion

Test: Autoclave Test (ACLV)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199702407	LMV321M5	A	1	96	77	0
RSC199702407	LMV321M5	A	2	168	77	0

Test: High Temperature Storage test (BAKE)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199702407	LMV321M5	A	1	168	77	0
RSC199702407	LMV321M5	A	2	500	77	0
RSC199702407	LMV321M5	A	3	1000	77	In progress

Test: Operating Life Test (Static) (SOPL; +/- 2.5V; 4765RE; 5627RE)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199702407	LMV321M5	A	1	168	77	0
RSC199702407	LMV321M5	A	2	500	77	0
RSC199702407	LMV321M5	A	3	1000	77	0
RSC199702489	LMV321M5	A	1	168	77	0
RSC199702489	LMV321M5	A	2	500	76*	In progress
RSC199702489	LMV321M5	A	3	1000	76	In progress
RSC199702511	LMV321M5	A	1	168	77	0
RSC199702511	LMV321M5	A	2	500	77	In progress
RSC199702511	LMV321M5	A	3	1000	77	In progress

5.0 RELIABILITY DATA

Test: Temperature Humidity Bias Test (THBT +/- 2.5V; 4766RE; 5620RE)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199702407	LMV321M5	A	1	168	77	0
RSC199702407	LMV321M5	A	2	500	77	0
RSC199702407	LMV321M5	A	3	1000	77	In progress

Test: Temperature Cycle (TMCL)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199702407	LMV321M5	A	1	500	77	0
RSC199702407	LMV321M5	A	2	1000	77	0

* S/N 21 missing

Conclusion

The estimated failure rate of LMV321 is 54.743FITS and the Mean Time Between Failures (MTBF) is 18267147.54098 hrs. The calculation performed at 60% confidence factor was based on an activation energy of 0.7eV and an ambient operating temperature of 55C.

The LMV321 is now released Code R based on the excellent results obtained.

National Semiconductor

Reliability Test Report

File Number: FSC19980093
Originator: Nick Stanco
Date:February 24, 1998

Purpose

LMV339 / LM393 / LM331
New Device Qualifications

Approvals

Reliability Engineer — Date: 2-3-98
Mgr, Rel. Engineering — Date: 2-3-98

Reference File Numbers

RSC199702691
RSC199702437
RSC199800128
RSC199800207
Q19970635

Distribution List

Doug Simin / Nick Stanco

Abstract

The LMV339 (true quad), LMV393 (dual derived from LMV358), and LMV331 (true single derived from LMV321) comparator devices were subjected to reliability testing per qual plan Q19970635 for qualification as new devices. SOPL testing was completed on all three devices with only two failures on the LMV339. One of these failures was due to EOS/ESD and is invalid. The other failed unit developed a faulty input protection diode on one comparator. If we assume this unit to be a valid failure and consider the implications towards this devices failure rate it can be seen that the failure rate for this device family (the low voltage family of CS80CBI processed amps and comparators) is still at an acceptable level of 8.82 FITS (@ 55C, 0.7eV, 60% CL) at this time and that release of this device is warranted. All three devices passed Latch-up testing and all devices were characterized for both Human Body Model and Machine Model ESD performance levels with rated voltages shown below in bold type. Based on these results the LMV339 (14L TSSOP and 14L SOIC packages), the LMV393 (8L MSOP and 8L SOIC packages) and the LMV331 5L SOT-23 and SC70 packages) are now fully qualified and released to production.

Description

Test Request	Device Name	Sbgp	Fab Loc	Fab Line	Pkg Code	Assy # Leads	Loc	Date Cd	Mold Cmpd
RSC199702437	LMV331M5X	A	FM	6 INCH	T\TG23	5	EM		B18
RSC199702691	LMV339M	A	FM	6 INCH	NMSON	014	EM	9742	B14
RSC199800128	LMV339M	B	FM	CMOS	NMSON	014	EM	9748	B14
RSC199800128	LMV339M	C	FM	CMOS	NMSON	014	EM	9748	B14
RSC199800207	LMV393M	A	FM	6 INCH	NMSON	8	EM	9748	B14

Tests Performed

5.0 RELIABILITY DATA

Test: Operating Life Test (Static) (SOPL): Ta=150C, static bias

Results/Discussion

		Rejects per Lot Sample		
Tests	Time/Cycles	Lot 1	Lot 2	Lot 3
LMV339M SOPL	336	2/77 *Note 1	0/77	0/77
	500	0/75	0/77	0/77
	1000	0/75	—	—
LMV393M SOPL	356	0/77		
	500	0/77		
	1000	—		
LMV331M5X SOPL	168	0/77		
	500	0/77		
	1000	0/77		

Note 1- Two LMV339M devices from Lot 1 failed after 336 hours of SOPL, details follow.

S/N 1 - This device failed ATE testing for high input offset voltage on comparators #1 and #2 and high input bias current on comparator #1. Curve tracing found a pin 5 to pin 12 short. A visual inspection found that the input diode had a metal flash from metal 1 to metal 1. Deprocessing and SEM analysis revealed an oxide rupture bridging metal 1 to metal 1, within the input protection diode. This is an invalid failure due to EOS/ESD of unknown origin.

S/N 23 - This device failed ATE testing for high input offset voltage and high input bias current on one comparator. This device did not recover after a 125C bake. Curve tracing found an early breakdown between pin 11 and pin 12. Bench test found comparator #3 to have more than 2mA input leakage. No anomalies were found during internal visual inspection. PHEMOS was performed and found the input diode to pin 11 to have an emission. This is typical of EOS/ESD damage. The diode was isolated from the circuit and mechanically probed to verify the failure mode. The unit was then deprocessed (in layers, all the way down to silicon), however, no defect was identified.

	HBM ESD		MM ESD		LATCH-UP
LMV339	500V	0/5	100V	0/5	0/5 (Per JEDEC 17)
	800V	**0/5**	**150V**	**0/5**	
	1000V	1/5	175V	2/5	
	1500V	1/5	200V	4/5	
	1750V	4/5			
LMV393	500V	0/5	100V	0/5	0/5 (Per JEDEC 17)
	800V	0/5	**125V**	**0/5**	
	1000V	**0/5**	150V	2/5	
	1500V	1/5	200V	4/5	
	1750V	1/5			
LMV331	500V	0/5	100V	0/5	0/5 (Per JEDEC 17)
	700V	0/5	**125V**	**0/5**	
	800V	**0/5**	150V	2/5	
	900V	1/5	175V	3/5	
	1000V	1/5			

ESD NOTE - BOLD ESD RESULTS REPRESENT THE RATED VALUES FOR EACH DEVICE.

Conclusion

The LMV339 (14L TSSOP and 14L SOIC packages), LMV393 (8L MSOP and 8L SOIC packages) and LMV331 5L SOT-23 and SC70 packages) are now fully qualified and released to production.

National Semiconductor

Reliability Test Report

File Number: **FSC19980031**
Originator: **Nick Stanco**
Date:January 20, 1998

Purpose

LMV821 New Device Qualification

Approvals

Reliability Engineer — Date: 3-16-98

Mgr. Rel. Engineering — Date: 3-16-98

Reference File Numbers

RSC199702913
Q19970977

Distribution List

Altaf Ahmad / Nick Stanco

Abstract

One lot of LMV821, specially bonded-out in an 8L MDIP package for qualification purposes, was subjected to SOPL testing per qual plan Q19970977 for qualification as a new device for the Amplifiers product line. 500 hours of SOPL at Ta=150C was completed without failure on the LMV821 qual lot. HBM and MM ESD characterization were also completed. Based on this SOPL testing, and successfully completed LMV321 5L SOT-23 and 5L SC-70 package qualifications, the LMV821 is now fully qualified and released in both the SOT-23 and SC-70 packages.

Description

Test Request	Device Name	Sbgp	Fab Loc	Fab Line	Pkg Code	Assy # Leads	Assy Loc	Date Cd	Mold Cmpd
RSC199702913	LMV821	A	FM	CS80CBI	NMDIP	8	EM		B8

Tests Performed

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	Rel Ckt	Voltage
RSC199702913	LMV821	A	0	0	150	4755Rs-A	+/- 2.5V

Timepoints:	Test Request	TP	Duration
	RSC199702913	1	168
	RSC199702913	2	500

5.0 RELIABILITY DATA

Results/Discussion

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199702913	LMV821	A	1	168	77	0
RSC199702913	LMV821	A	2	500	77	0

Test: Human Body Model ESD
Result: The LMV821 is rated at ±900V.

Test: Machine Model ESD
Result The LMV821 is rated at ±150V

Conclusion

Based upon successful completion of all reliability requirements as specified in qual plan Q19970977, the LMV821 op-amp is now fully qualified and released to production in both the 5L SOT-23 and 5L SC-70 packages.

National Semiconductor

Reliability Test Report

File Number: FSC19980030
Originator: Nick Stanco
Date: January 20, 1998

Purpose

LMV822 & LMV824 New Device Qualifications

Approvals

Reliability Engineer — Date: 3-16-98

Mgr. Rel. Engineering — Date: 3-16-98

Reference File Numbers

RSC199702693
Q19970978

Distribution List

Altaf Ahmad / Nick Stanco

Abstract

One lot of LMV824M in the 14L SOIC package was subjected to SOPL testing per qual plan Q19970978 to qualify the LMV824 and LMV822 (metal option to create dual version from the LMV824 quad op-amp) as new devices for the Amplifiers product line. 1000 hours of SOPL at Ta=150C was completed without failure on the LMV824M qual lot. ESD and Latch-up tests yielded acceptable results. Based on these results both devices are now fully qualified and released to production.

The LMV822 is qualified in both the 8L MSOP and 8L SOIC packages and the LMV824 is qualified in both the 14L TSSOP and 14L SOIC packages.

Description

Test Request	Device Name	Sbgp	Fab Loc	Fab Line	Pkg Code	# Leads	Assy Loc	Date Cd	Mold Cmpd
RSC199702693	LMV824M	A	FM	CS80CBI	NSOIC	014	EM	9745	B14

Tests Performed

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	Rel Ckt	Voltage
RSC199702693	LMV824M	A	———	———	150	5009Re-A	+/- 2.5V

Timepoints:	Test Request	TP	Duration
	RSC199702693	1	168
	RSC199702693	2	500
	RSC199702693	3	1000

5.0 RELIABILITY DATA

Results/Discussion

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	TP	Duration	Sample Size	Rejects
RSC199702693	LMV824M	A	1	168	77	0
RSC199702693	LMV824M	A	2	500	77	0
RSC199702693	LMV824M	A	3	1000	77	0

Test: Human Body Model ESD
Result: Both the LMV822 and LMV824 achieved a rating of ±2000V.

Test: Machine Model ESD
Result: Both the LMV822 and LMV824 achieved a rating of ±100V.

Test: Latch-up
Result: Both devices are rated to ±300ma at 25°C and 85°C.

Conclusion

Based upon successful completion of all reliability requirements as specified in qual plan Q19970978, the LMV822 and LMV824 op-amps are now fully qualified and released to production.

6.0 CHARACTERIZATION DATA

6.1 Parametric Data for LMV3xx

LMV324 Room Temperature Data

Test Name	Units	Avg	Sigma
PSI 2.7V	mA	0.272	0.024
PSI 5V	mA	0.379	0.028
VOS A 2.7V	mV	1.4	2
VOS B 2.7V	mV	1.5	1.9
VOS C 2.7V	mV	1.5	2
VOS D 2.7V	mV	1.4	2
VOS A 5V	mV	-0.2	1.8
VOS B 5V	mV	-0.1	1.8
VOS C 5V	mV	-0.1	1.8
VOS D 5V	mV	-0.2	1.9
-IBIAS A 2.7V	nA	-16.3	2.1
-IBIAS B 2.7V	nA	-16.5	2.3
-IBIAS C 2.7V	nA	-16.3	2
-IBIAS D 2.7V	nA	-16	3.5
+IBIAS A 2.7V	nA	16.1	2.1
+IBIAS B 2.7V	nA	16	2
+IBIAS C 2.7V	nA	16.5	2
+IBIAS D 2.7V	nA	16.7	3.7
IOS A 2.7V	nA	-0.3	1.5
IOS B 2.7V	nA	-0.6	2.1
IOS C 2.7V	nA	0.3	1.6
IOS D 2.7V	nA	0.9	3.5
-IBIAS A 5V	nA	-18.1	2.4
-IBIAS B 5V	nA	-18.1	2.4
-IBIAS C 5V	nA	-18.7	2.4
-IBIAS D 5V	nA	-18.7	3.2
+IBIAS A 5V	nA	19.6	2.4
+IBIAS B 5V	nA	19.6	2.5
+IBIAS C 5V	nA	19.2	2.2
+IBIAS D 5V	nA	18.8	2.8
IOS A 5V	nA	1.7	2.9
IOS B 5V	nA	1.9	3
IOS C 5V	nA	2	3.1
IOS D 5V	nA	2.1	3.1
+SWINGA 5V 2K	V	4.951	0.034
+SWINGB 5V 2K	V	4.95	0.048
+SWINGC 5V 2K	V	4.951	0.006
+SWINGD 5V 2K	V	4.951	0.033

LMV324 Room Temperature Data (cont)

Test Name	Units	Avg	Sigma
+SWINGA 5V 10K	V	4.951	0.001
+SWINGB 5V 10K	V	4.991	0.002
+SWINGC 5V 10K	V	4.99	0.001
+SWINGD 5V 10K	V	4.991	0.002
+SWINGA 2.7V 10	V	2.693	0.002
+SWINGB 2.7V 10	V	2.692	0.001
+SWINGC 2.7V 10	V	2.692	0.001
+SWINGD 2.7V 10	V	2.692	0.001
-SWINGA 5V 2K	V	0.123	0.007
-SWINGB 5V 2K	V	0.122	0.006
-SWINGC 5V 2K	V	0.122	0.007
-SWINGD 5V 2K	V	0.124	0.006
-SWINGA 5V 10K	V	0.073	0.006
-SWINGB 5V 10K	V	0.072	0.006
-SWINGC 5V 10K	V	0.073	0.006
-SWINGD 5V 10K	V	0.073	0.006
-SWINGA 2.7V 10	V	0.062	0.004
-SWINGB 2.7V 10	V	0.062	0.003
-SWINGC 2.7V 10	V	0.062	0.004
-SWINGD 2.7V 10	V	0.063	0.004

LMV321 Room Temperature Data

Test Name	Units	Avg	Sigma
PSI 2.7V	mA	0.077	0.005
PSI 5V	mA	0.107	0.006
VOS A 2.7V	mV	-0.4	2.3
VOS A 5V	mV	-1.9	2
-IBIAS A 2.7V	nA	-17.2	3.6
+IBIAS A 2.7V	nA	16.1	3.9
IOS A 2.7V	nA	-1.2	1.9
-IBIAS A 5V	nA	-18.2	4.1
+IBIAS A 5V	nA	19.9	4.1
IOS A 5V	nA	-0.2	1.3
+SWINGA 5V 2K	V	4.95	0.015
+SWINGA 5V 10K	V	4.991	0.004
+SWINGA 2.7V10K	V	2.692	0.002
-SWINGA 5V 2K	V	0.127	0.013
-SWINGA 5V 10K	V	0.076	0.004
-SWINGA 2.7V10K	V	0.065	0.003

LMV358 Room Temperature Data

Test Name	Units	Avg	Sigma
PSI 2.7V	mA	0.132	0.023
PSI 5V	mA	0.243	0.028
VOS A 2.7V	mV	2.8	2.2
VOS B 2.7V	mV	2.9	2.2
VOS A 5V	mV	-0.9	2.1
VOS B 5V	mV	-1	2
-IBIAS A 2.7V	nA	-14	6.9
-IBIAS B 2.7V	nA	-12.9	6.3
+IBIAS A 2.7V	nA	14.1	6.6
+IBIAS B 2.7V	nA	13.1	7
IOS A 2.7V	nA	0.4	2.1
IOS B 2.7V	nA	0.9	2.1
-IBIAS A 5V	nA	-21.1	5.6
-IBIAS B 5V	nA	-20.5	5.6
+IBIAS A 5V	nA	23	5.4
+IBIAS B 5V	nA	21.4	5.7
IOS A 5V	nA	0.1	1.8
IOS B 5V	nA	0.1	2.1
+SWINGA 5V 2K	V	4.938	0.029
+SWINGB 5V 2K	V	4.943	0.02
+SWINGA 5V 10K	V	4.988	0.006
+SWINGB 5V 10K	V	4.989	0.005
+SWINGA 2.7V 10K	V	2.692	0.002
+SWINGB 2.7V 10K	V	2.693	0.002
-SWINGA 5V 2K	V	0.126	0.019
-SWINGB 5V 2K	V	0.127	0.018
-SWINGA 5V 10K	V	0.073	0.009
-SWINGB 5V 10K	V	0.073	0.009
-SWINGA 2.7V 10K	V	0.066	0.005
-SWINGB 2.7V 10K	V	0.067	0.005

6.0 CHARACTERIZATION DATA

LMV339 Room Temperature Data

Test Name	Units	Avg	Sigma
PSI 5V	UA	153.3	11.6
PSI 2.7V	UA	115	9.7
VSAT 4MA 5V A	MV	207.1	7.6
VSAT 4MA 5V B	MV	202	3.6
VSAT 4MA 5V C	MV	205	5.2
VSAT 4MA 5V D	MV	199	3.9
VOS 5V A	MV	-2.1	1.9
VOS 5V B	MV	-2.5	1.9
VOS 5V C	MV	-2.3	2
VOS 5V D	MV	-2.2	1.9
+IIB 5V A	NA	21.9	2.4
+IIB 5V B	NA	21.4	2.1
+IIB 5V C	NA	20.7	2
+IIB 5V D	NA	21.7	2.5
-IIB 5V A	NA	-25	2.2
-IIB 5V B	NA	-25.7	2
-IIB 5V C	NA	-25.6	2.2
-IIB 5V D	NA	-25.3	2.1
IOS 5V A	NA	-2.7	2.2
IOS 5V B	NA	-3.9	2.1
IOS 5V C	NA	-3.9	2.1
IOS 5V D	NA	-3.1	2.1
VOS 2.7V A	MV	-0.3	2.1
VOS 2.7V B	MV	-0.4	2.3
VOS 2.7V C	MV	-0.6	2.1
VOS 2.7V D	MV	-0.1	2.1
+IIB 2.7V A	NA	17.9	1.9
+IIB 2.7V B	NA	17.4	1.9
+IIB 2.7V C	NA	16.5	1.8
+IIB 2.7V D	NA	17.6	1.8
-IIB 2.7V A	NA	-18.7	1.8
-IIB 2.7V B	NA	-19.3	1.7
-IIB 2.7V C	NA	-19.2	1.9
-IIB 2.7V D	NA	-19.2	1.7
IOS 2.7V A	NA	-0.8	1.9
IOS 2.7V B	NA	-1.7	2
IOS 2.7V C	NA	-1.9	1.8
IOS 2.7V D	NA	-1.2	1.8

LMV393 Room Temperature Data

Test Name	Units	Avg	Sigma
PSI 5V	UA	104.3	8.8
PSI 2.7V	UA	71	6.6
VSAT 4MA 5V A	MV	177.8	3.9
VSAT 4MA 5V B	MV	180.7	4.1
VOS 5V A	MV	-0.4	1.5
VOS 5V B	MV	-0.3	1.6
+IIB 5V A	NA	28.2	3.7
+IIB 5V B	NA	27	3.3
-IIB 5V A	NA	-29.3	3.5
-IIB 5V B	NA	-29.2	4
IOS 5V A	NA	-1	2.1
IOS 5V B	NA	-1.7	2.3
VOS 2.7V A	MV	1.3	1.7
VOS 2.7V B	MV	1.2	1.7
+IIB 2.7V A	NA	20.3	3.1
+IIB 2.7V B	NA	20.9	2.7
-IIB 2.7V A	NA	-20.3	3.2
-IIB 2.7V B	NA	-20.4	3.3
IOS 2.7V A	NA	1.1	1.8
IOS 2.7V B	NA	0.4	1.9

LMV331 Room Temperature Data

Test Name	Units	Avg	Sigma
PSI 5V	UA	66.7	5.4
PSI 2.7V	UA	40.4	5.2
VSAT 4MA 5V	MV	175.3	5.6
VOS 5V	MV	0.6	1.7
VOS 2.7V	MV	2.4	1.9
+IIB 5V	NA	26.6	4.1
-IIB 5V	NA	-27	4.3
IOS 5V	NA	-0.3	2.4
+IIB 2.7V	NA	17.5	2.6
-IIB 2.7V	NA	-17.4	2.1
IOS 2.7V	NA	1.3	2.1

6.2 Parametric Data for LMV8xx

LMV824 Room Temperature Data

Test Name	Units	Avg	Sigma
PSI 2.7V	mA	0.792	0.043
PSI 5V	mA	1.042	0.054
Vos A 2.7V	mV	0.07	1.08
Vos B 2.7V	mV	0.08	1.11
Vos C 2.7V	mV	0.04	1.06
Vos D 2.7V	mV	-0.225	1.14
Vos A 5V	mV	0.055	1.11
Vos B 5V	mV	0.03	1.13
Vos C 5V	mV	-0.168	1.05
Vos D 5V	mV	-0.225	1.15
Neg Ibias A 2.7V	nA	38.3	3.5
Neg Ibias B 2.7V	nA	36.8	3.7
Neg Ibias C 2.7V	nA	38.7	3.1
Neg Ibias D 2.7V	nA	38.1	3.2
Pos Ibias A 2.7V	nA	37.5	3.6
Pos Ibias B 2.7V	nA	36.8	3.7
Pos Ibias C 2.7V	nA	37.9	3.4
Pos Ibias D 2.7V	nA	37.4	3.3
Ios A 2.7V	nA	-0.76	3.9
Ios B 2.7V	nA	-1.04	4.3
Ios C 2.7V	nA	-0.76	3.4
Ios D 2.7V	nA	-0.78	3.5
Neg Ibias A 5V	nA	44.8	3.1
Neg Ibias B 5V	nA	43.8	4.1
Neg Ibias C 5V	nA	43.6	3.5
Neg Ibias D 5V	nA	42.9	3.5
Pos Ibias A 5V	nA	43.7	3.6
Pos Ibias B 5V	nA	42.1	3.9
Pos Ibias C 5V	nA	42.6	3.3
Pos Ibias D 5V	nA	43.1	3.4
Ios A 5V	nA	-1.2	3.8
Ios B 5V	nA	-1.7	4.5
Ios C 5V	nA	-1	3.3
Ios D 5V	nA	-0.8	3.7
Pos Swing A 5V 600	V	4.828	0.004
Pos Swing B 5V 600	V	4.826	0.004
Pos Swing C 5V 600	V	4.826	0.006
Pos Swing D 5V 600	V	4.827	0.004

LMV824 Room Temperature Data (cont)

Test Name	Units	Avg	Sigma
Pos Swing A 5V 2K	V	4.941	0.003
Pos Swing B 5V 2K	V	4.94	0.003
Pos Swing C 5V 2K	V	4.94	0.003
Pos Swing D 5V 2K	V	4.94	0.004
Pos Swing A 2.5V 600	V	2.372	0.004
Pos Swing B 2.5V 600	V	2.372	0.004
Pos Swing C 2.5V 600	V	2.372	0.004
Pos Swing D 2.5V 600	V	2.371	0.005
Pos Swing A 2.7V 2K	V	2.458	0.001
Pos Swing B 2.7V 2K	V	2.458	0.001
Pos Swing C 2.7V 2K	V	2.458	0.001
Pos Swing D 2.7V 2K	V	2.457	0.001
Neg Swing A 5V 600	V	0.185	0.003
Neg Swing B 5V 600	V	0.184	0.003
Neg Swing C 5V 600	V	0.184	0.004
Neg Swing D 5V 600	V	0.187	0.004
Neg Swing A 5V 2K	V	0.112	0.003
Neg Swing B 5V 2K	V	0.111	0.002
Neg Swing C 5V 2K	V	0.111	0.002
Neg Swing D 5V 2K	V	0.112	0.002
Neg Swing A 2.5V 600	V	0.136	0.003
Neg Swing B 2.5V 600	V	0.135	0.003
Neg Swing C 2.5V 600	V	0.135	0.003
Neg Swing D 2.5V 600	V	0.137	0.003
Neg Swing A 2.7V 2K	V	0.089	0.002
Neg Swing B 2.7V 2K	V	0.09	0.002
Neg Swing C 2.7V 2K	V	0.09	0.002
Neg Swing D 2.7V 2K	V	0.09	0.002

LMV822 Room Temperature Data

Test Name	Units	Avg	Sigma
PSI 2.7V	mA	0.409	0.022
PSI 5V	mA	0.534	0.023
Vos A 2.7V	mV	0.07	1.08
Vos B 2.7V	mV	0.08	1.11
Vos A 5V	mV	0.055	1.11
Vos B 5V	mV	0.03	1.13
Neg Ibias A 2.7V	nA	38.3	3.5
Neg Ibias B 2.7V	nA	36.8	3.7
Pos Ibias A 2.7V	nA	37.5	3.6
Pos Ibias B 2.7V	nA	36.8	3.7
Ios A 2.7V	nA	-0.76	3.9
Ios B 2.7V	nA	-1.04	4.3
Neg Ibias A 5V	nA	44.8	3.1
Neg Ibias B 5V	nA	43.8	4.1
Pos Ibias A 5V	nA	43.7	3.6
Pos Ibias B 5V	nA	42.1	3.9
Ios A 5V	nA	-1.2	3.8
Ios B 5V	nA	-1.7	4.5
Pos Swing A 5V 600	V	4.828	0.004
Pos Swing B 5V 600	V	4.826	0.004
Pos Swing A 5V 2K	V	4.941	0.003
Pos Swing B 5V 2K	V	4.94	0.003
Pos Swing A 2.5V 600	V	2.372	0.004
Pos Swing B 2.5V 600	V	2.372	0.004
Pos Swing A 2.7V 2K	V	2.458	0.001
Pos Swing B 2.7V 2K	V	2.458	0.001
Neg Swing A 5V 600	V	0.185	0.003
Neg Swing B 5V 600	V	0.184	0.003
Neg Swing A 5V 2K	V	0.112	0.003
Neg Swing B 5V 2K	V	0.111	0.002
Neg Swing A 2.5V 600	V	0.136	0.003
Neg Swing B 2.5V 600	V	0.135	0.003
Neg Swing A 2.7V 2K	V	0.089	0.002
Neg Swing B 2.7V 2K	V	0.09	0.002

LMV821 Room Temperature Data

Test Name	Units	Avg	Sigma
PSI 2.7V	mA	0.206	0.014
PSI 5V	mA	0.278	0.019
Vos A 2.7V	mV	0.07	1.08
Vos A 5V	mV	0.055	1.11
Neg Ibias A 2.7V	nA	38.3	3.5
Pos Ibias A 2.7V	nA	37.5	3.6
Ios A 2.7V	nA	-0.76	3.9
Neg Ibias A 5V	nA	44.8	3.1
Pos Ibias A 5V	nA	43.7	3.6
Ios A 5V	nA	-1.2	3.8
Pos Swing A 5V 600	V	4.828	0.004
Pos Swing A 5V 2K	V	4.941	0.003
Pos Swing A 2.5V 600	V	2.372	0.004
Pos Swing A 2.7V 2K	V	2.458	0.001
Neg Swing A 5V 600	V	0.185	0.003
Neg Swing A 5V 2K	V	0.112	0.003
Neg Swing A 2.5V 600	V	0.136	0.003
Neg Swing A 2.7V 2K	V	0.089	0.002

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