LMC6035IBP Qualification Package

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Is Size Critical?
We've got the
Smallest Package
Possible!

New Dual Op Amp
in the
8-Bump µSMD
Package.

National Semiconductor

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Semiconductor

LMC6035
QUALIFICATION PACKAGE

Fall 1998

Table of Contents

1.0 INTRODUCTION

1.1 General Product Description

This qualification booklet covers a general purpose Dual Op Amp assembled in a wafer-level chip-scale package. It is available in 3000 piece or 250 piece tape and reel carriers.

LMC6035IBPX (3000 piece tape and reel)
LMC6035IBP (250 piece tape and reel)

It features low voltage single supply operation with guaranteed performance at 2.7V, 3V, and 15V. Using a package with lateral dimensions the same size as the die, it is ideal in applications that can take advantage of a surface mount package smaller than SOT23 or SC70.

The LMC6035 has previously been offered only in larger size packages (8-Pin Small Outline – LMC6035IMX/LMC6035IM, and 8-Pin Mini Small Outline – LMC6035IMMX/LMC6035IMM).

1.2 Technical Product Description

As with previous versions of LMC6035, the LMC6035IBPX and LMC6035IBP is manufactured using National's double silicon poly gate CMOS process with 4-micron minimum channel length and single-layer metal. Internal name for this process is P2CMOS, which uses 6-inch wafers.

National's name for the wafer-level chip-scale package used for LMC6035 is µSMD (micro-Surface-Mount-Device). Since assembly of the die is done at wafer level, there are additional wafer processing steps that are used instead of the usual assembly of a molded plastic surface mount package. These additional steps are covered under Packaging Information section of this qualification booklet.

The µSMD version of LMC6035 is assembled with 8 eutectic solder bumps (functioning as pins) on active side of die. Non-active side of die is coated with epoxy and laser marked with a pin1 orientation symbol, part number identification code, and a die lot/date code. Customer mounts part on application printed circuit board bump side down using same methods as other small surface mount packages.

1.3 Reliability/Qualification Overview

Reliability testing was done for 3 different qualification aspects – device level, mechanical joint integrity, and board level.

Device level testing was done on LMC6035 and included Operational Life, High Temperature Bias Test, and Temperature Cycle.

Mechanical joint integrity of 2 interfaces – bump to die and bump to printed circuit board, was done using a daisy chain test die.

Board level reliability also used the daisy chain test die mounted on boards and involved drop, bend, and vibration tests.

1.4 Technical Assistance

Package Engineer

Nikhil Kelkar
email: Nikhil.Kelkar@nsc.com
Tel: 408.721.5506

Applications Engineer

John Christensen
email: John.Christensen@nsc.com
Tel: 408.721.6815

Product Engineer

Doug Simin
email: Doug.Simin@nsc.com
Tel: 408.721.3245

2.0 DEVICE INFORMATION

2.1 Datasheet

National Semiconductor

June 1998

LMC6035 Dual /LMC6036 Quad Low Power 2.7V Single Supply CMOS Operational Amplifiers

General Description

. The LMC6035/6 is an economical, low voltage op amp capable of rail-to-rail output swing into loads of 600Ω. LMC6035 is available in a chip sized package (8-Bump WLCS) using National's µSMD package technology. Both allow for single supply operation and are guaranteed for 2.7V, 3V, 5V and 15V supply voltage. The 2.7 supply voltage corresponds to the End-of-Life voltage (0.9V/cell) for three NiCd or NiMH batteries in series, making the LMC6035/6 well suited for portable and rechargeable systems. It also features a well behaved decrease in its specifications at supply voltages below its guaranteed 2.7V operation. This provides a "comfort zone" for adequate operation at voltages significantly below 2.7V. Its ultra low input currents (I_{IN}) makes it well suited for low power active filter application, because it allows the use of higher resistor values and lower capacitor values. In addition, the drive capability of the LMC6035/6 gives these op amps a broad range of applications for low voltage systems.

Features

(Typical Unless Otherwise Noted)

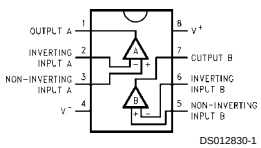
- LMC6035 in µSMD Package
- Guaranteed 2.7V, 3V, 5V and 15V Performance
- Specified for 2 kΩ and 600Ω Loads
- Wide Operating Range: 2.0V to 15.5V
- Ultra Low Input Current: 20 fA
- Rail-to-Rail Output Swing
  @ 600Ω: 200 mV from either rail at 2.7V
  @ 100 kΩ: 5 mV from either rail at 2.7V
- High Voltage Gain: 126dB
- Wide Input Common-Mode Voltage Range
  -0.1V to 2.3V at Vs = 2.7V
- Low Distortion: 0.01% at 10 kHz

Applications

- Filters
- High Impedance Buffer or Preamplifier
- Battery Powered Electronics
- Medical Instrumentation

Connection Diagrams

8-Pin SO/MSOP



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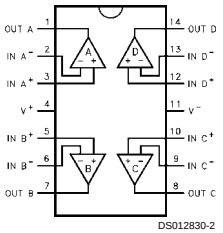
Top View

14-Pin SO/TSSOP



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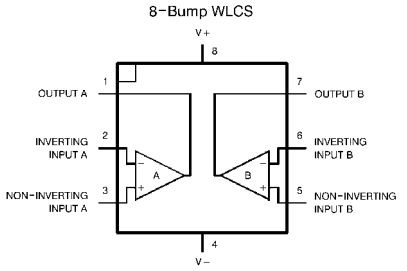
Top View

8−Bump WLCS



Top View

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Ordering Information

Package	Temperature Range	Transport Media	NSC Drawing
	Industrial −40˚C to +85˚C		
8-pin Small Outline (SO)	LMC6035IM	Rails	M8A
	LMC6035IMX	Tape and Reel	
8-pin Mini Small Outline (MSOP)	LMC6035IMM	Rails	MUA08A
	LMC6035IMMX	Tape and Reel	
14-pin Small Outline (SO)	LMC6036IM	Rails	M14A
	LMC6036IMX	Tape and Reel	
14-pin Thin Shrink Small Outline (TSSOP)	LMC6036IMT	Rails	MTC14
	LMC6036IMTX	Tape and Reel	
8-bump Wafer Level Chip Scale (WLCS)	LMC6035IBP	Rails	SWA08A
	LMC6035IBPX	Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	3000V
Machine Model	300V
Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 8)
Output Short Circuit to V^-	(Note 3)
Lead Temperature (soldering, 10 sec.)	260˚C
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 4)	150˚C

Operating Ratings (Note 1)

Supply Voltage	2.0V to 15.5V
Temperature Range	
LMC6035I and LMC6036I	$-40^\circ C \le T_J \le +85^\circ C$
Thermal Resistance (θ_{JA})	
MSOP, 8-pin Mini Surface Mount	230˚C/W
M Package, 8-pin Surface Mount	175˚C/W
M Package, 14-pin Surface Mount	127˚C/W
MTC Package, 14-pin TSSOP	137˚C/W
WLCS Package	220˚C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = 1.0V$, $V_O = 1.35V$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6035I LMC6036I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.5	5	mV
				6	max
TCV_{OS}	Input Offset Voltage Average Drift		2.3		µV/˚C
I_{IN}	Input Current	(Note 11)	0.02		pA
				90	max
I_{OS}	Input Offset Current	(Note 11)	0.01		pA
				45	max
R_{IN}	Input Resistance		> 10		Tera Ω
CMRR	Common Mode Rejection Ratio	$0.7V \le V_{CM} \le 12.7V$, $V^+ = 15V$	96	63	dB
				60	min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V_O = 2.5V$	93	63	dB
				60	min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$, $V_O = 2.5V$, $V^+ = 5V$	97	74	dB
				70	min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 2.7V$, For CMRR ≥ 40 dB	−0.1	0.3	V
				0.5	max
			2.3	2.0	V
				1.7	min
		$V^+ = 3V$, For CMRR ≥ 40 dB	−0.3	0.1	V
				0.3	max
			2.6	2.3	V
				2.0	min
		$V^+ = 5V$, For CMRR ≥ 50 dB	−0.5	−0.2	V
				0.0	max
			4.5	4.2	V
				3.9	min
		$V^+ = 15V$, For CMRR ≥ 50 dB	−0.5	−0.2	V
				0.0	max
			14.4	14.0	V
				13.7	min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6035I LMC6036I Limit (Note 6)	Units
A_V	Large Signal Voltage Gain (Note 7)	R_L = 600Ω	Sourcing	1000	100	V/mV
					75	min
			Sinking	250	25	V/mV
					20	min
		R_L =2 kΩ	Sourcing	2000		V/mV
			Sinking	500		V/mV
V_O	Output Swing	V^+ = 2.7V R_L = 600Ω to 1.35V		2.5	2.0	V
					1.8	min
				0.2	0.5	V
					0.7	max
		V^+ = 2.7V R_L = 2 kΩ to 1.35V		2.62	2.4	V
					2.2	min
				0.07	0.2	V
					0.4	max
		V^+ = 15V R_L = 600Ω to 7.5V		14.5	13.5	V
					13.0	min
				0.36	1.25	V
					1.50	max
		V^+ = 15V R_L = 2 kΩ to 7.5V		14.8	14.2	V
					13.5	min
				0.12	0.4	V
					0.5	max
I_O	Output Current	V_O = 0V	Sourcing	8	4	mA
					3	min
		V_O = 2.7V	Sinking	5	3	mA
					2	min
I_S	Supply Current	LMC6035 for Both Amplifiers V_O = 1.35V		0.65	1.6	mA
					1.9	max
		LMC6036 for All Four Amplifiers V_O = 1.35V		1.3	2.7	mA
					3.0	max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Units
SR	Slew Rate	(Note 9)	1.5	V/µs
GBW	Gain Bandwidth Product	V^+ = 15V	1.4	MHz
θ_m	Phase Margin		48	°
G_m	Gain Margin		17	dB
	Amp-to-Amp Isolation	(Note 10)	130	dB
e_n	Input-Referred Voltage Noise	f = 1 kHz V_{CM} = 1V	27	$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise	f = 1 kHz	0.2	$fA/\sqrt{Hz}$
THD	Total Harmonic Distortion	f = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} V^+ = 10V	0.01	%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of 30 mA over long term may adversely affect reliabilty.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board with no air flow.

Note 5: Typical Values represent the most likely parametric norm or one sigma value.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 3.5V ≤ V_O ≤ 7.5V.

Note 8: Do not short circuit output to V^+ when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: V^+ = 15V. Connected as voltage follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

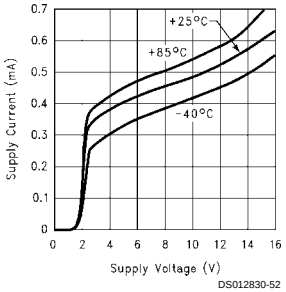
Note 10: Input referred, V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 12 V_{PP}.

Note 11: Guaranteed by design.

Typical Performance Characteristics

Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25˚C

Supply Current vs Supply Voltage (Per Amplifier)



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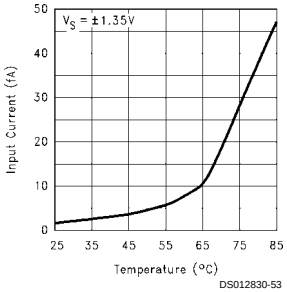
Input Current vs Temperature



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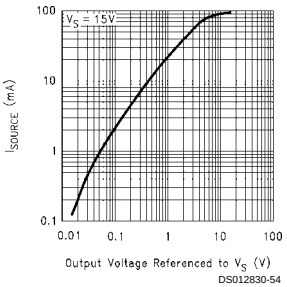
Sourcing Current vs Output Voltage



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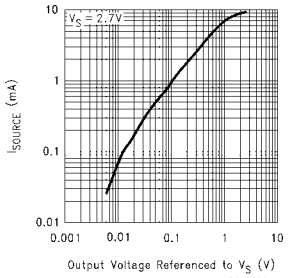
Typical Performance Characteristics

Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25˚C (Continued)

Sourcing Current vs Output Voltage



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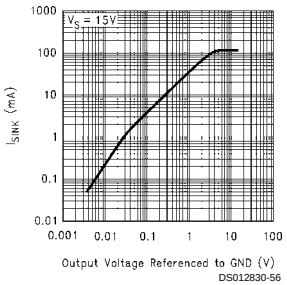
Sinking Current vs Output Voltage



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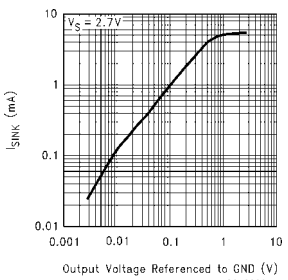
Sinking Current vs Output Voltage



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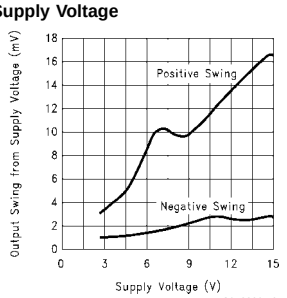
Output Voltage Swing vs Supply Voltage



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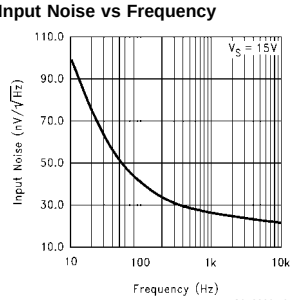
Input Noise vs Frequency



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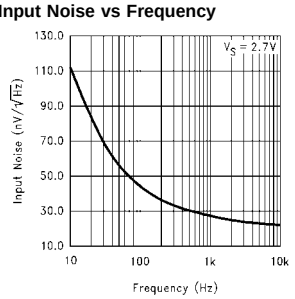
Input Noise vs Frequency



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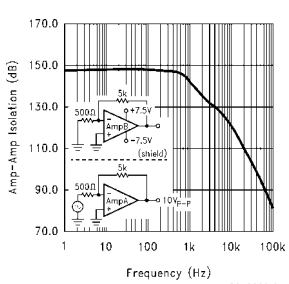
Amp to Amp Isolation vs Frequency



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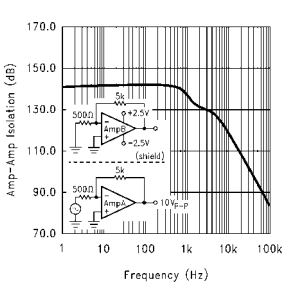
Amp to Amp Isolation vs Frequency



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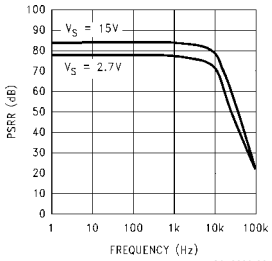
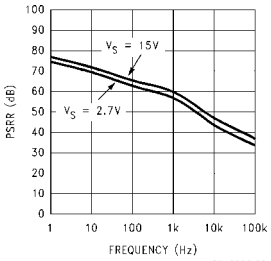
Typical Performance Characteristics Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25˚C (Continued)

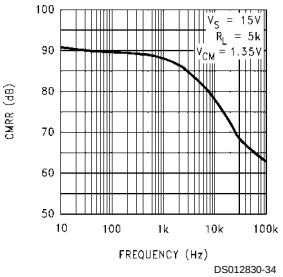
+PSRR vs Frequency



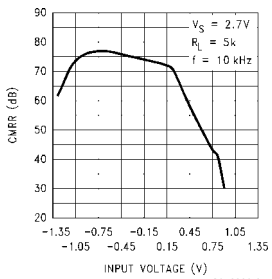
−PSRR vs Frequency



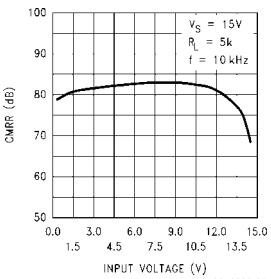
CMRR vs Frequency



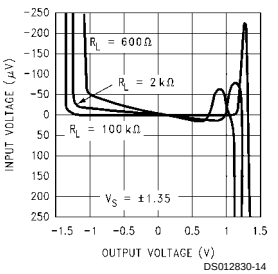
CMRR vs Input Voltage



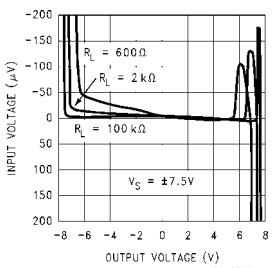
CMRR vs Input Voltage



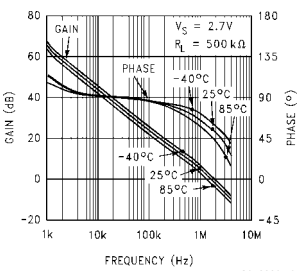
Input Voltage vs Output Voltage



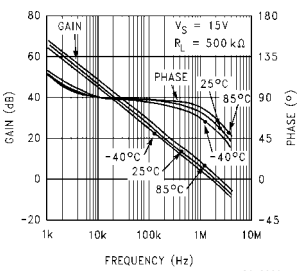
Input Voltage vs Output Voltage



Frequency Response vs Temperature

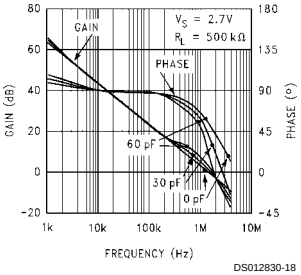


Frequency Response vs Temperature



Typical Performance Characteristics Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25˚C (Continued)

Gain and Phase vs Capacitive Load



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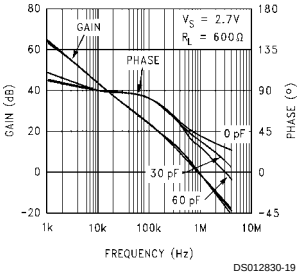
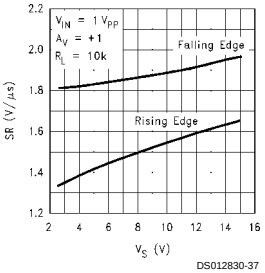
Gain and Phase vs Capacitive Load



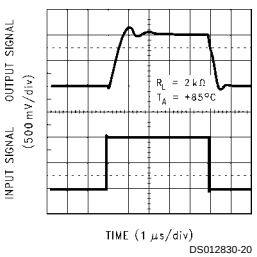
DS012830-19

Slew Rate vs Supply Voltage



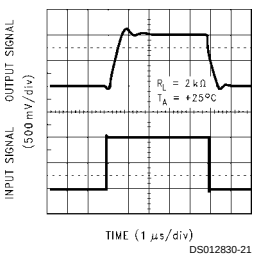
DS012830-37

Non-Inverting Large Signal Response



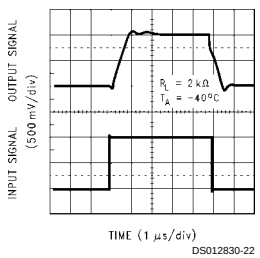
DS012830-20

Non-Inverting Large Signal Response



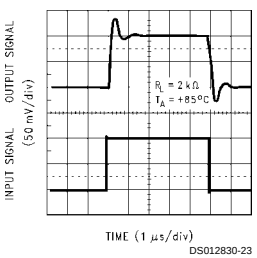
DS012830-21

Non-Inverting Large Signal Response



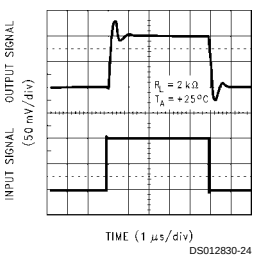
DS012830-22

Non-Inverting Small Signal Response



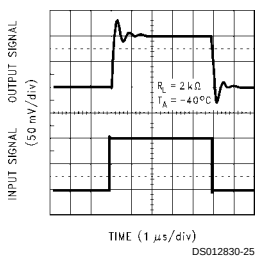
DS012830-23

Non-Inverting Small Signal Response



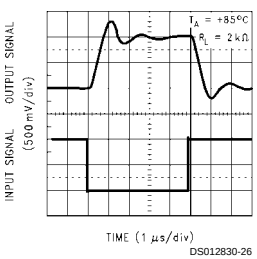
DS012830-24

Non-Inverting Large Signal Response



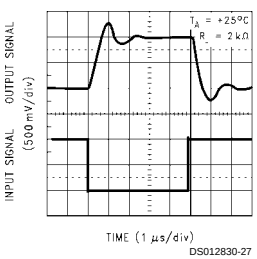
DS012830-25

Inverting Large Signal Response



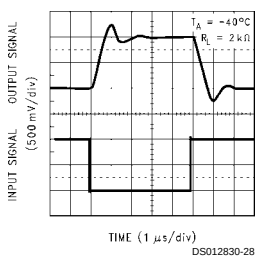
DS012830-26

Inverting Large Signal Response



DS012830-27

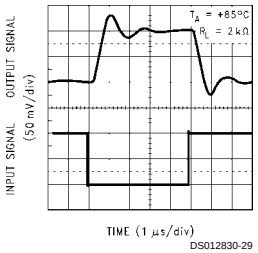
Inverting Large Signal Response



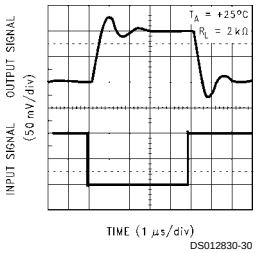
DS012830-28

Typical Performance Characteristics Unless otherwise specified, V_S = 2.7V, single supply, T_A = 25˚C (Continued)

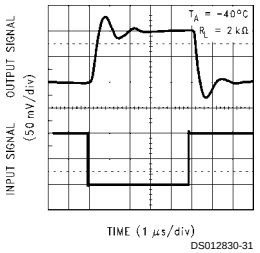
Inverting Small Signal Response



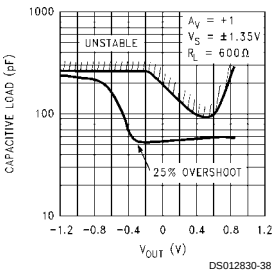
Inverting Small Signal Response



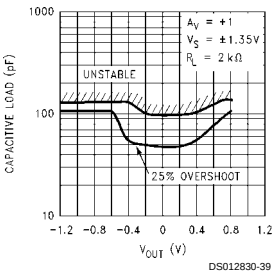
Inverting Small Signal Response



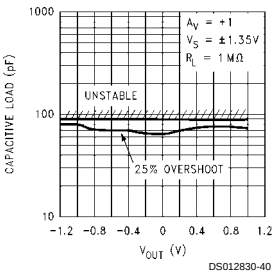
Stability vs Capacitive Load



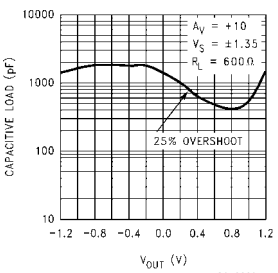
Stability vs Capacitive Load



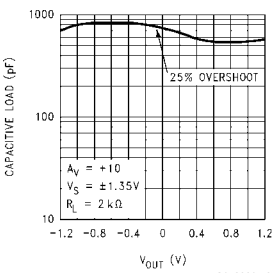
Stability vs Capacitive Load



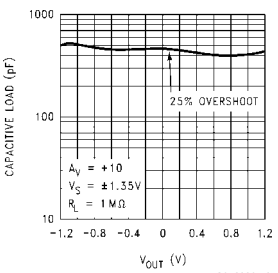
Stability vs Capacitive Load



Stability vs Capacitive Load



Stability vs Capacitive Load



1.0 Application Notes

1.1 Background

The LMC6035/6 is exceptionally well suited for low voltage applications. A desirable feature that the LMC6035/6 brings to low voltage applications is its output drive capability — a hallmark for National's CMOS amplifiers. The circuit of *Figure 1* illustrates the drive capability of the LMC6035/6 at 3V of supply. It is a differential output driver for a one-to-one audio transformer, like those used for isolating ground from the telephone lines. The transformer (T1) loads the op amps with about 600Ω of AC load, at 1 kHz. Capacitor C1 functions to block DC from the low winding resistance of T1. Although the value of C1 is relatively high, its load reactance (Xc) is negligible compared to inductive reactance (X_l) of T1.

1.0 Application Notes (Continued)

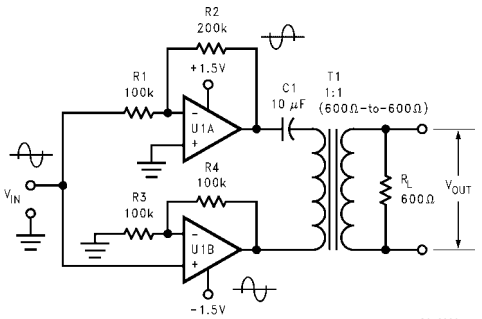


FIGURE 1. Differential Driver

The circuit in *Figure 1* consists of one input signal and two output signals. U1A amplifies the input with an inverting gain of −2, while the U1B amplifies the input with a noninverting gain of +2. Since the two outputs are 180° out of phase with each other, the gain across the differential output is 4. As the differential output swings between the supply rails, one of the op amps sources the current to the load, while the other op amp sinks the current.

How good a CMOS op amp can sink or source a current is an important factor in determining its output swing capability. The output stage of the LMC6035/6 — like many op amps — sources and sinks output current through two complementary transistors in series. This "totem pole" arrangement translates to a channel resistance (R_{dson}) at each supply rail which acts to limit the output swing. Most CMOS op amps are able to swing the outputs very close to the rails — except, however, under the difficult conditions of low supply voltage and heavy load. The LMC6035/6 exhibits exceptional output swing capability under these conditions.

The scope photos of *Figure 2* and *Figure 3* represent measurements taken directly at the output (relative to GND) of U1A, in *Figure 1*. *Figure 2* illustrates the output swing capability of the LMC6035, while *Figure 3* provides a benchmark comparison. (The benchmark op amp is another low voltage (3V) op amp manufactured by one of our reputable competitors.)

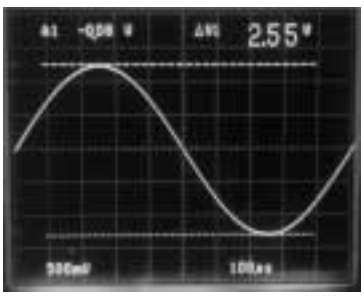


FIGURE 2. Output Swing Performance of the LMC6035 per the Circuit of *Figure 1*

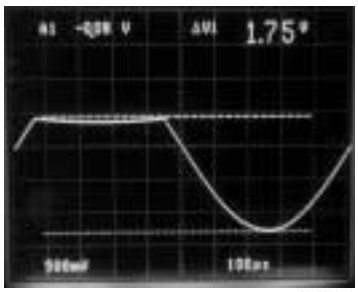


FIGURE 3. Output Swing Performance of Benchmark Op Amp per the Circuit of *Figure 1*

Notice the superior drive capability of LMC6035 when compared with the benchmark measurement — even though the benchmark op amp uses twice the supply current.

Not only does the LMC6035/6 provide excellent output swing capability at low supply voltages, it also maintains high open loop gain (A_{VOL}) with heavy loads. To illustrate this, the LMC6035 and the benchmark op amp were compared for their distortion performance in the circuit of *Figure 1*. The graph of *Figure 4* shows this comparison. The y-axis represents percent Total Harmonic Distortion (THD plus noise) across the loaded secondary of T1. The x-axis represents the input amplitude of a 1 kHz sine wave. (Note that T1 loses about 20% of the voltage to the voltage divider of R_L (600Ω) and T1's winding resistances — a performance deficiency of the transformer.)

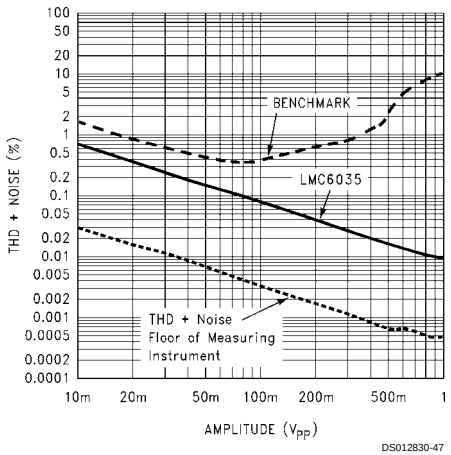


FIGURE 4. THD+Noise Performance of LMC6035 and "Benchmark" per Circuit of *Figure 1*

Figure 4 shows the superior distortion performance of LMC6035/6 over that of the benchmark op amp. The heavy loading of the circuit causes the A_{VOL} of the benchmark part to drop significantly which causes increased distortion.

1.0 Application Notes (Continued)

1.2 APPLICATION CIRCUITS

1.2.1 Low-Pass Active Filter

A common application for low voltage systems would be active filters, in cordless and cellular phones for example. The ultra low input currents (I_{IN}) of the LMC6035/6 makes it well suited for low power active filter applications, because it allows the use of higher resistor values and lower capacitor values. This reduces power consumption and space.

Figure 5 shows a low pass, active filter with a Butterworth (maximally flat) frequency response. Its topology is a Sallen and Key filter with unity gain. Note the normalized component values in parenthesis which are obtainable from standard filter design handbooks. These values provide a 1 Hz cutoff frequency, but they can be easily scaled for a desired cutoff frequency (f_c). The bold component values of *Figure 5* provide a cutoff frequency of 3 kHz. An example of the scaling procedure follows *Figure 5*.

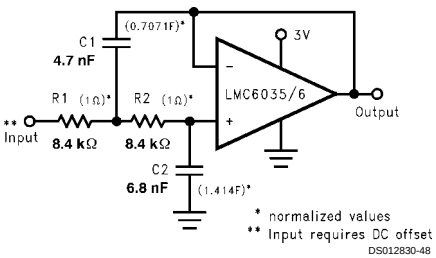


FIGURE 5. 2-Pole, 3 kHz, Active, Sallen and Key, Lowpass Filter with Butterworth Response

1.2.1.1 Low-Pass Frequency Scaling Procedure

The actual component values represented in bold of *Figure 5* were obtained with the following scaling procedure:

1. First determine the frequency scaling factor (FSF) for the desired cutoff frequency. Choosing f_c at 3 kHz, provides the following FSF computation:
   $FSF = 2\pi \times 3\ kHz_{\ (desired\ cutoff\ freq.)} = 18.84 \times 10^3$
2. Then divide all of the normalized capacitor values by the FSF as follows:
   $C1' = C_{(Normalized)}/FSF$
   $C1' = 0.707/18.84 \times 10^3 = 37.93 \times 10^{-6}$
   $C2' = 1.414/18.84 \times 10^3 = 75.05 \times 10^{-6}$
   (C1' and C2': prior to impedance scaling)
3. Last, choose an impedance scaling factor (Z). This Z factor can be calculated from a standard value for C2. Then Z can be used to determine the remaining component values as follows:

$Z = C2'/C2_{(chosen)} = 75.05 \times 10^{-6}/\mathbf{6.8\ nF} = 8.4k$

$C1 = C1'/Z = 37.93 \times 10^{-6}/8.4k = 4.52\ nF$

(Standard capacitor value chosen for C1 is **4.7 nF**)

$R1 = R1_{(normalized)} \times Z = 1\Omega \times 8.4k = 8.4\ k\Omega$

$R2 = R2_{(normalized)} \times Z = 1\Omega \times 8.4k = 8.4\ k\Omega$

(Standard value chosen for R1 and R2 is **8.45 kΩ**)

1.2.2 High Pass Active Filter

The previous low-pass filter circuit of *Figure 5* converts to a high-pass active filter per *Figure 6*.

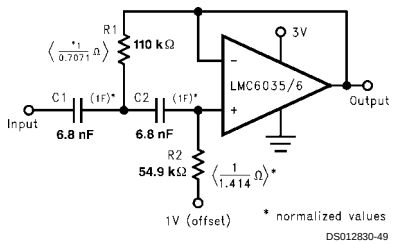


FIGURE 6. 2 Pole, 300 Hz, Sallen and Key, High-Pass Filter

1.2.2.1 High-Pass Frequency Scaling Procedure

Choose a standard capacitor value and scale the impedances in the circuit according to the desired cutoff frequency (300 Hz) as follows:

C = C1 = C2

$Z = 1\ Farad/C_{(chosen)} \times 2\pi \times (desired\ cutoff\ freq.)$
$= 1\ Farad/\mathbf{6.8\ nF} \times 2\pi \times 300\ Hz = 78.05k$

$R1 = Z \times R1_{(normalized)} = 78.05k \times (1/0.707) = 110.4\ k\Omega$

(Standard value chosen for R1 is **110 kΩ**)

$R2 = Z \times R2_{(normalized)} = 78.05k \times (1/1.414) = 55.2\ k\Omega$

(Standard value chosen for R1 is **54.9 kΩ**)

1.2.3 Dual Amplifier Bandpass Filter

The dual amplifier bandpass (DABP) filter features the ability to independently adjust f_c and Q. In most other bandpass topologies, the f_c and Q adjustments interact with each other. The DABP filter also offers both low sensitivity to component values and high Qs. The following application of *Figure 7*, provides a 1 kHz center frequency and a Q of 100.

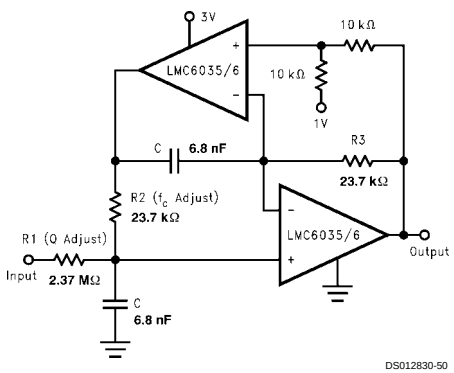


FIGURE 7. 2 Pole, 1 kHz Active, Bandpass Filter

1.2.3.1 DABP Component Selection Procedure

Component selection for the DABP filter is performed as follows:

1.0 Application Notes (Continued)

1. First choose a center frequency (f_c). *Figure 7* represents component values that were obtained from the following computation for a center frequency of 1 kHz.
   R2 = R3 = 1/(2 πf_cC)
   Given: f_c = 1 kHz and $C_{(chosen)}$ = **6.8 nF**
   R2 = R3 = 1/(2π x 3 kHz x 6.8 nF) = 23.4 kΩ
   (Chosen standard value is **23.7 kΩ**)
2. Then compute R1 for a desired Q (f_c/BW) as follows:
   R1 = Q x R2.
   Choosing a Q of 100,
   R1 = 100 x 23.7 kΩ = **2.37 MΩ.**

1.3 PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with < 1000 pA of leakage current requires special layout of the PC board. If one wishes to take advantage of the ultra-low bias current of the LMC6035/6, typically < 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may at times appear acceptably low. Under conditions of high humidity, dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6035 or LMC6036 inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op amp's inputs. See *Figure 8*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the amplifiers actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figure 9a, b, c* for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 9d*.

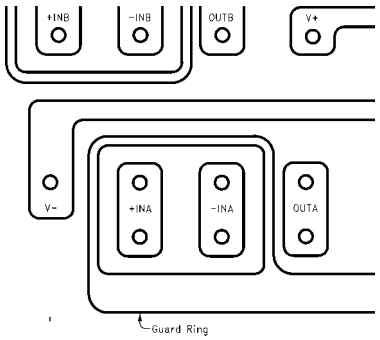
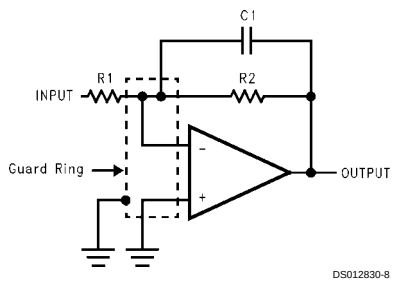
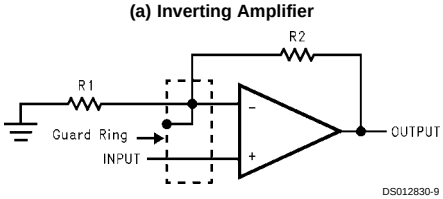


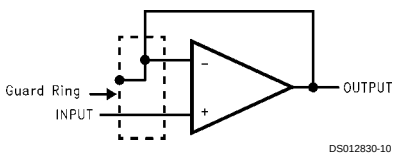
FIGURE 8. Example, using the LMC6036 of Guard Ring in P.C. Board Layout



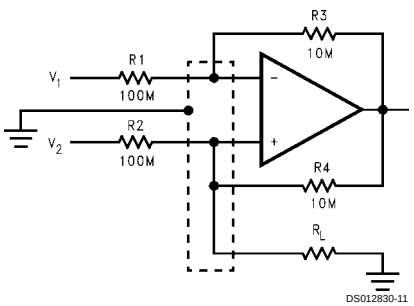
(a) Inverting Amplifier



(b) Non-Inverting Amplifier



(c) Follower



(d) Howland Current Pump

FIGURE 9. Guard Ring Connections

1.0 Application Notes (Continued)

1.3.1 CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6035/6 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in *Figure 10*, the addition of a small resistor (50Ω–100Ω) in series with the op amp's output, and a capacitor (5 pF–10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

1.4 µSMD Considerations

Contrary to what might be guessed, the µSMD package does not follow the trend of smaller packages having higher thermal resistance. LMC6035 in WLCS has thermal resistance of 220˚C/W compared to 230˚C/W in MSOP. Even when driving a 600Ω load and operating from ±7.5V supplies, the maximum temperature raise will be under 4.5˚C. For application information specific to µSMD, see Application note AN-1112.

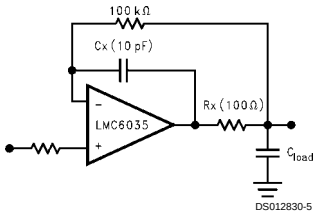


FIGURE 10. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 11*). Typically a pull up resistor conducting 500 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

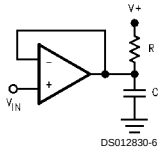
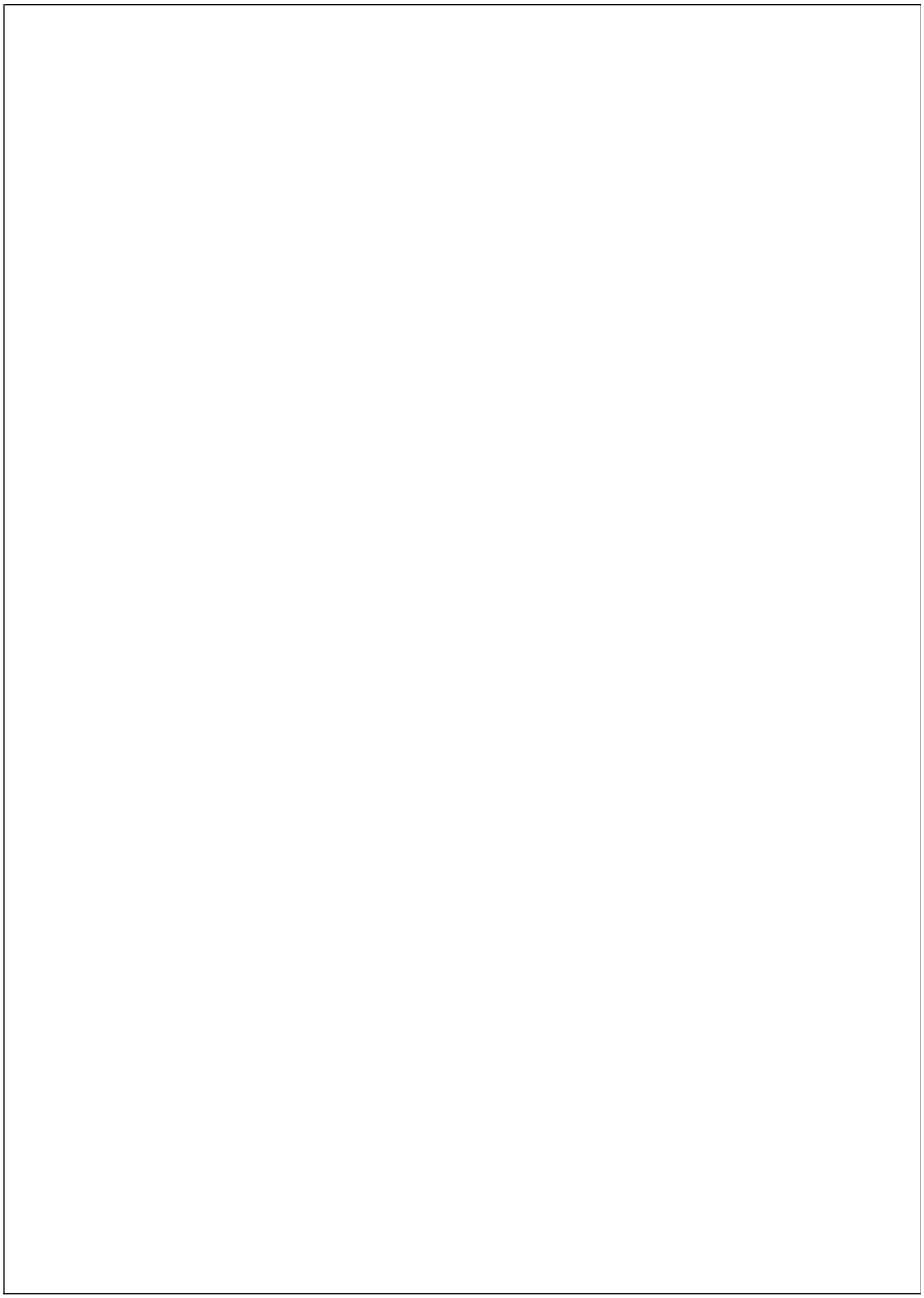
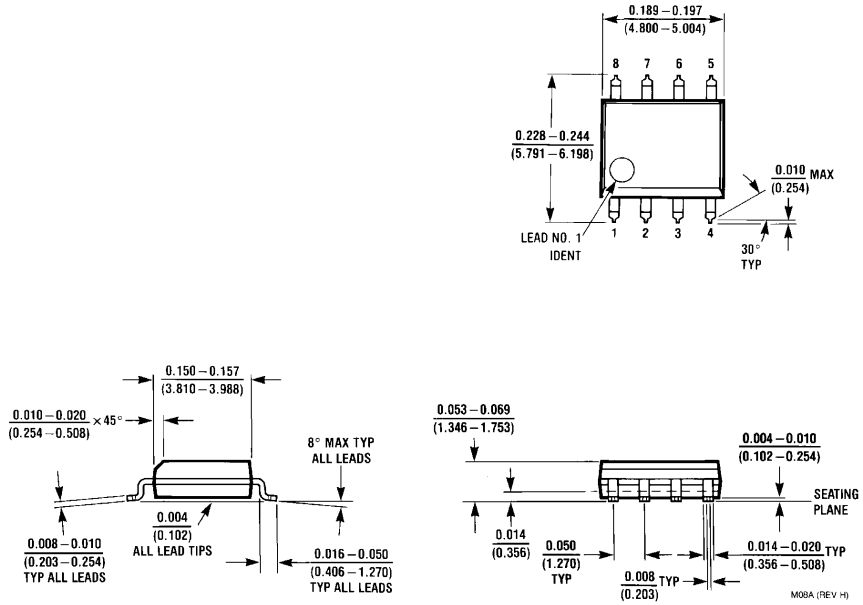


FIGURE 11. Compensating for Large Capacitive Loads with a Pull Up Resistor



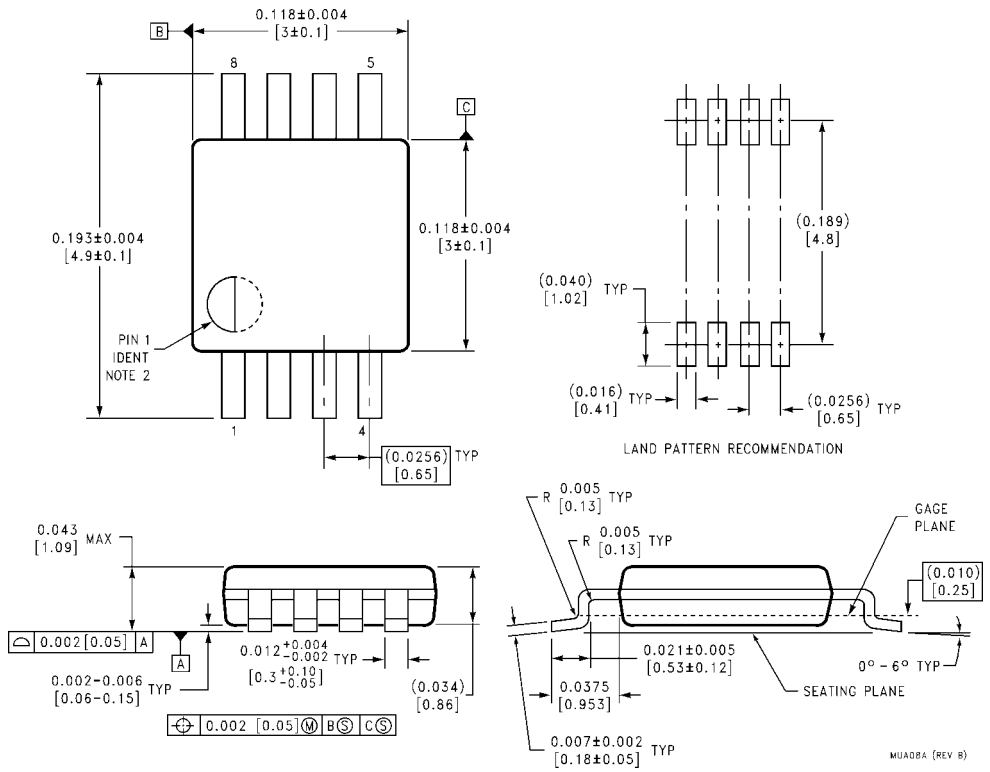
14

Physical Dimensions inches (millimeters) unless otherwise noted



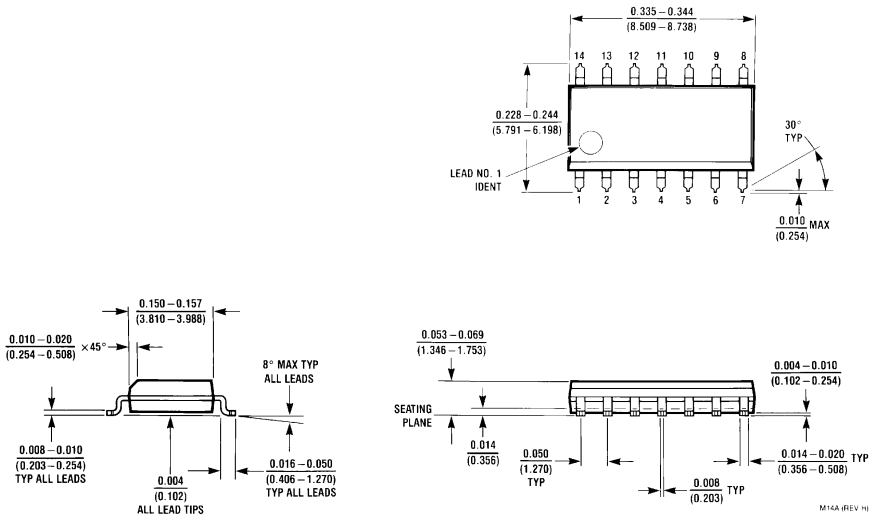
8-Lead (0.150" Wide) Molded
Small Outline Package, JEDEC
Order Number LMC6035IM or LMC6035IMX
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



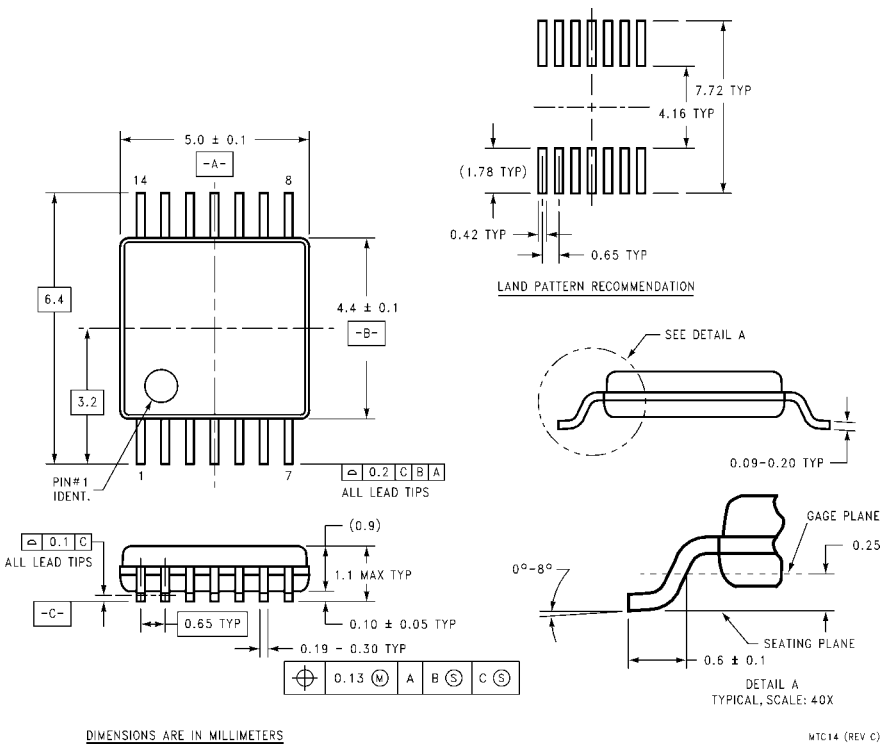
8-Lead (0.150" Wide) Molded
Mini Small Outline Package, JEDEC
Order Number LMC6035IMM or LMC6035IMMX
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



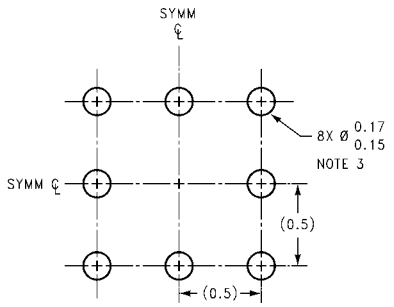
14-Lead (0.150" Wide) Molded
Small Outline Package, JEDEC
Order Number LMC6036IM or LMC6036IMX
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

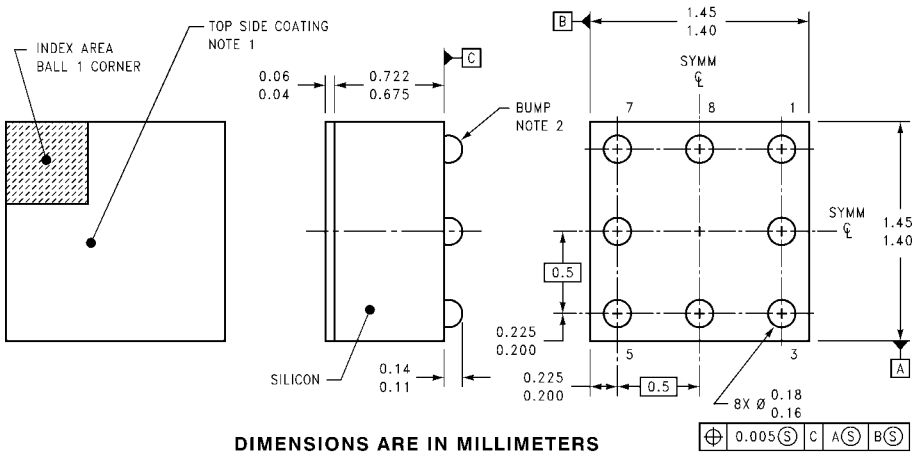


14-Pin TSSOP
Order Number LMC6036IMT or LMC6036IMTX
NS Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING.
2. 63Sn/Pb EUTECTIC BUMP.
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. NO JEDEC REGISTRATION AS OF FEB, 1998.

SWA08A (REV. B)

8-Bump WLCS
Order Number LMC6035IBP or LMC6035IBPX
NS Package Number SWA08A

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

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Tel: 81-3-5620-6175
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3.0 PROCESS INFORMATION

3.1 Process Outline

Fabrication Site: Greenock, Scotland
Process Technology: P2CMOS (double silicon poly gate CMOS)
Minimum Feature Size: 4microns
Wafer Diameter: 6inches
Number of Masks: 17 (including bump assembly)
Metallization: Single Layer Aluminum
Active Side Passivation: Nitride (11,000Å thick) over VOM (5000Å thick) with 2nd Passivation covering the Nitride/VOM
Metallization: Single Layer Aluminum (12,000Å thick)

3.2 Process Detail & Masks

1: Initial Oxide
2: **Mask 1.0**, P-
3: P- Implant
4: **Mask 1.4**, N-
5: N- Implant
6: P- Drive
7: Field Oxide
8: **Mask 2.0**, Composite
9: Etch
10: **Mask 3.0**, N- Field Implant
11: N- Field Implant
12: **Mask 4.0**, P- Field Implant
13: P- Field Implant
14: Field Oxide
15: Etch
16: Gate Oxide
17: **Mask 5.0**, Vtp
18: Vtp Implant
19: **Mask 5.3**, P-Deplete
20: P-Deplete Implant
21: Poly Dep
22: Back Etch
23: Poly Dope
24: **Mask 6.0**, Poly1
25: Etch
26: **Mask 7.0**, P+S/D Implant
27: P+ Implant
28: **Mask 8.1**, N+S/D Implant
29: N+ Implant1
30: **Mask 8.2**, N+S/D Implant
31: N+ Implant2
32: Rapid Thermal Anneal
33: Poly Reox
34: Poly Dep
35: Back Etch
36: Poly Dope
37: **Mask 9.0**, Poly2
38: Etch
39: Field Vapox
40: **Mask 10.2**, Contact
41: Etch
42: Ox Reflow
43: Metal Dep
44: **Mask 11.0**, Metal
45: Etch
46: Alloy
47: VOM
48: Nitride
49: **Mask 12.0**, Passivation
50: Etch
51: Final Alloy
52: Ship To Bump Assembly Processing

4.0 PACKAGING INFORMATION

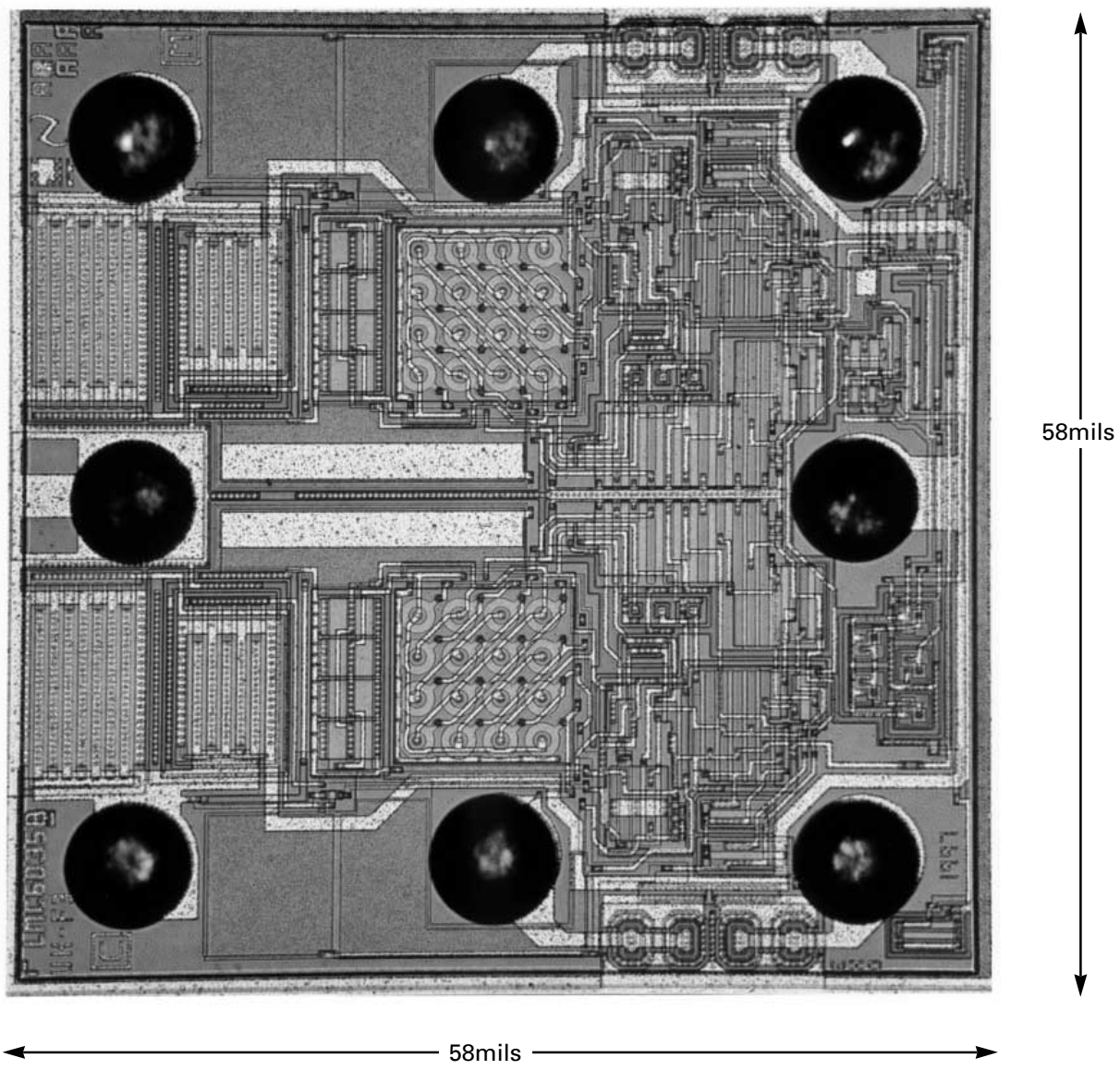
4.1 Package Material

Generic Package Type	**µSMD**
NS Package Number	SWA08A
Package Material Type	8 bump Wafer-Level Chip-Scale (WLCS)
Bump Material	Eutectic Solder (63%Sn/37%Pb)
Bump Mechanical:	
Stress Buffer Material (Active Side of Die)	2nd Passivation
Back Side Coating Material (Non-Active Side of Die)	Epoxy
Package Thermal	220°C/W

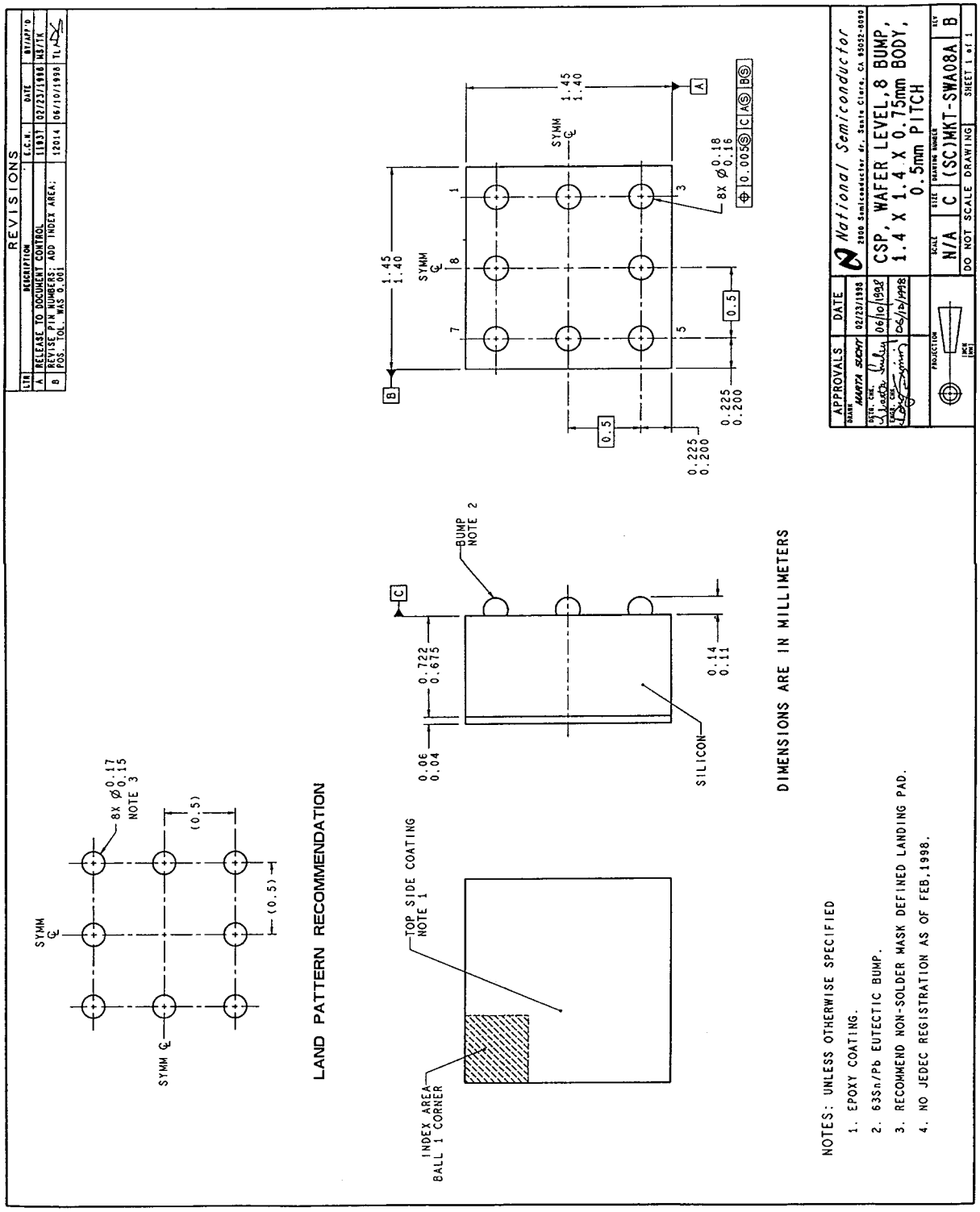
4.2 Assembly Flow

1: Receive Into Bump Assembly Processing	[wafer level]
2: 2nd Passivation	[wafer level]
3: Passivation Mask	[wafer level]
4: Passivation Etch	[wafer level]
5: UBM (under bump metal) Application	[wafer level]
6: UBM Etch	[wafer level]
7: Solder Bump Application	[wafer level]
8: Solder Bump Reflow	[wafer level]
9: Epoxy Back Side	[wafer level]
10: Laser Mark Back Side	[wafer level]
11: Electric Test	[wafer level]
12: Saw Scribe Singulation	[wafer level]
13: Pack in Tape/Reel	[individual part level]

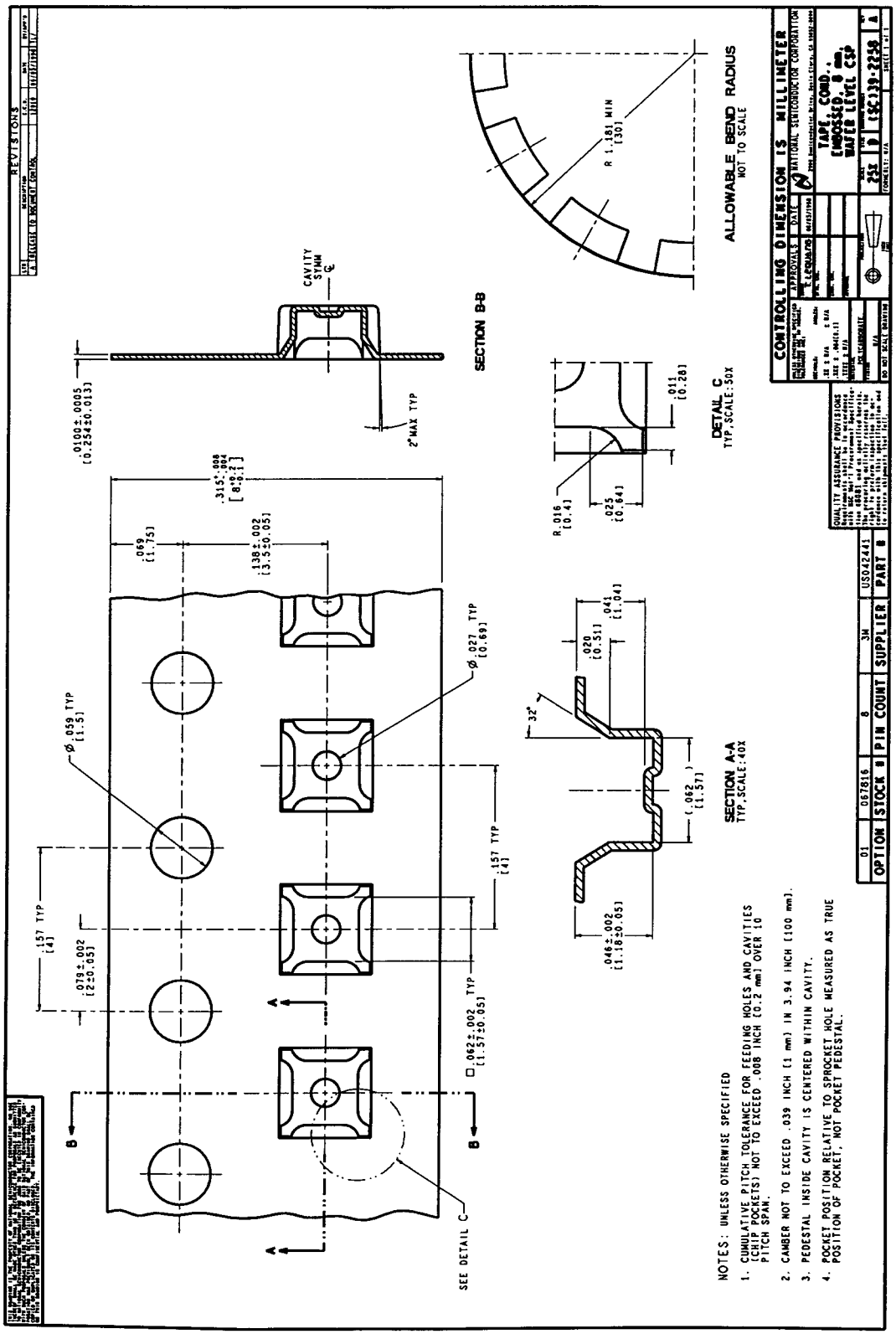
4.3 Die Photo



4.4 Package Dimensions



4.5 Tape & Reel Dimensions



5.0 RELIABILITY DATA

National Semiconductor

Date: August 18, 1998

Reliability Test Report

Purpose

To qualify the new µSMD Micro Surface Mount Device which is an 8 bump wafer level chip scale package - SWA08A - using the LMC6035 die fabricated in UK.

Approvals

Reliability Engineer

Mgr Ref Engineering

Reference File Numbers

RSC199801484	
RSC199801076	RSC199801052
RSC199800814	RSC199801367
RSC199800908	RSC199801366

Distribution List

Abstract

The Micro Surface Mount Device (µSMD) is a version of a wafer level chip scale package where the package size is the same as that of the die. Electrical connection to the outside world is made through solder bump construction on the Aluminum bond pad, where the die is flipped to solder on to the printed circuit board. The die passivation and the 2nd Passivation, along with the solder bumps forms a protective barrier for the active area of the die from outside world contaminants. An Epoxy back coat done to the backside of the die is used for marking.

The LMC6035 is re-laid out so as to provide necessary spacing between the bond pads that enables proper surface mounting of this die. To qualify this new die, 3 die runs assembled in MDIP will be subjected to OPL 150C. Using one die run, 3 lots of the µSMD devices will be fabricated. All tests except TMCL will be done on these devices mounted on conversion boards. Two TMCL evaluations will be conducted over different temperature ranges since the capability of this package has not yet been established. The devices undergoing TMCL, and THBT will be level 1 preconditioned.

Assembly of µSMD devices will be done at EM.

Solder joint reliability study will be performed with daisy chain configuration of µSMD devices. TMCL (0/100C) will be performed on these daisy chained devices (as per IPC specification IPC-SM-785).

Description

Test Request	Device Name	Sbgp	Wafer Die Run	Fab Loc	Fab Line	Pkg Code	# Leads	Assy Loc	Date Cd	Mold C
RSC199800814	LMC6035	A	W#01	UK		SWA08A	8	EM		Epoxy globtop
RSC199800814	LMC6035	B	W#09	UK		SWA08A	8	EM		Epxoy globtop
RSC199800814	LMC6035	C	W#10	UK		SWA08A	8	EM		Epxoy globtop
RSC199800908	LMC6035	A	JM087R26A	UK		SWA08A	8	EM		Epoxy globtop
RSC199800908	LMC6035	B	JM087R26A	UK		SWA08A	8	EM		Epxoy globtop
RSC199800908	LMC6035	C	JM087R26A	UK		SWA08A	8	EM		Epxoy globtop
RSC199801052	LMC6035	A		UK		SWA08A	8	EM		Epoxy globtop
RSC199801052	LMC6035	B		UK		SWA08A	8	EM		Epxoy globtop
RSC199801052	LMC6035	C		UK		SWA08A	8	EM		Epxoy globtop
RSC199801076	LMC6035N	A	JM087R26	UK		N\MDIP	8	EM	9812	B8
RSC199801076	LMC6035N	B	JM087V42	UK		N\MDIP	8	EM	9812	B8
RSC199801076	LMC6035N	C	JM088V53	UK		N\MDIP	8	EM	9812	B8
RSC199801484	LMC6035	A		UK		SWA08A	8	EM		Epoxy globtop
RSC199801484	LMC6035	B		UK		SWA08A	8	EM		Epxoy globtop
RSC199801484	LMC6035	C		UK		SWA08A	8	EM		Epxoy globtop

5.0 RELIABILITY DATA

Tests Performed

1. Preconditioning-IB1
   a. temp cycle - 5 cycles at -40/60C
   b. bake - 16 hours at 125C
   c. moisture sensitivity level 1 - moisture soak for 168 hours at 85C and 85%RH
   d. IR reflow 235C 3 passes
   e. Flux immersion
   f. clean

2. ESD - Five units for each level.
   a. Human Body Model = 1000V, 1500V, 2000V, 2500V, 3000V, 3500V
   b. Machine Model = 50V, 100V, 200V, 300V , 350V, 400V

3. Latch-Up Testing - Six units passed for each level.
   a. 200ma at 25C, µSMD package, 200ma at 85C MDIP, 200ma at 125C MDIP

4. Test: Operating Life Test (Static) (SOPL) (150C, static bias, ckt 2526RE-B1) - Release at 500 hours.

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199800908	LMC6035	A	0	0	150	0
RSC199800908	LMC6035	B	0	0	150	0
RSC199800908	LMC6035	C	0	0	150	0
RSC199801076	LMC6035N	A	0	0	150	0
RSC199801076	LMC6035N	B	0	0	150	0
RSC199801076	LMC6035N	C	0	0	150	0

5. Test: Temperature Cycle (TMCL)) (-65 to +150C, air-air, unbiased) - Release at 500 cycles.

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199801484	LMC6035	A	0	0	150	-65
RSC199801484	LMC6035	B	0	0	150	-65
RSC199801484	LMC6035	C	0	0	150	-65

6. Test: Temperature Cycle (TMCL)) (-40 to +125C, air-air, unbiased) - Release at 1440 cycles.

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199801052	LMC6035	A	0	0	125	-40
RSC199801052	LMC6035	B	0	0	125	-40
RSC199801052	LMC6035	C	0	0	125	-40

7. Test: Daisy Chain Temperature Cycle (TMCL)) (0 to +100C per IPC specification IPC-SM-785) - Release at 1000 cycles.

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
0605 Daisy Chain	A	0	0	100	0	

8. Test: Daisy Chain Temperature Cycle (TMCL)) (-40 to +125C per IPC specification IPC-SM-785) - For information only.

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
0605 Daisy Chain	A	0	0	125	-40	

9. Test: Temperature Humidity Bias Test (THBT) (85C, 85% RH, Biased, ckt 2161RE-A) - Release at 500 hours.

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199800814	LMC6035	A	85	0	85	0
RSC199800814	LMC6035	B	85	0	85	0
RSC199800814	LMC6035	C	85	0	85	0

Table Showing Results after Reliability Tests for Qualification

LMC6035 µSMD wafer level chip scale package Qualification					
Tests	**Time/Cycles**	**Sbgrp A**	**Sbgrp B**	**Sbgrp C**	**Status**
SOPL - µSMD	168	0/77	0/77	0/77	Passed
	500	0/77	0/77	0/77	Passed
SOPL - MDIP	168	0/77	0/77	0/77	Passed
	500	0/77	0/77	0/77	Passed
	1000	0/77	0/77	0/77	Passed
THBT - µSMD	168	0/77	0/77	0/77	Passed
	500	0/77	0/77	0/77	Passed
	1000	0/77	0/77	0/77	Passed
TMCL - µSMD	500	0/80	0/80	0/79[1]	Passed
-40C to 125C	1440	0/80	0/80	0/79	Passed
TMCL - µSMD -65C to 150C	500	0/80	0/80	0/80	Passed
TMCL - Daisy Chain 0C to 100C	500	0/62			Passed
	1000	0/62			Passed
	2300	0/62			Passed
TMCL - Daisy Chain -40C to +125C	800	0/61			Information only

Table Showing Results of ESD and Latch-Up Tests for Qualification

LMC6035 µSMD wafer level chip scale package Qualification					
Tests	**Levels**				**Status**
ESD - HMB (rejects/tested)	2000V 0/5	2500V 0/5	3000V 0/5	3500V 5/5	Passed to 3000V
ESD - MM (rejects/tested)	200V 0/5	250V 0/5	300V 0/5	350V 2/5	Passed to 300V
Latch-Up (rejects/tested)	25C - µSMD 0/6	85C - MDIP 0/6	125C - MDIP 0/6		Passed to 125C

Notes

TMCL - µSMD

[1]Unit was lost. Since the TMCL parts were not mounted on conversion boards they are very difficult to handle due to their small size and one unit was lost. No corrective action is necessary.

Conclusion

The wafer level chip scale package SWA08A has passed the SOPL, TMCL, and THBT legs using the LMC6035 die. The package/part also passed ESD and Latch-Up.

Appendix: Board Level Testing

In addition to above device level and mechanical joint integrity reliability, the following board level testing was done.

1. Drop Test, 3 mutually exclusive axes from height of 750 mm onto non-cushioning vinyl tile surface
2. Three-Point Bend Test, test board span of 100 mm with cross-head speed of 9.45 mm/min and 25 mm deflection
3. Sinusoidal Vibration Test, frequency sweep of 260 Hz to 320 Hz for board response of 20 G to 40 G
4. Random Vibration Test, 2 G RMS with frequencies from 20 Hz to 2,000 Hz

6.0 CHARACTERIZATION DATA

6.1 Parametric Data (Room Temperature, Key Tests)

Test Name	Units	Min	Mean	Max
Supply Current, 2.7V	mA	0.35	0.51	0.69
Input Offset Voltage A, 2.7V	mV	-3.04	-0.12	2.85
Input Offset Voltage B, 2.7V	mV	-3.99	-0.13	3.47
Pos Output Swing A, 2.7V, 600Ω	V	2.38	2.45	2.48
Pos Output Swing B, 2.7V, 600Ω	V	2.28	2.45	2.48
Pos Output Swing A, 2.7V, 2kΩ	V	2.59	2.62	2.63
Pos Output Swing B, 2.7V, 2kΩ	V	2.55	2.62	2.63
Pos Output Swing A, 15V, 2kΩ	V	14.77	14.82	14.84
Pos Output Swing B, 15V, 2kΩ	V	14.79	14.82	14.84
Pos Output Swing A, 15V, 600Ω	V	14.29	14.44	14.51
Pos Output Swing B, 15V, 600Ω	V	14.34	14.44	14.51
Neg Output Swing A, 2.7V, 600Ω	V	0.21	0.23	0.26
Neg Output Swing B, 2.7V, 600Ω	V	0.21	0.23	0.26
Neg Output Swing A, 2.7V, 2kΩ	V	0.066	0.074	0.082
Neg Output Swing B, 2.7V, 2kΩ	V	0.066	0.074	0.082
Neg Output Swing A, 15V, 2kΩ	V	0.13	0.14	0.18
Neg Output Swing B, 15V, 2kΩ	V	0.13	0.14	0.16
Neg Output Swing A, 15V, 600Ω	V	0.41	0.44	0.57
Neg Output Swing B, 15V, 600Ω	V	0.41	0.44	0.49

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