National Semiconductor

ADVANCED INFORMATION
February 1997

PT80C525
PicoPower NILE-II Advanced PCI-to-PCI Bridge Interface Controller

General Description

NILE-II PT80C525 is a high-performance Microsoft® Windows® 95-compatible PCI-to-PCI bridge interface controller for portable and desktop systems. It is compliant with the PCI Local Bus Specification Revision 2.1 and the PCI-to-PCI Bridge Specification Revision 1.0.

A high performance PCI-to-PCI bridge, the NILE-II expands the bus mastering and the bus loading capabilities of the PCI Local bus in portable or desktop systems. By implementing support for SmartDock™ II technology, Distributed DMA, and Serial IRQ Specifications, NILE-II becomes a docking PCI-to-PCI bridge to enable hot-, warm-, and cold-docking on the PCI bus. It complements National Semiconductor's VESUVIUS-LS system controller to offer a cost-effective, high performance solution for portable computers with docking stations.

The primary function of NILE-II is to allow transactions to occur between a master on one PCI bus and a target on the other PCI bus. NILE-II allows system designers to overcome electrical loading limits by creating hierarchical PCI buses. The two PCI buses can operate concurrently; a master and a target on the same PCI bus can communicate even if the other PCI bus is busy. NILE-II can thus isolate traffic between devices on one bus from devices on other PCI buses, enhancing overall system performance.

NILE-II functions as a transparent or full bridge: In transparent mode, NILE-II provides a single logical bus with devices on both primary and secondary buses configured by the same Type 0 configuration cycle. The NILE-II register set maintains backward compatibility with NILE PT80C524. The eight-deep buffers within NILE-II allow concurrency by default, thus enhancing the system performance. In full bridge mode, NILE-II creates a new, independent hierarchical PCI bus and implements the configuration space adhering to the PCI-to-PCI bridge header format. The BIOS fully programs NILE-II registers and the operating system performs bus enumeration. As in transparent mode, the data buffers are enabled by default and allow concurrent bus operation.

NILE-II incorporates patent-pending SmartDock docking technology to enable true hot-docking, a significantly superior solution to current cold- and warm-docking methods. With true hot-docking, a portable can be inserted into a docking station while still running. Since the portable computer does not have to be rebooted to activate automatic reconfiguration, true hot docking offers a quick and easy migration to mobile computing with performance and flexibility which parallels a desktop computer.

The NILE-II system block diagrams illustrate typical applications in (1) a dual-ISA system attached to a docking station, and (2) a desktop system. NILE-II has two interfaces: (i) a primary interface that is connected to the PCI bus closest to the CPU (primary PCI bus), and (ii) a secondary interface that is connected to the PCI bus farthest from the CPU (secondary PCI bus). Each interface is capable of passing master operations or receiving target operations.

NILE-II functions as a target on the initiating bus on behalf of the target that actually resides on the target bus. Similarly, NILE-II functions as master on the target bus on behalf of the master that actually resides on the initiating bus.

NILE-II is available in a space-efficient 176-pin VQFP package. The device comes with full technical and hardware support, including samples, evaluation boards, and design examples in OrCAD®.

Features

- Ideal PCI-to-PCI solution to support hot docking, server, desktop, and add-on peripheral card designs
- Fully compliant with the PCI Local Bus Specification Revision 2.1
- Fully compliant with PCI-to-PCI Bridge Architecture Specification Revision 1.0
- SmartDock II docking technology (patent-pending) enables true hot docking
- Supports Microsoft Windows 95 Plug-and-Play capabilities, including "Eject PC"
- Supports programmable subtractive or positive decoding for downstream and upstream transactions
  - — Eight programmable I/O or Memory Base/Limit Address registers providing positive programmable windows for either downstream or upstream transactions
  - — Each base and limit address register is software-enabled and can be configured to decode I/O or memory accesses for upstream or downstream transactions
  - — Supports up to 64 Kbyte of I/O space with 1-byte alignment and granularity for upstream or downstream transactions
  - — Supports up to 4 Gbytes of memory space with 1-Mbyte alignment and granularity for upstream or downstream transactions
  - — Fourteen software-enabled hardwired memory locations for upstream cycles
  - — Software-enabled hardwired I/O ranges to support audio, network and super I/O for downstream cycles
- Supports multiple NILE-II devices in either serial- or parallel-port configuration
- Registers maintain backward-compatibility with NILE
- Fully optimized for VESUVIUS-LS and V-PLUS
- Supports two 32-bit PCI buses
- Supports Bus 0-to-Bus 0 and Bus 0-to-Bus 1 configuration modes

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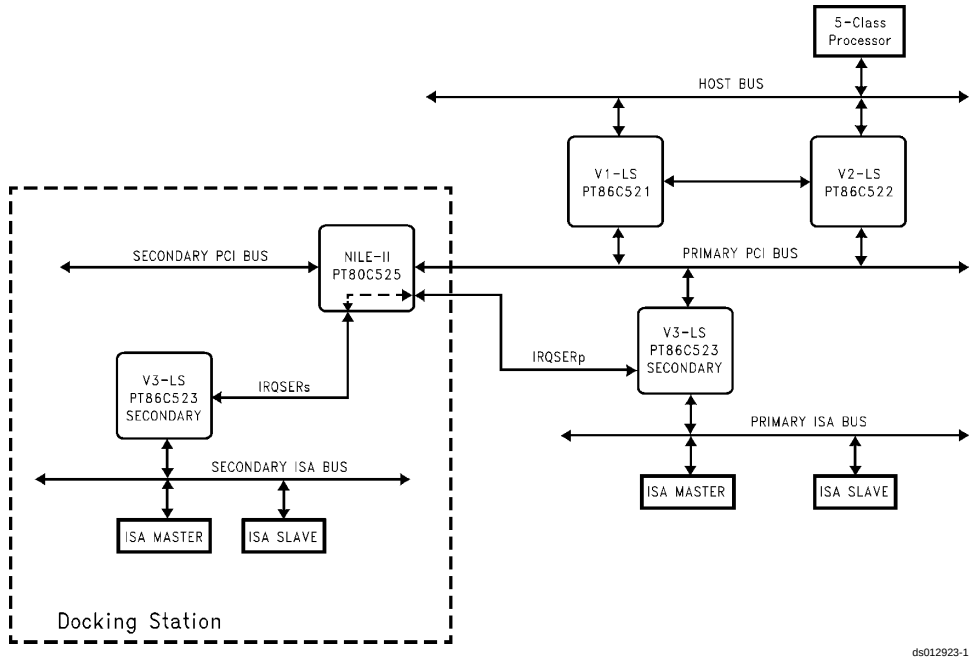
PrintDate=1997/02/08 PrintTime=09:37:45 ds012923 Rev. No. 4 **Final**

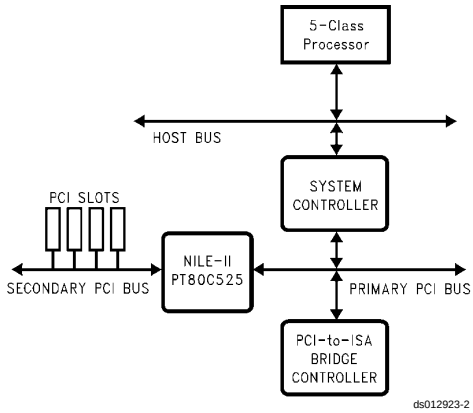
Features (Continued)

- Supports concurrent cycles on the primary and secondary buses
- Supports VGA-compatible devices on secondary PCI bus
- Supports early cycle start (speculative cycle)
- Supports up to 3-1-1-1 write bursting snd 5-1-1-1 read bursting on the primary and secondary buses to enable 120 Mbyte per second sustained PCI bandwidth
- Eight independent 32-bit—one Dword-wide—buffers in each direction
  - — Used simultaneously for posted memory writes and read pre-fetches
  - — Continuous read pre-fetching on both downstream and upstream transactions
- Supports secondary interface arbiter
  - — Supports six REQ#/GNT# pairs
  - — Supports programmable, pre-emptable, and non-pre-emptable bus requests
  - — Secondary bus parking
- Serial IRQ protocol to support interrupts in a dual-ISA system
- Supports Distributed DMA (Direct Memory Access) protocol
- Propagates and maintains locks upstream and downstream in flow-through mode
- Software-enabled data parity checking and reporting
- Software-enabled forwarding of system errors across the NILE-II bridge
- Supports fast back-to-back cycles as a target
- Supports 33-MHz synchronous clocks for the primary and secondary buses
- Integrated PLL (Phase-Locked Loop) with four secondary PCI clock pins
- 3.3-V core device with 5-V tolerance on primary and secondary PCI interfaces
- Supports one PCI clock latency for signals forwarded across the NILE-II device
- Available in a space-efficient 176-pin VQFP package

System Block Diagram
Portable Computer with Docking Station



System Block Diagram
Desktop System



Physical Dimensions inches (millimeters)

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