National Semiconductor

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MM54C164/MM74C164
8-Bit Parallel-Out Serial Shift Register

General Description

The MM54C164/MM74C164 shift registers are a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. These 8-bit shift registers have gated serial inputs and clear. Each register bit is a D-type master/slave flip-flop. A high-level input enables the other input which will then determine the state of the flip-flop.

Data is serially shifted in and out of the 8-bit register during the positive going transition of clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input. All inputs are protected against electrostatic effects.

Features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)
■ Medium speed operation	0.8 MHz (typ.) with 10V supply

Applications

- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

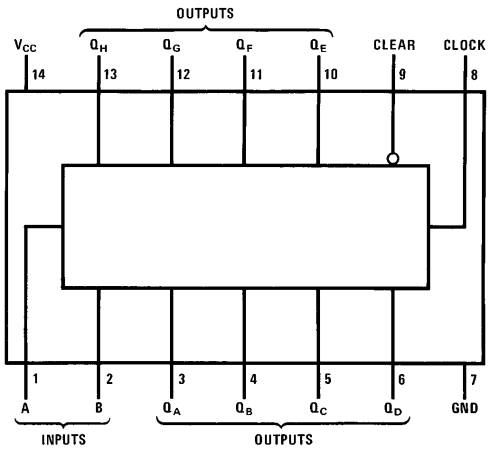
Truth Table

Serial Inputs A and B

Inputs t_n		Output t_n+1
A	B	Q_A
1	1	1
0	1	0
1	0	0
0	0	0

Connection Diagram

Dual-In-Line Package

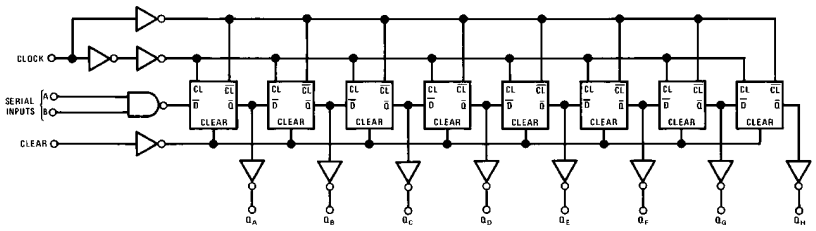


TL/F/5896–2

Top View

Order Number MM54C164 or MM74C164

Block Diagram



TL/F/5896–1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C164	$-55°C$ to $+125°C$
MM74C164	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Absolute Maximum V_{CC}	18V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Lead Temperature (soldering, 10 sec.)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_O = -10\ \mu A$ $V_{CC} = 10V$, $I_O = -10\ \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$, $I_O = +10\ \mu A$ $V_{CC} = 10V$, $I_O = +10\ \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS TO LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = -360\ \mu A$ 74C $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = 360\ \mu A$ 74C $V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5V$, $V_{IN(1)} = 5V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V$, $V_{IN(1)} = 10V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

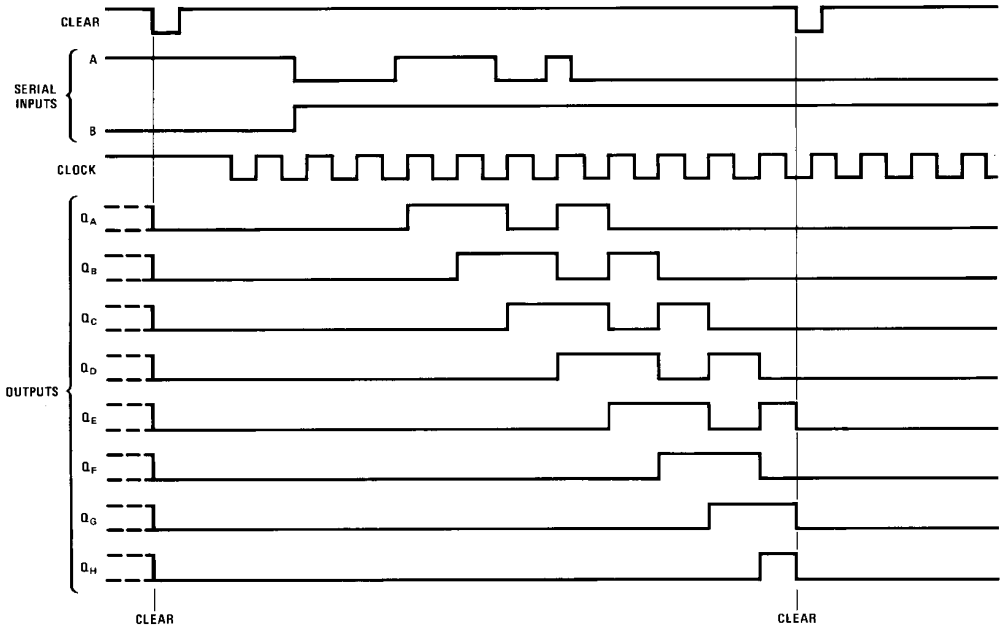
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay Time to a Logical "0" or a Logical "1" from Clock to Q	$V_{CC} = 5V$ $V_{CC} = 10V$		230 90	310 120	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0" from Clear to Q	$V_{CC} = 5V$ $V_{CC} = 10V$		280 110	380 150	ns ns
t_S	Time Prior to Clock Pulse that Data Must be Present	$V_{CC} = 5V$ $V_{CC} = 10V$	200 80	110 30		ns ns
t_H	Time After Clock Pulse that Data Must be Held	$V_{CC} = 5V$ $V_{CC} = 10V$	0 0	0 0		ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5V$ $V_{CC} = 10V$	2.0 5.5	3 8		MHz MHz
t_W	Minimum Clear Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		150 55	250 90	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$ $V_{CC} = 10V$	15 5			μs μs
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		140		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

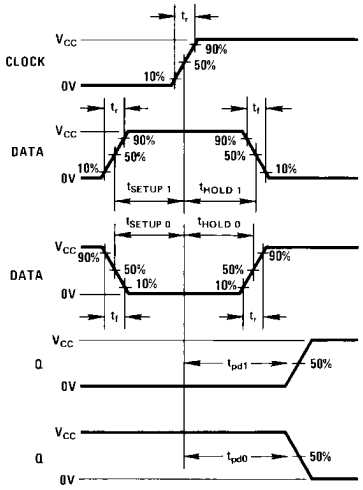
Logic Waveforms



TL/F/5896–3

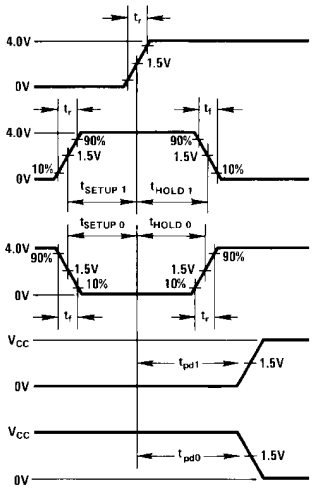
Switching Time Waveforms

CMOS to CMOS



TL/F/5896–4

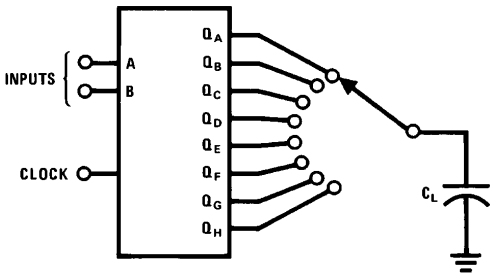
TTL to CMOS



TL/F/5896–5

$t_r = t_f = 20$ ns

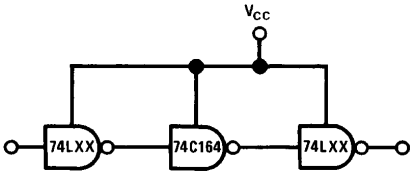
AC Test Circuit



TL/F/5896–6

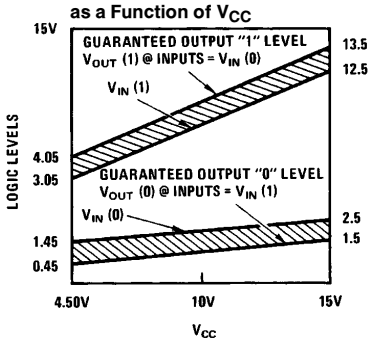
Typical Applications

74C Compatibility



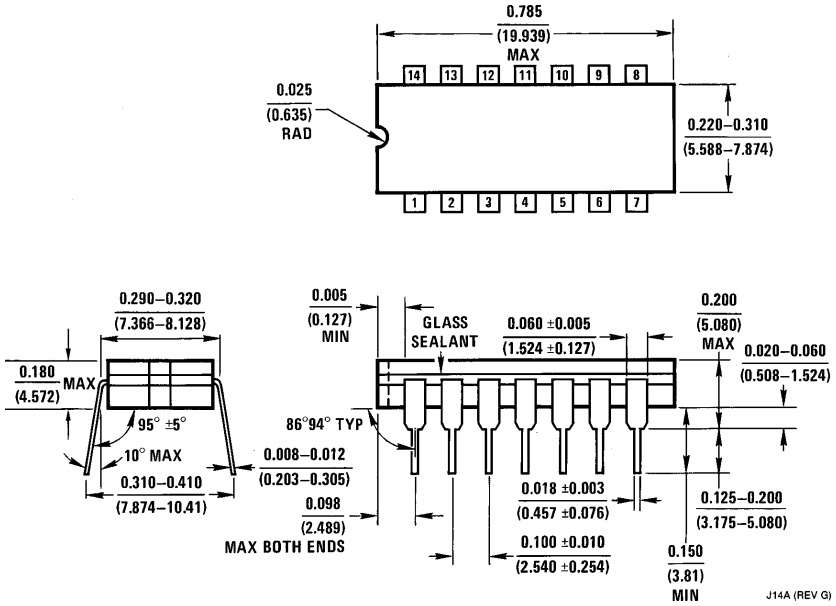
TL/F/5896–7

Guaranteed Noise Margin as a Function of V_{CC}



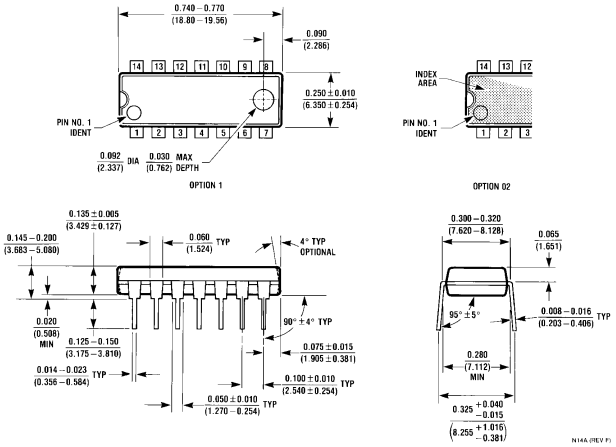
TL/F/5896–8

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C164J or MM74C164J
NS Package Number J14A

Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number MM54C164N or MM74C164N
NS Package Number N14A

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