National Semiconductor

ADVANCE INFORMATION
November 1996

LMX9301
Frequency Synthesizer Module

General Description

The Frequency Synthesizer Module is a Low Temperature Co-fired Ceramic (LTCC) RF module consisting of a high performance frequency synthesizer, loop filter, and voltage controlled oscillator (VCO). The frequency synthesizer is fabricated using National's ABiC IV BiCMOS process (f_T = 14 GHz). The loop filter and VCO are fabricated with National's Low Temperature Co-fired Ceramics.

The Frequency Synthesizer Module can be used for local oscillator applications. Using a digital phase locked loop technique, the on board frequency synthesizer can generate a very stable, low noise local oscillator. Serial data is transferred into the module using a three wire interface. The loop filter is designed for fast lock times and maximum attenuation of reference spurs.

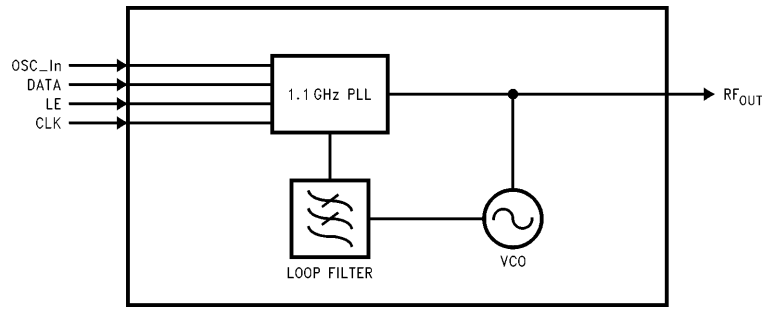
The module is available in an 18-pin 500 mil × 500 mil × 125 mil (refer to dwg) package.

Features

- Low current consumption
- Low phase noise tunable local oscillator
- 1.1 GHz PLLatinum™ PLL in module

Applications

- AMPS wireless cellular systems
- Portable wireless communications (PCS/PCN, cordless)



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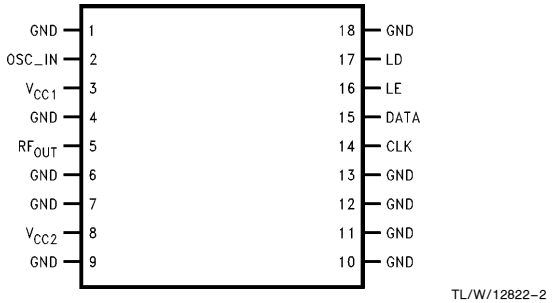
Pin Diagram



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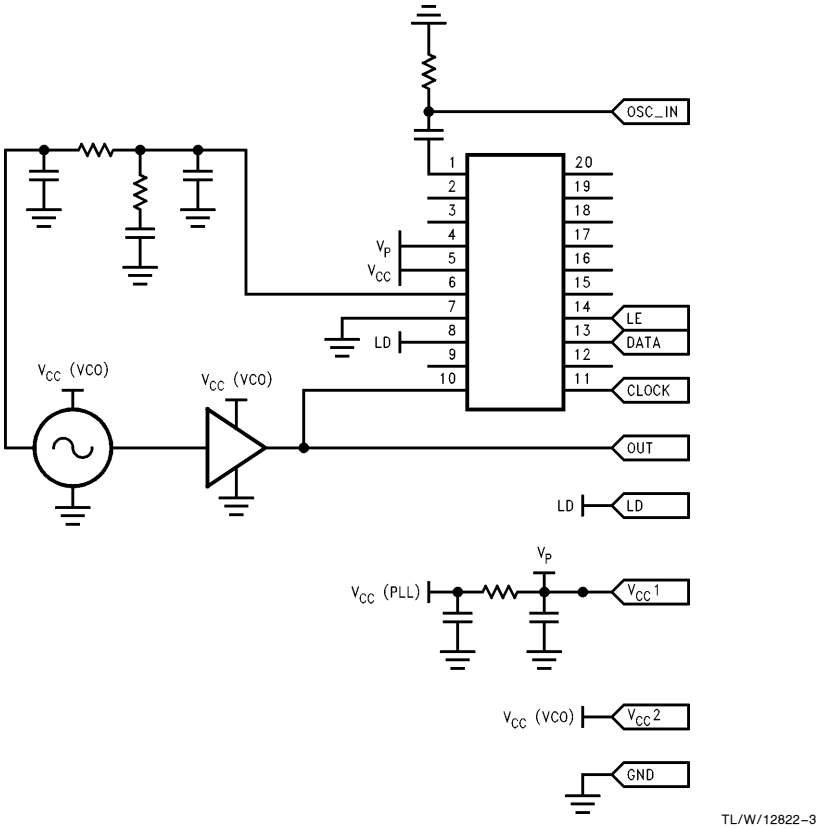
Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	GND		Ground.
2	OSC__IN	I	Reference Oscillator input. A CMOS inverting gate input intended for connection to a crystal resonator for operation as an oscillator. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate. May also be used as a buffer for an externally provided reference oscillator.
3	$V_{CC}1$		Power supply voltage input to PLL.
4	GND		Ground.
5	RF_{OUT}	O	VCO frequency output.
6	GND		Ground.
7	GND		Ground.
8	$V_{CC}2$		Power supply voltage input to VCO.
9	GND		Ground.
10	GND		Ground.
11	GND		Ground.
12	GND		Ground.
13	GND		Ground.
14	CLK	I	High impedance CMOS Clock input. Data is clocked in on the rising edge, into the various counters and registers.
15	DATA	I	Binary serial data input. Data entered MSB first. LSB is control bit. High impedance CMOS input.
16	LE	I	Load enable input (with internal pull-up resistor). When LE transitions HIGH, data stored in the shift registers is loaded into the appropriate latch (control bit dependent). Clock must be low when LE toggles high or low. See serial diagram.
17	LD	O	Lock detect. Output provided to indicate when the VCO frequency is in ''lock''. When the loop is locked, the pin's output is HIGH with narrow pulses.
18	GND		Ground.

Functional Diagram



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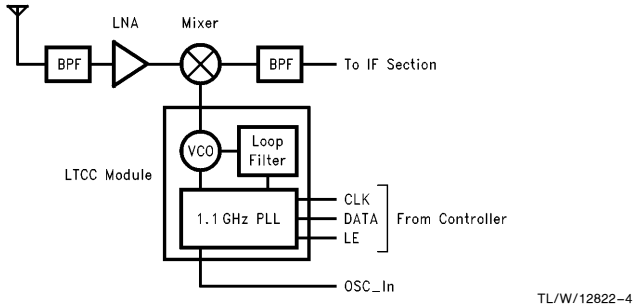
Typical Application Example



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	−0.3V to +6.5V
V_P	−0.3V to +6.5V
Voltage on Any Pin with GND = 0V (V_I)	−0.3V to +6.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temperature (T_L) (solder, 4 sec.)	+260°C

Recommended Operating Conditions

Power Supply Voltage (V_{CC})	4.75V to 5.5V
Operating Temperature (T_A)	−10°C to +70°C

Note 1: Absolute Maximum Rating indicate limits beyond which daage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Electrical Characteristics

The following specifications are guaranteed over the recommended operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
I_{CC}	Power Supply Current			35	45	mA
f_{OSC}	Reference Oscillator Frequency			15		MHz
f_{VCO}	Frequency		738		766	MHz
P_{OUT}	Output Level		−3	0	+3	dBm
ℓ (f_m)	Single Side Band Phase Noise	f_m = 1000 Hz	80			dBc/Hz
		f_m = 30000 Hz	110			dBc/Hz
	Spurious Reference Sidebands	30 kHz Offset		−80	−70	dBc
		60 kHz Offset		−90		dBc
	Nth Spurious Harmonic	2nd harmonic		−38	−10	dBc
	Spurious Non Harmonic				−70	dBc
T_{LOCK}	Frequency Lock Time (MAX)	±1 kHz from carrier, 25 MHz jump		25	40	ms
T_{LOCK}	Frequency Lock Time (Adjacent Channels)	±1 kHz from carrier, 30 kHz jump		8	20	ms

DC Electrical Characteristics

The following specifications are guaranteed over the recommended operating conditions.

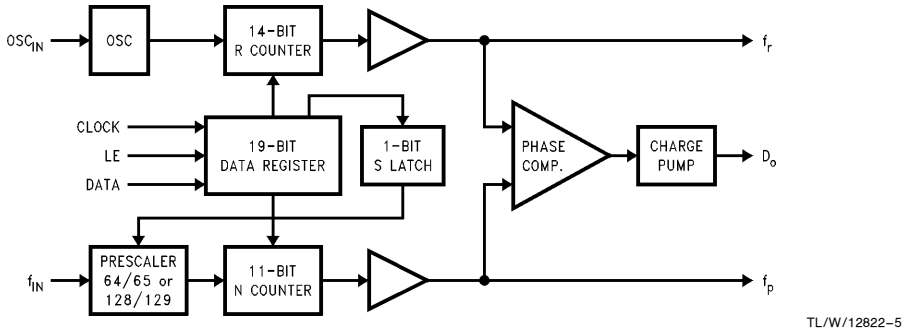
DIGITAL INTERFACE SECTION

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
V_{IH}	High Level Input Voltage		V_{CC} − 0.8			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IN}	Input Current	GND < V_{IN} < V_{CC}	−1.0		1.0	μA
t_{CS}	Data to Clock Set Up Time		50			ns
t_{CH}	Data to Clock Hold Time		10			ns
t_{CWH}	Clock Pulse Width High		50			ns
t_{CWL}	Clock Pulse Width Low		50			ns
t_{ES}	Clock to Load Enable Set Up Time		50			ns
t_{EW}	Load Enable Pulse Width		50			ns

Note 1: DC Electrical Characteristics for the digital section apply to the power down pin and the MICROWIRE™ interface.

PLL Functional Description

The simplified block diagram below shows the 19-bit data register, the 14-bit R Counter and the S Latch, and the 18-bit N Counter (intermediate latches are not shown). The data stream is clocked (on the rising edge of clock) into the DATA input, MSB first. If the Control Bit (last bit input) is HIGH, the DATA is transferred into the R Counter (programmable reference divider) and the S Latch (prescaler select: 64/65 and 128/129). If the Control Bit (LSB) is LOW, the DATA is transferred into the N Counter (programmable divider).



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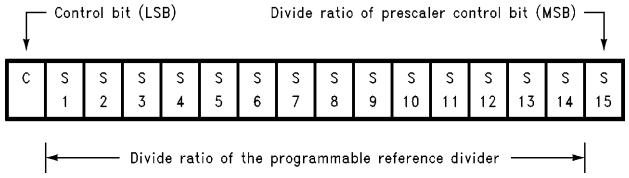
PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) AND PRESCALER SELECT (S LATCH)

If the Control Bit (last bit shifted into the Data Register) is HIGH, data is transferred from the 19-bit shift register into a 14-bit latch (which sets the 14-bit R Counter) and the 1-bit S Latch (S15, which sets the prescaler 64/65 and 128/129). Serial data format is shown below.



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14-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

The R divide ratio must be set to maintain a 30 kHz phase comparator frequency. The divide ratio is chosen by dividing the selected reference oscillator frequency by 30 kHz. For example, a 15 MHz reference oscillator frequency gives:

$$R = \frac{OSC\_IN}{30\ kHz} = \frac{15\ MHz}{30\ kHz} = 500$$

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
1333	0	0	0	1	0	1	0	0	1	1	0	1	0	1

Notes: Divide ratios less than 3 or greater than 1333 are prohibited.

S1 to S14: These bits select the divide ratio of the programmable reference divider.

C: Control bit (set to HIGH level to load R counter and S Latch)

Data is shifted in MSB first.

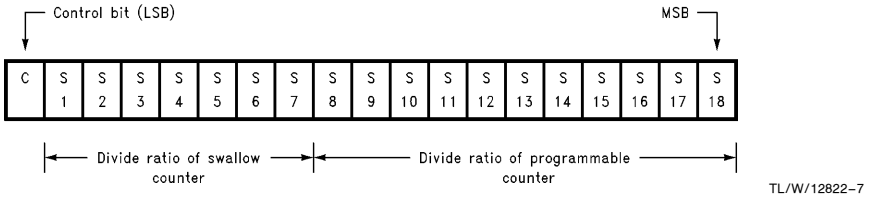
1-BIT PRESCALER SELECT (S LATCH)

Prescaler Select P	S 15
128/129	0
64/65	1

PLL Functional Description (Continued)

PROGRAMMABLE DIVIDER (N COUNTER)

The N counter consists of the 7-bit swallow counter (A counter) and the 11-bit programmable counter (B counter). If the Control Bit (last bit shifted into the Data Register) is LOW, data is transferred from the 19-bit shift register into a 7-bit latch (which sets the 7-bit Swallow (A) Counter) and an 11-bit latch (which sets the 11-bit programmable (B) Counter). Serial data format is shown below.



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Note: S8 to S18: Programmable counter divide ratio control bits (3 to 2047)

7-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)

The A COUNTER divide ratio is dependent on the PRESCALER select.

PRESCALER = 64/65

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
64	0	1	1	1	1	1	1

Notes: Divide ratio: 0 to 63
B ≥ A

PRESCALER = 128/129

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Notes: Divide ratio: 0 to 127
B ≥ A

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER)

The B COUNTER divide ratio is dependent on the PRESCALER select.

PRESCALER = 64/65

Divide Ratio R	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
384	0	0	1	1	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•	•
399	0	0	1	1	0	0	0	1	1	1	1

Note: Divide ratio: 384 to 399 (Other divide ratios are prohibited)

PRESCALER = 128/129

Divide Ratio R	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
192	0	0	0	1	1	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•	•
199	0	0	0	1	1	0	0	0	1	1	1

Note: Divide ratio: 192 to 199 (Other divide ratios are prohibited)

Functional Description (Continued)

PULSE SWALLOW FUNCTION

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$, where $f_{OSC} = 30$ kHz.

f_{VCO} Output frequency of voltage controlled oscillator (VCO), 738 MHz to 766 MHz

B: Preset divide ratio of binary 11-bit programmable counter,
If $P = 128$, then $192 \leq B \leq 199$
If $P = 64$, then $384 \leq B \leq 399$

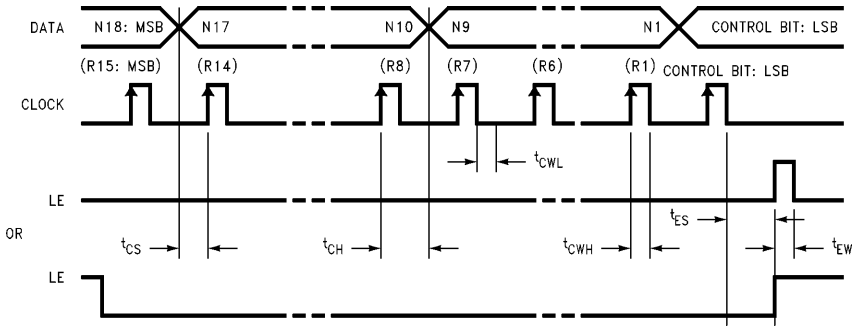
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A \leq B$)
If $P = 128$, then $0 \leq A \leq 127$
If $P = 64$, then $0 \leq A \leq 64$

f_{OSC}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 1333)

P: Preset modulus of dual modulus prescaler

SERIAL DATA INPUT TIMING



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Notes: Parenthesis data indicates programmable reference divider data.

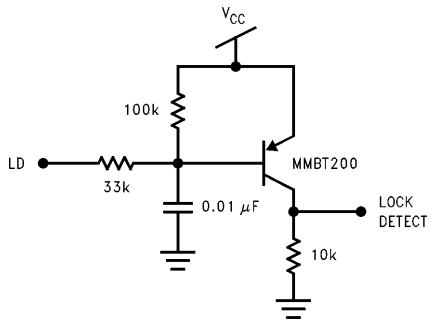
Data shifted into register on clock rising edge.

Data is shifted in MSB first.

Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6 V/ns with amplitudes of 2.2V @ $V_{CC} = 2.7$V and 2.6V @ $V_{CC} = 5.5$V.

Typical Lock Detect Circuit

A lock detect circuit is needed in order to provide a steady LOW signal when the PLL is in the locked state. A typical circuit is shown below.



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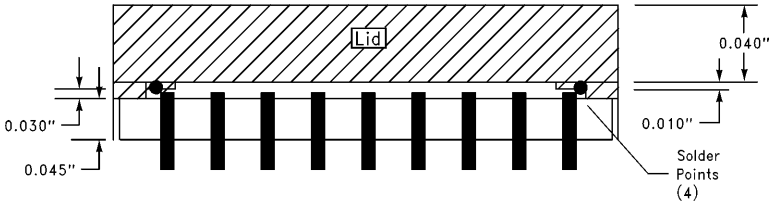
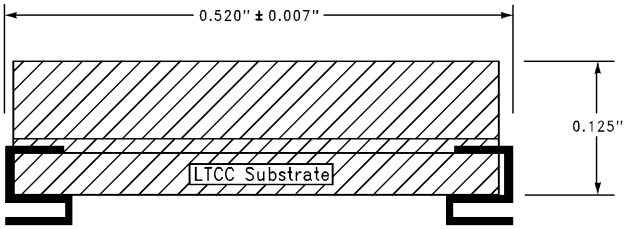
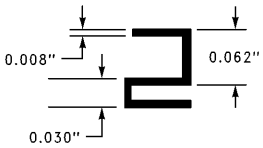


Side View with Lid Cutout Over Leads



Edge View with Lid Extended to Substrate Base



Clip Lead

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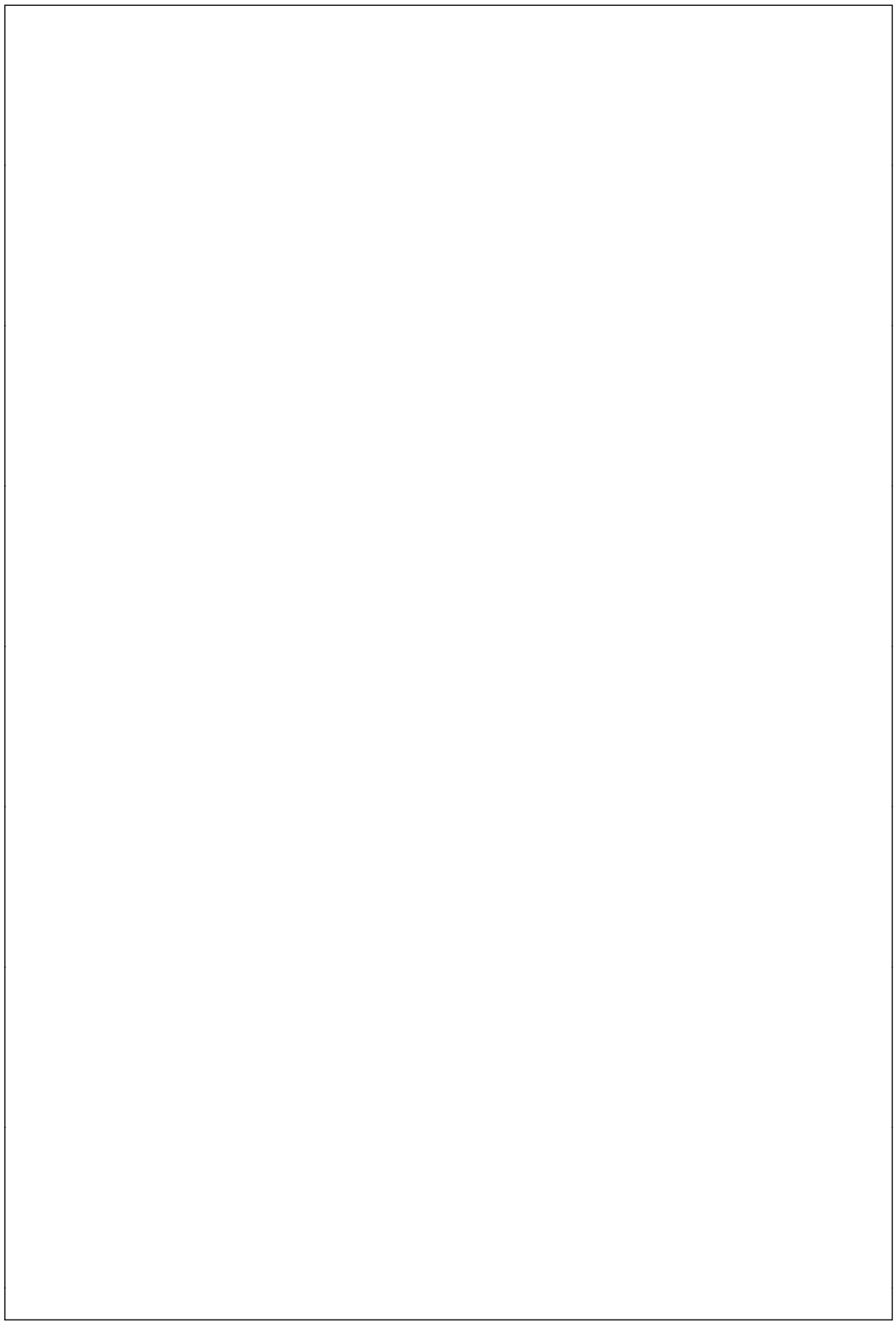

Physical Dimensions inches (millimeters) unless otherwise noted

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