National Semiconductor

April 1995

LM12L454/LM12L458 12-Bit + Sign Data Acquisition System with Self-Calibration

General Description

The LM12L454 and LM12L458 are highly integrated 3.3V Data Acquisition Systems. They combine a fully-differential self-calibrating (correcting linearity and zero errors) 13-bit (12-bit + sign) analog-to-digital converter (ADC) and sample-and-hold (S/H) with extensive analog functions and digital functionality. Up to 32 consecutive conversions, using two's complement format, can be stored in an internal 32-word (16-bit wide) FIFO data buffer. An internal 8-word RAM can store the conversion sequence for up to eight acquisitions through the LM12L458's eight-input multiplexer. The LM12L454 has a four-channel multiplexer, a differential multiplexer output, and a differential S/H input. The LM12L454 and LM12L458 can also operate with 8-bit + sign resolution and in a supervisory "watchdog" mode that compares an input signal against two programmable limits. Programmable acquisition times and conversion rates are possible through the use of internal clock-driven timers.

All registers, RAM, and FIFO are directly addressable through the high speed microprocessor interface to either an 8-bit or 16-bit databus. The LM12L454 and LM12L458 include a direct memory access (DMA) interface for high-speed conversion data transfer.

Key Specifications (f_{CLK} = 6 MHz)

- Resolution — 12-bit + sign or 8-bit + sign
- 13-bit conversion time — 7.3 μs
- 9-bit conversion time — 3.5 μs
- 13-bit Through-put rate — 106k samples/s (min)
- Comparison time ("watchdog" mode) — 1.8 μs (max)
- ILE — ±1 LSB (max)
- V_{IN} range — GND to V_A+
- Power dissipation — 15 mW (max)
- Stand-by mode — 5 μW (typ)
- Single supply — 3V to 5.5V

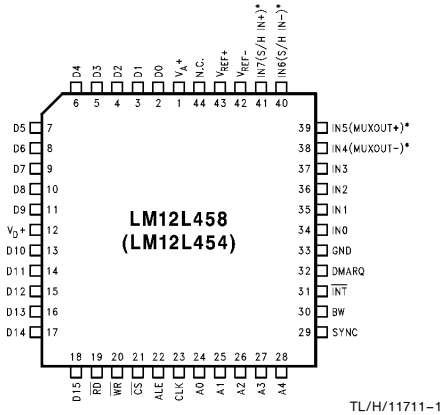
Features

- Three operating modes: 12-bit + sign, 8-bit + sign, and "watchdog"
- Single-ended or differential inputs
- Built-in Sample-and-Hold
- Instruction RAM and event sequencer
- 8-channel (LM12L458), 4-channel (LM12L454) multiplexer
- 32-word conversion FIFO
- Programmable acquisition times and conversion rates
- Self-calibration and diagnostic mode
- 8- or 16-bit wide databus microprocessor or DSP interface
- CMOS compatible I/O

Applications

- Data Logging
- Process Control
- Energy Management
- Medical Instrumentation

Connection Diagram



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*Pin names in ( ) apply to the LM12L454.

Order Number LM12L454CIV or LM12L458CIV
See NS Package Number V44A

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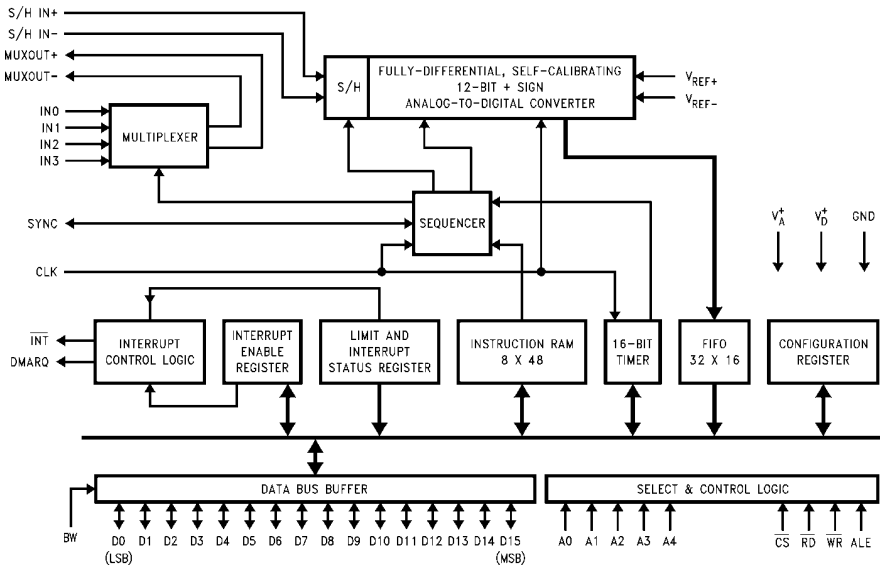
Functional Diagrams

LM12L454



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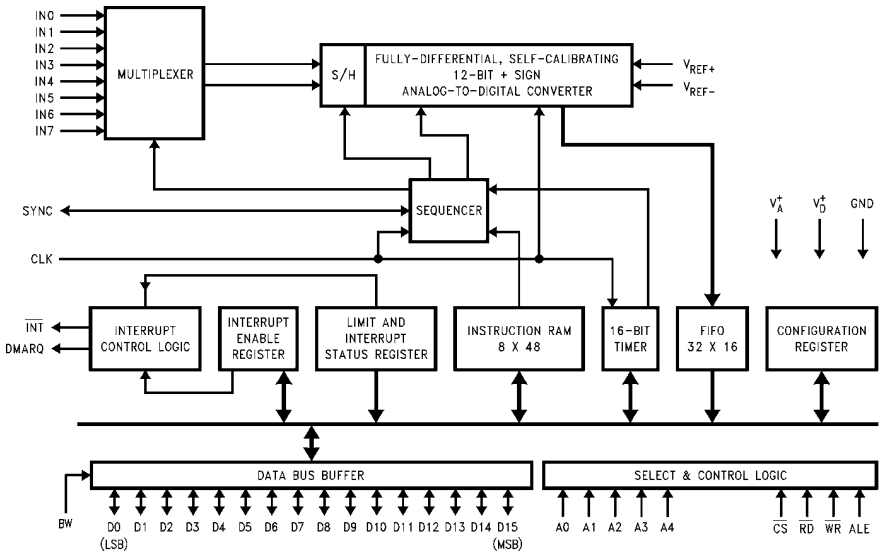
LM12L458



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Ordering Information

Guaranteed Clock Freq (min)	Guaranteed Linearity Error (max)	Order Part Number	See NS Package Number
6 MHz	±1.0 LSB	LM12L454CIV LM12L458CIV	V44A V44A

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_A^+ and V_D^+)	6.0V
Voltage at Input and Output Pins except IN0−IN3 (LM12L454) and IN0−IN7 (LM12L458)	−0.3V to V^+ + 0.3V
Voltage at Analog Inputs IN0−IN3 (LM12L454) and IN0−IN7 (LM12L458)	GND − 5V to V^+ + 5V
$\lvert V_A^+ - V_D^+ \rvert$	300 mV
Input Current at Any Pin (Note 3)	±5 mA
Package Input Current (Note 3)	±20 mA
Power Dissipation (T_A = 25°C) V Package (Note 4)	875 mW
Storage Temperature	−65°C to +150°C
Lead Temperature V Package, Infrared, 15 sec.	+300°C
ESD Susceptibility (Note 5)	1.5 kV

See AN-450 ''Surface Mounting Methods and Their Effect on Product Reliability'' for other methods of soldering surface mount devices.

Operating Ratings (Notes 1, 2)

Temperature Range ($T_{min} \le T_A \le T_{max}$) LM12L454CIV/LM12L458CIV	$-40°C \le T_A \le 85°C$
Supply Voltage	
V_A^+, V_D^+	3.0V to 5.5V
$\lvert V_A^+ - V_D^+ \rvert$	≤100 mV
V_{IN+} Input Range	$GND \le V_{IN+} \le V_A^+$
V_{IN-} Input Range	$GND \le V_{IN-} \le V_A^+$
V_{REF+} Input Voltage	$1V \le V_{REF+} \le V_A^+$
V_{REF-} Input Voltage	$0V \le V_{REF-} \le V_{REF+} - 1V$
$V_{REF+} - V_{REF-}$	$1V \le V_{REF} \le V_A^+$
V_{REF} Common Mode Range (Note 16)	$0.1\ V_A^+ \le V_{REFCM} \le 0.6\ V_A^+$

Converter Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, $V_{REF+} = 2.5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 6.0$ MHz, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \le 25\Omega$, fully-differential input with fixed 1.25V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8, and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
ILE	Positive and Negative Integral Linearity Error	After Auto-Cal (Notes 12, 17)	±1/2	**±1**	LSB (max)
TUE	Total Unadjusted Error	After Auto-Cal (Note 12)	±1		LSB
	Resolution with No Missing Codes	After Auto-Cal (Note 12)		**13**	Bits (max)
DNL	Differential Non-Linearity	After Auto-Cal		**±1**	LSB (max)
	Zero Error	After Auto-Cal (Notes 13, 17)	±1/4	**±1**	LSB (max)
	Positive Full-Scale Error	After Auto-Cal (Notes 12, 17)	±1/2	**±3**	LSB (max)
	Negative Full-Scale Error	After Auto-Cal (Notes 12, 17)	±1/2	**±3**	LSB (max)
	DC Common Mode Error	(Note 14)	±2	**±4**	LSB (max)
ILE	8-Bit + Sign and ''Watchdog'' Mode Positive and Negative Integral Linearity Error	(Note 12)		**±1/2**	LSB (max)
TUE	8-Bit + Sign and ''Watchdog'' Mode Total Unadjusted Error	After Auto-Zero	±1/2	**±3/4**	LSB (max)
	8-Bit + Sign and ''Watchdog'' Mode Resolution with No Missing Codes			**9**	Bits (max)
DNL	8-Bit + Sign and ''Watchdog'' Mode Differential Non-Linearity			**±1**	LSB (max)
	8-Bit + Sign and ''Watchdog'' Mode Zero Error	After Auto-Zero		**±1/2**	LSB (max)
	8-Bit + Sign and ''Watchdog'' Positive and Negative Full-Scale Error			**±1/2**	LSB (max)

Converter Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, $V_{REF+} = 2.5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 6.0$ MHz, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 1.25V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8, and 9) (Continued)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
	8-Bit + Sign and "Watchdog" Mode DC Common Mode Error		±1/8		LSB
	Multiplexer Channel-to-Channel Matching		±0.05		LSB
V_{IN+}	Non-Inverting Input Range			**GND** **V_A^+**	V (min) V (max)
V_{IN-}	Inverting Input Range			**GND** **V_A^+**	V (min) V (max)
$V_{IN+} - V_{IN-}$	Differential Input Voltage Range			**$-V_A^+$** **V_A^+**	V (min) V (max)
$\frac{V_{IN+} - V_{IN-}}{2}$	Common Mode Input Voltage Range			**GND** **V_A^+**	V (min) V (max)
PSS	Power Supply Zero Error Sensitivity Full-Scale Error (Note 15) Linearity Error	$V_A^+ = V_D^+ = 3.3V$ ±10% $V_{REF+} = 2.5V$, $V_{REF-} = GND$	±0.2 ±0.4 ±0.2	**±1.75** **±2**	LSB (max) LSB (max) LSB
C_{REF}	V_{REF+}/V_{REF-} Input Capacitance		85		pF
C_{IN}	Selected Multiplexer Channel Input Capacitance		75		pF

Converter AC Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, $V_{REF+} = 2.5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 6.0$ MHz, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 1.25V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8, and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
	Clock Duty Cycle		50	 **40** **60**	% % (min) % (max)
t_C	Conversion Time	13-Bit Resolution, Sequencer State S5 *(Figure 11)*	44 (t_{CLK})	**44 (t_{CLK}) + 50 ns**	(max)
		9-Bit Resolution, Sequencer State S5 *(Figure 11)*	21 (t_{CLK})	**21 (t_{CLK}) + 50 ns**	(max)
t_A	Acquisition Time	Sequencer State S7 *(Figure 11)* Built-in minimum for 13-Bits	9 (t_{CLK})	**9 (t_{CLK}) + 50 ns**	(max)
		Built-in minimum for 9-Bits and "Watchdog" mode	2 (t_{CLK})	**2 (t_{CLK}) + 50 ns**	(max)
t_Z	Auto-Zero Time	Sequencer State S2 *(Figure 11)*	76 (t_{CLK})	**76 (t_{CLK}) + 50 ns**	(max)
t_{CAL}	Full Calibration Time	Sequencer State S2 *(Figure 11)*	4944 (t_{CLK})	**4944 (t_{CLK}) + 50 ns**	(max)
	Throughput Rate (Note 18)		107	**106**	kHz (min)
t_{WD}	"Watchdog" Mode Comparison Time	Sequencer States S6, S4, and S5 *(Figure 11)*	11 (t_{CLK})	**11 (t_{CLK}) + 50 ns**	(max)
t_{PU}	Power-Up Time		10		ms
t_{WU}	Wake-Up Time		10		ms

DC Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, $V_{REF+} = 2.5V$, $V_{REF-} = 0V$, $f_{CLK} = 6.0$ MHz and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, and 8)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
I_D^+	V_D^+ Supply Current	$\overline{CS}$ = "1" LM12L454/8	0.4	**1.0**	mA (max)
I_A^+	V_A^+ Supply Current	$\overline{CS}$ = "1" LM12L454/8	2.25	**3.5**	mA (max)
I_{ST}	Stand-By Supply Current ($I_D^+ + I_A^+$)	Power-Down Mode Selected Clock Stopped 6 MHz Clock	 1.5 30	 4.5	 μA (max) μA (max)
	Multiplexer ON-Channel Leakage Current	$V_A^+ = 3.6V$ ON-Channel = 3.6V, OFF-Channel = 0V ON-Channel = 0V, OFF-Channel = 3.6V	 0.1 0.1	 **0.3** **0.3**	 μA (max) μA (max)
	Multiplexer OFF-Channel Leakage Current	$V_A^+ = 3.6V$ ON-Channel = 3.6V, OFF-Channel = 0V ON-Channel = 0V, OFF-Channel = 3.6V	 0.1 0.1	 **0.3** **0.3**	 μA (max) μA (max)
R_{ON}	Multiplexer ON-Resistance	LM12L454 $V_{IN} = 3.3V$ $V_{IN} = 1.65V$ $V_{IN} = 0V$	 850 1300 830	 **1500** **2000** **1500**	 Ω(max) Ω(max) Ω(max)
	Multiplexer Channel-to-Channel R_{ON} matching	LM12L454 $V_{IN} = 3.3V$ $V_{IN} = 1.65V$ $V_{IN} = 0V$	 ±1.0% ±1.0% ±1.0%	 ±**3.0%** ±**3.0%** ±**3.0%**	 (max) (max) (max)

Digital Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, and 8)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
$V_{IN(1)}$	Logical "1" Input Voltage	$V_A^+ = V_D^+ = 3.6V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V_A^+ = V_D^+ = 3.0V$ ALE, Pin 22		**0.7** **0.6**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 3.3V$	0.005	**1.0** **2.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1.0** **−2.0**	μA (max)
C_{IN}	D0−D15 Input Capacitance		6		pF
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_A^+ = V_D^+ = 3.0V$ $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		**2.4** **2.85**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_A^+ = V_D^+ = 3.0V$ $I_{OUT} = 1.6$ mA $I_{OUT} = 10\ \mu A$		**0.4** **0.1**	V (max)
I_{OUT}	TRI-STATE® Output Leakage Current	$V_{OUT} = 0V$ $V_{OUT} = 3.3V$	−0.01 0.01	**−3.0** **3.0**	μA (max) μA (max)

Digital Timing Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, $t_r = t_f = 3$ ns, and $C_L = 100$ pF on data I/O, $\overline{INT}$ and DMARQ lines unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, and 8)

Symbol (See *Figures 8a, 8b,* and *8c*)	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
1, 3	$\overline{CS}$ or Address Valid to ALE Low Set-Up Time			**40**	ns (min)
2, 4	$\overline{CS}$ or Address Valid to ALE Low Hold Time			**20**	ns (min)
5	ALE Pulse Width			**45**	ns (min)
6	$\overline{RD}$ High to Next ALE High			**35**	ns (min)
7	ALE Low to $\overline{RD}$ Low			**20**	ns (min)
8	$\overline{RD}$ Pulse Width			**100**	ns (min)
9	$\overline{RD}$ High to Next $\overline{RD}$ or $\overline{WR}$ Low			**100**	ns (min)
10	ALE Low to $\overline{WR}$ Low			**20**	ns (min)
11	$\overline{WR}$ Pulse Width			**60**	ns (min)
12	$\overline{WR}$ High to Next ALE High			**75**	ns (min)
13	$\overline{WR}$ High to Next $\overline{RD}$ or $\overline{WR}$ Low			**140**	ns (min)
14	Data Valid to $\overline{WR}$ High Set-Up Time			**40**	ns (min)
15	Data Valid to $\overline{WR}$ High Hold Time			**30**	ns (min)
16	$\overline{RD}$ Low to Data Bus Out of TRI-STATE		30	**10** **70**	ns (min) ns (max)
17	$\overline{RD}$ High to TRI-STATE	$R_L = 1\ k\Omega$	30	**10** **110**	ns (min) ns (max)
18	$\overline{RD}$ Low to Data Valid (Access Time)		30	**10** **95**	ns (min) ns (max)

Digital Timing Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, $t_r = t_f = 3$ ns, and $C_L = 100$ pF on data I/O, $\overline{INT}$ and DMARQ lines unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, and 8) (Continued)

Symbol (See *Figures 8a, 8b,* and *8c*)	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
20	Address Valid or $\overline{CS}$ Low to $\overline{RD}$ Low			**20**	ns (min)
21	Address Valid or $\overline{CS}$ Low to $\overline{WR}$ Low			**20**	ns (min)
19	Address Invalid from $\overline{RD}$ or $\overline{WR}$ High			**10**	ns (min)
22	$\overline{INT}$ High from $\overline{RD}$ Low		30	**10** **60**	ns (min) ns (max)
23	DMARQ Low from $\overline{RD}$ Low		30	**10** **60**	ns (min) ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

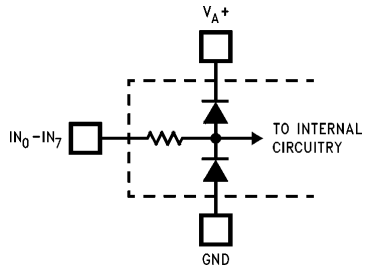
Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} <$ GND or $V_{IN} > (V_A^+$ or $V_D^+)$), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current of 5 mA, to simultaneously exceed the power supply voltages.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), Θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 150°C$, and the typical thermal resistance (Θ_{JA}) of the LM12L454 and LM12L458 in the V package, when board mounted, is 47°C/W.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Two on-chip diodes are tied to each analog input through a series resistor, as shown below. Input voltage magnitude up to 5V above V_A^+ or 5V below GND will not damage the LM12L454 or the LM12L458. However, errors in the A/D conversion can occur if these diodes are forward biased by more than 100 mV. As an example, if V_A^+ is 3.0 V_{DC}, full-scale input voltage must be $\leq$3.1 V_{DC} to ensure accurate conversions.



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Note 7: V_A^+ and V_D^+ must be connected together to the same power supply voltage and bypassed with separate capacitors at each V^+ pin to assure conversion/comparison accuracy.

Note 8: Accuracy is guaranteed when operating at $f_{CLK} = 6$ MHz.

Note 9: With the test condition for $V_{REF} = V_{REF+} - V_{REF-}$ given as +2.5V, the 12-bit LSB is 305 μV and the 8-bit/''Watchdog'' LSB is 4.88 mV.

Note 10: Typicals are at $T_A = 25°C$ and represent most likely parametric norm.

Note 11: Limits are guaranteed to National's AOQL (Average Output Quality Level).

Note 12: Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative integral linearity error the straight line passes through negative full-scale and zero. (See *Figures 5b* and *5c*).

Note 13: Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the worst-case value of the code transitions between −1 to 0 and 0 to +1 (see *Figure 6*).

Note 14: The DC common-mode error is measured with both inputs shorted together and driven from 0V to 2.5V. The measured value is referred to the resulting output value when the inputs are driven with a 1.25V signal.

Note 15: Power Supply Sensitivity is measured after Auto-Zero and/or Auto-Calibration cycle has been completed with V_A^+ and V_D^+ at the specified extremes.

Note 16: V_{REFCM} (Reference Voltage Common Mode Range) is defined as $(V_{REF+} + V_{REF-})/2$.

Note 17: The LM12L454/8's self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of ±0.10 LSB.

Note 18: The Throughput Rate is for a single instruction repeated continuously. Sequencer states 0 (1 clock cycle), 1 (1 clock cycle), 7 (9 clock cycles) and 5 (44 clock cycles) are used (see *Figure 11*). One additional clock cycle is used to read the conversion result stored in the FIFO, for a total of 56 clock cycles per conversion. The Throughput Rate is f_{CLK} (MHz)/N, where N is the number of clock cycles/conversion.

Electrical Characteristics

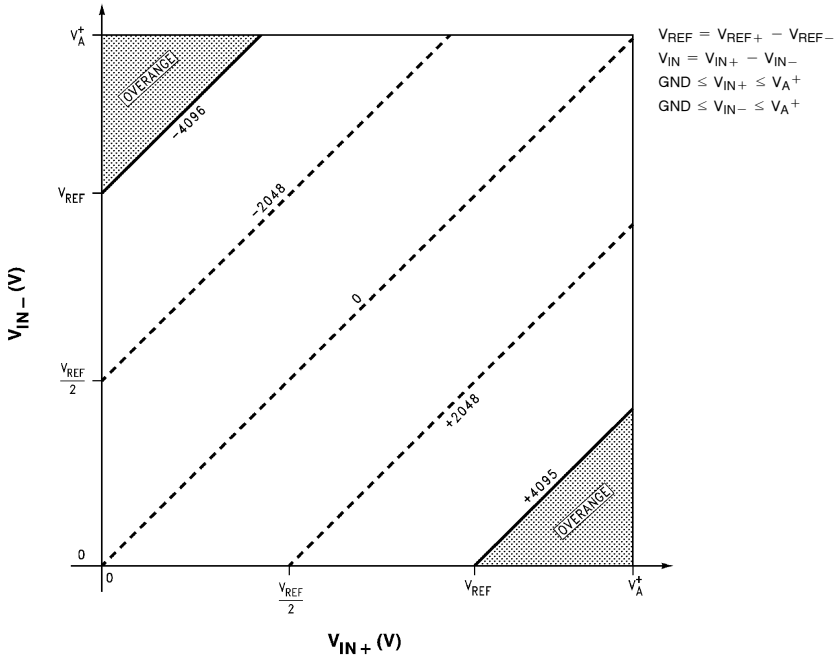

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FIGURE 1. The General Case of Output Digital Code vs the Operating Input Voltage Range

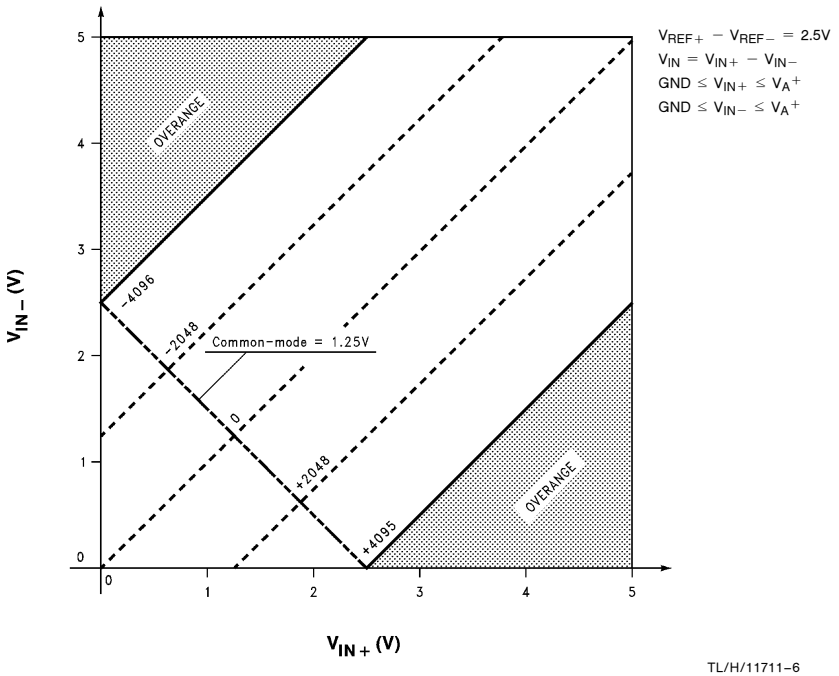

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FIGURE 2. Specific Case of Output Digital Code vs the Operating Input Voltage Range for $V_{REF} = 2.5V$

Electrical Characteristics (Continued)

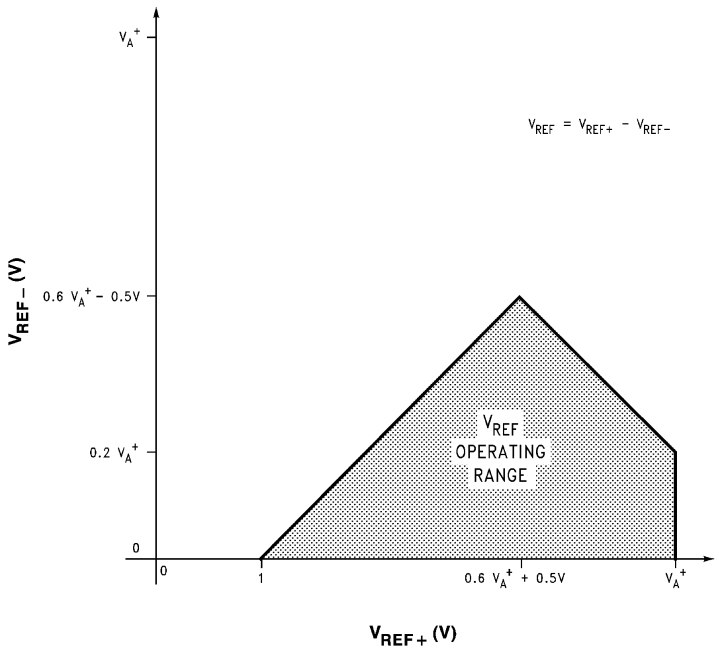

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FIGURE 3. The General Case of the V_{REF} Operating Range

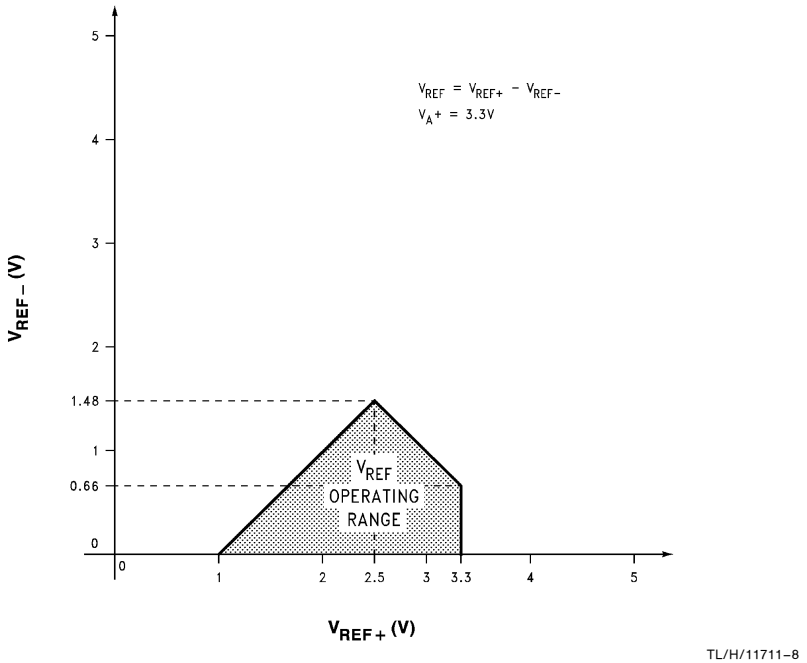

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FIGURE 4. The Specific Case of the V_{REF} Operating Range for $V_A^+ = 3.3V$

Electrical Characteristics (Continued)

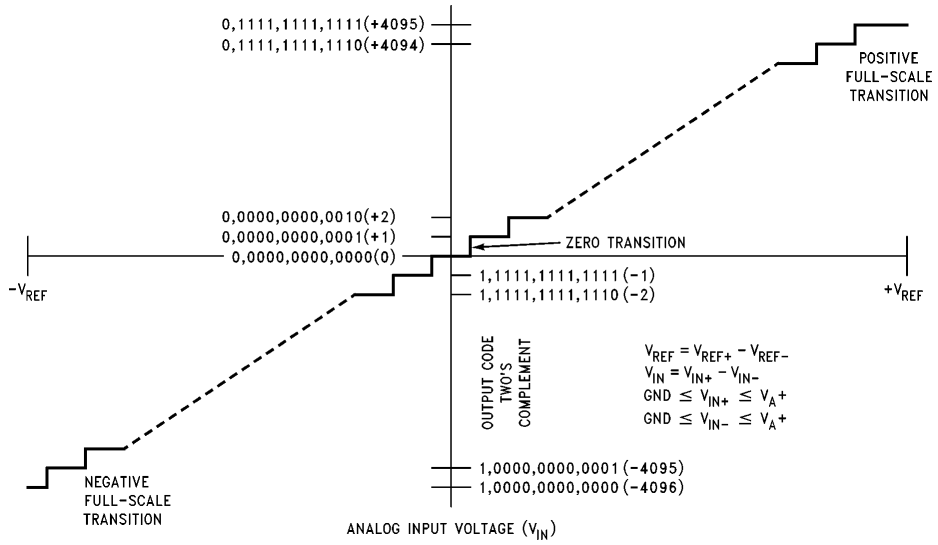

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FIGURE 5a. Transfer Characteristic

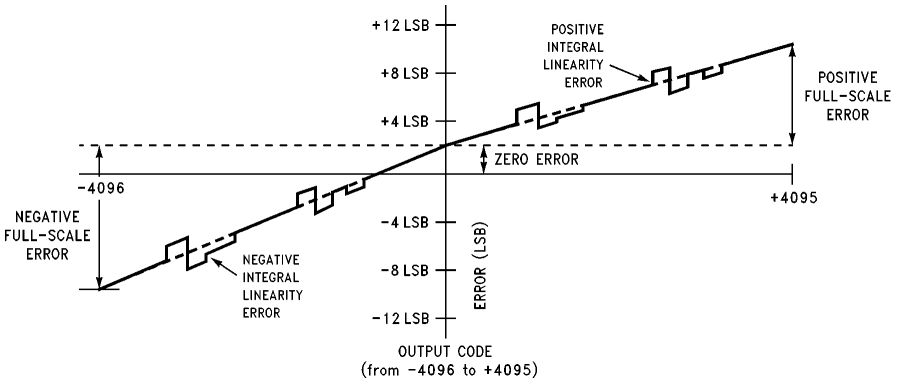

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FIGURE 5b. Simplified Error Curve vs Output Code without Auto-Calibration or Auto-Zero Cycles

Electrical Characteristics (Continued)

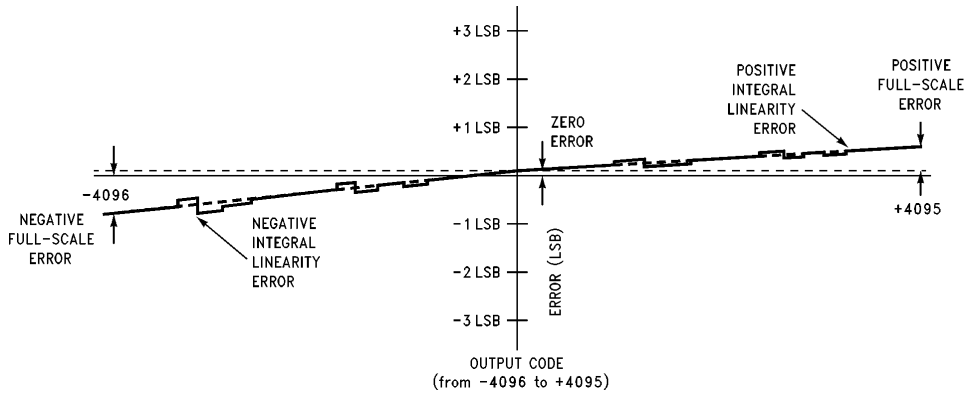

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FIGURE 5c. Simplified Error Curve vs Output Code after Auto-Calibration Cycle

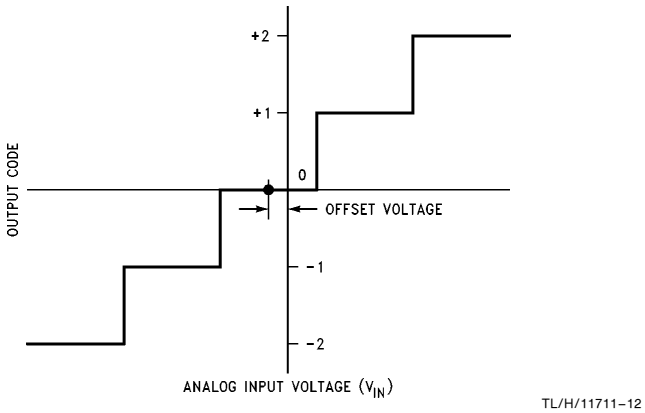

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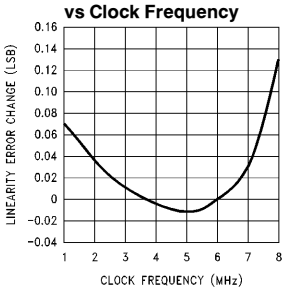
FIGURE 6. Offset or Zero Error Voltage

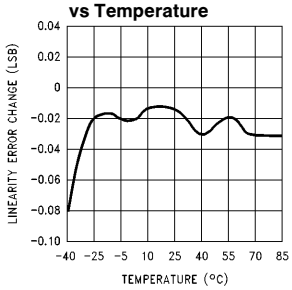
Typical Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration with $V_A^+ = V_D^+ = 3.3V$, $V_{REF+} = 2.5V$, $V_{REF-} = 0V$, $T_A = 25°C$, and $f_{CLK} = 6$ MHz unless otherwise specified. The performance for 8-bit + sign and "watchdog" modes is equal to or better than shown. (Note 9)

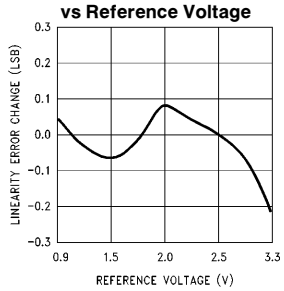
Linearity Error Change vs Clock Frequency



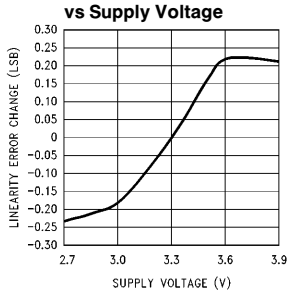
Linearity Error Change vs Temperature



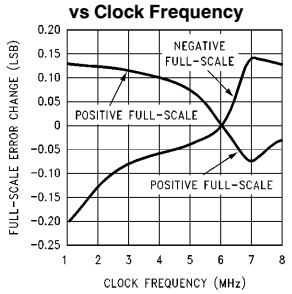
Linearity Error Change vs Reference Voltage



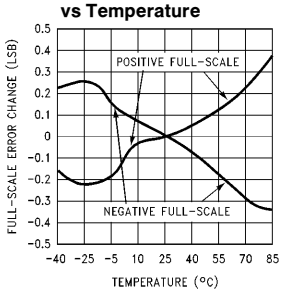
Linearity Error Change vs Supply Voltage



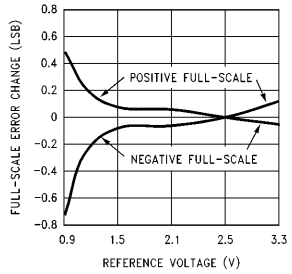
Full-Scale Error Change vs Clock Frequency



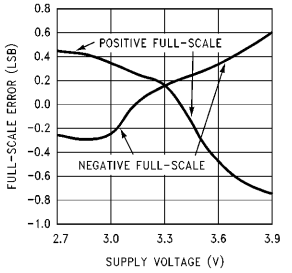
Full-Scale Error Change vs Temperature



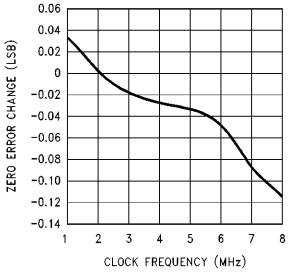
Full-Scale Error Change vs Reference Voltage



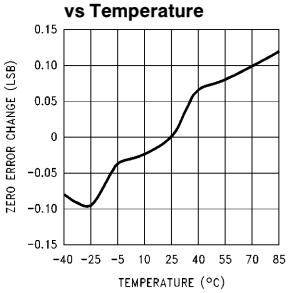
Full-Scale Error vs Supply Voltage



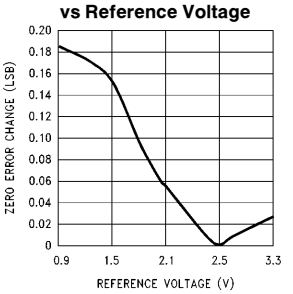
Zero Error Change vs Clock Frequency



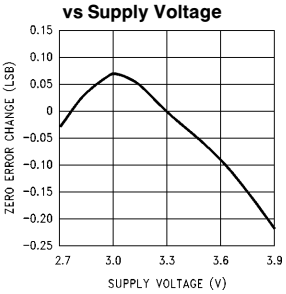
Zero Error Change vs Temperature



Zero Error Change vs Reference Voltage



Zero Error Change vs Supply Voltage



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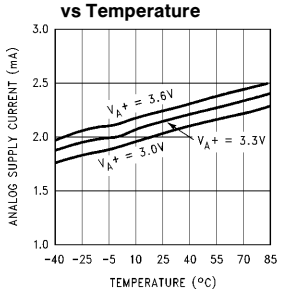
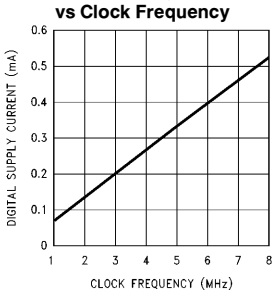
Typical Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign and ''watchdog'' modes is equal to or better than shown. (Note 9) (Continued)

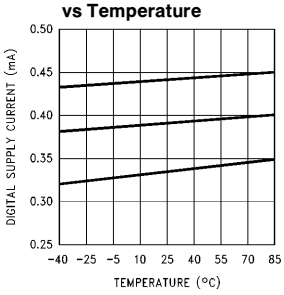
Analog Supply Current vs Temperature



Digital Supply Current vs Clock Frequency



Digital Supply Current vs Temperature



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Test Circuits and Waveforms

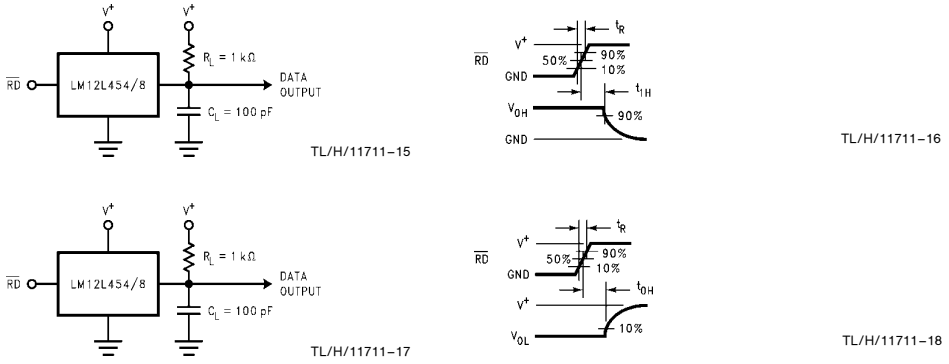

FIGURE 7. TRI-STATE Test Circuits and Waveforms

Timing Diagrams

$V_A^+ = V_D^+ = +3.3V$, $t_R = t_F = 3$ ns, $C_L = 100$ pF for the $\overline{INT}$, DMARQ, D0–D15 outputs.

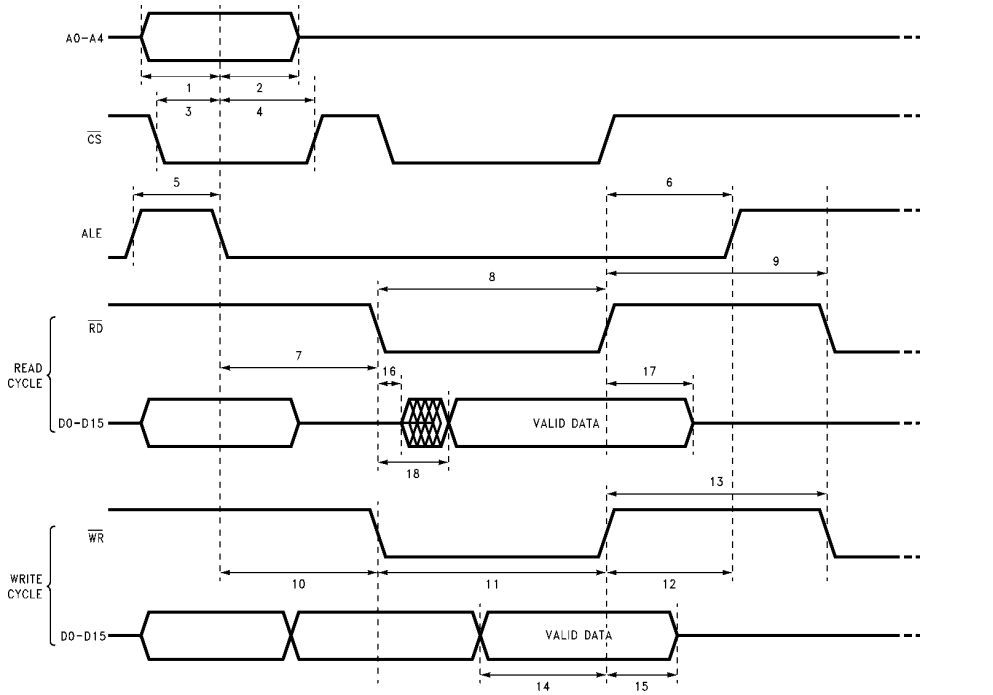

FIGURE 8a. Multiplexed Data Bus

1, 3: $\overline{CS}$ or Address valid to ALE low set-up time.
2, 4: $\overline{CS}$ or Address valid to ALE low hold time.
5: ALE pulse width
6: $\overline{RD}$ high to next ALE high
7: ALE low to $\overline{RD}$ low
8: $\overline{RD}$ pulse width
9: $\overline{RD}$ high to next $\overline{RD}$ or $\overline{WR}$ low
10: ALE low to $\overline{WR}$ low
11: $\overline{WR}$ pulse width
12: $\overline{WR}$ high to next ALE high
13: $\overline{WR}$ high to next $\overline{WR}$ or $\overline{RD}$ low
14: Data valid to $\overline{WR}$ high set-up time
15: Data valid to $\overline{WR}$ high hold time
16: $\overline{RD}$ low to data bus out of TRI-STATE
17: $\overline{RD}$ high to TRI-STATE
18: $\overline{RD}$ low to data valid (access time)

Timing Diagrams

$V_A^+ = V_D^+ = +3.3V$, $t_R = t_F = 3$ ns, $C_L = 100$ pF for the $\overline{INT}$, DMARQ, D0–D15 outputs. (Continued)

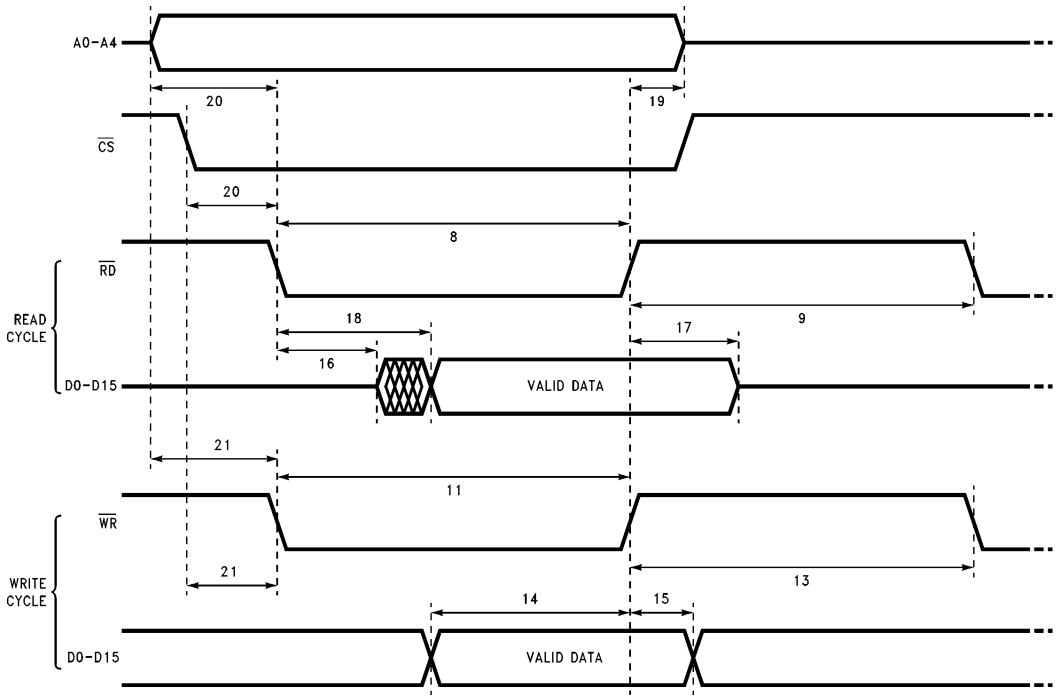

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FIGURE 8b. Non-Multiplexed Data Bus (ALE = 1)

8: $\overline{RD}$ pulse width
9: $\overline{RD}$ high to next $\overline{RD}$ or $\overline{WR}$ low
11: $\overline{WR}$ pulse width
13: $\overline{WR}$ high to next $\overline{WR}$ or $\overline{RD}$ low
14: Data valid to $\overline{WR}$ high set-up time
15: Data valid to $\overline{WR}$ high hold time
16: $\overline{RD}$ low to data bus out of TRI-STATE
17: $\overline{RD}$ high to TRI-STATE
18: $\overline{RD}$ low to data valid (access time)
19: Address invalid from $\overline{RD}$ or $\overline{WR}$ high (hold time)
20: $\overline{CS}$ low or address valid to $\overline{RD}$ low
21: $\overline{CS}$ low or address valid to $\overline{WR}$ low

$V_A^+ = V_D^+ = +3.3V$, $t_R = t_F = 3$ ns, $C_L = 100$ pF for the $\overline{INT}$, DMARQ, D0–D15 outputs.

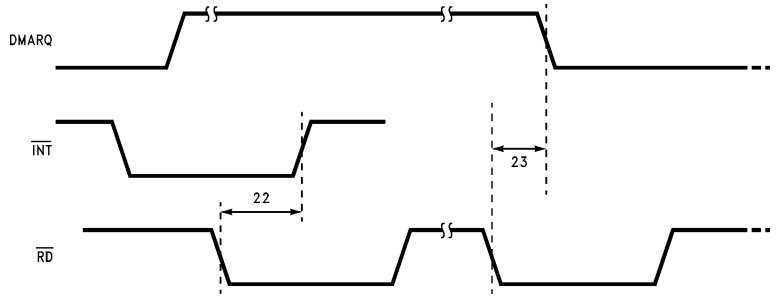

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FIGURE 8c. Interrupt and DMARQ

22: $\overline{INT}$ high from $\overline{RD}$ low
23: DMARQ low from $\overline{RD}$ low

Pin Description

V_A^+ V_D^+ These are the analog and digital supply voltage pins. The LM12L454/8's supply voltage operating range is $+3.0V$ to $+5.5V$. Accuracy is guaranteed only if V_A^+ and V_D^+ are connected to the same power supply. Each pin should have a parallel combination of 10 μF (electrolytic or tantalum) and 0.1 μF (ceramic) bypass capacitors connected between it and ground.

D0–D15 The internal data input/output TRI-STATE buffers are connected to these pins. These buffers are designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. These pins allows the user a means of instruction input and data output. With a logic **high** applied to the **BW** pin, data lines D8–D15 are placed in a high impedance state and data lines D0–D7 are used for instruction input and data output when the LM12L454/8 is connected to an 8-bit wide data bus. A logic **low** on the **BW** pin allows the LM12L454/8 to exchange information over a 16-bit wide data bus.

$\overline{RD}$ This is the input for the active low READ bus control signal. The data input/output TRI-STATE buffers, as selected by the logic signal applied to the **BW** pin, are enabled when $\overline{RD}$ and $\overline{CS}$ are both low. This allows the LM12L454/8 to transmit information onto the databus.

$\overline{WR}$ This is the input for the active low WRITE bus control signal. The data input/output TRI-STATE buffers, as selected by the logic signal applied to the **BW** pin, are enabled when $\overline{WR}$ and $\overline{CS}$ are both low. This allows the LM12L454/8 to receive information from the databus.

$\overline{CS}$ This is the input for the active low Chip Select control signal. A logic low should be applied to this pin only during a READ or WRITE access to the LM12L454/8. The internal clocking is halted and conversion stops while Chip Select is low. Conversion resumes when the Chip Select input signal returns high.

ALE This is the Address Latch Enable input. It is used in systems containing a multiplexed databus. When ALE is asserted **high**, the LM12L454/8 accepts information on the databus as a valid address. A high-to-low transition will latch the address data on A0–A4 and the logic state on the $\overline{CS}$ input. Any changes on A0–A4 and $\overline{CS}$ while ALE is low will not affect the LM12L454/8. See *Figure 8a*. When a non-multiplexed bus is used, ALE is continuously asserted **high**. See *Figure 8b*.

CLK This is the external clock input pin. The LM12L454/8 operates with an input clock frequency in the range of 0.05 MHz to 8 MHz.

A0–A4 These are the LM12L454/8's address lines. They are used to access all internal registers, Conversion FIFO, and Instruction **RAM**.

SYNC This is the synchronization input/output. When used as an output, it is designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. SYNC is an **input** if the Configuration register's "I/O Select" bit is **low**. A rising edge on this pin causes the internal S/H to hold the input signal. The next rising clock edge either starts a conversion or makes a comparison to a programmable limit depending on which function is requested by a programming instruction. This pin will be an **output** if "I/O Select" is set **high**. The SYNC output goes high when a conversion or a comparison is started and low when completed. (See Section 2.2). An internal reset after power is first applied to the LM12L454/8 automatically sets this pin as an input.

BW This is the Bus Width input pin. This input allows the LM12L454/8 to interface directly with either an 8- or 16-bit databus. A logic high sets the width to 8 bits and places D8–D15 in a high impedance state. A logic low sets the width to 16 bits.

$\overline{INT}$ This is the active low interrupt output. This output is designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. An interrupt signal is generated any time a non-masked interrupt condition takes place. There are eight different conditions that can cause an interrupt. Any interrupt is reset by reading the Interrupt Status register. (See Section 2.3.)

DMARQ This is the active high Direct Memory Access Request output. This output is designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. It goes high whenever the number of conversion results in the conversion FIFO equals a programmable value stored in the Interrupt Enable register. It returns to a logic low when the FIFO is empty.

GND This is the LM12L454/8 ground connection. It should be connected to a low resistance and inductance analog ground return that connects directly to the system power supply ground.

IN0–IN7 (IN0–IN3 LM12L454) These are the eight (LM12L458) or four (LM12L454) analog inputs. A given channel is selected through the instruction RAM. Any of the channels can be configured as an independent single-ended input. Any pair of channels, whether adjacent or non-adjacent, can operate as a fully differential pair.

S/H IN+ S/H IN− These are the LM12L454's non-inverting and inverting inputs to the internal S/H.

MUXOUT+ MUXOUT− These are the LM12L454's non-inverting and inverting outputs from the internal multiplexer.

$V_{REF}-$ This is the negative reference input. The LM12L454/8 operate with $0V \leq V_{REF}- \leq V_{REF}+$. This pin should be bypassed to ground with a parallel combination of 10 μF and 0.1 μF (ceramic) capacitors.

$V_{REF}+$ This is the positive reference input. The LM12L454/8 operate with $0V \leq V_{REF}+ \leq V_A^+$. This pin should be bypassed to ground with a parallel combination of 10 μF and 0.1 μF (ceramic) capacitors.

N.C. This is a no connect pin.

Application Information

1.0 Functional Description

The LM12L454 and LM12L458 are multi-functional Data Acquisition Systems that include a fully differential 12-bit-plus-sign self-calibrating analog-to-digital converter (ADC) with a two's-complement output format, an 8-channel (LM12L458) or a 4-channel (LM12L454) analog multiplexer, a first-in-first-out (FIFO) register that can store 32 conversion results, and an Instruction RAM that can store as many as eight instructions to be sequentially executed. The LM12L454 also has a differential multiplexer output and a differential S/H input. All of this circuitry operates on only a single +3.3V power supply.

The LM12L454/8 have three modes of operation:

12-bit + sign with correction
8-bit + sign without correction
8-bit + sign comparison mode ("watchdog" mode)

The fully differential 12-bit-plus-sign ADC uses a charge re-distribution topology that includes calibration capabilities. Charge re-distribution ADCs use a capacitor ladder in place of a resistor ladder to form an internal DAC. The DAC is used by a successive approximation register to generate intermediate voltages between the voltages applied to V_{REF-} and V_{REF+}. These intermediate voltages are compared against the sampled analog input voltage as each bit is generated. The number of intermediate voltages and comparisons equals the ADC's resolution. The correction of each bit's accuracy is accomplished by calibrating the capacitor ladder used in the ADC.

Two different calibration modes are available; one compensates for offset voltage, or zero error, while the other corrects both offset error and the ADC's linearity error.

When correcting offset only, the offset error is measured once and a correction coefficient is created. During the full calibration, the offset error is measured eight times, averaged, and a correction coefficient is created. After completion of either calibration mode, the offset correction coefficient is stored in an internal offset correction register.

The LM12L454/8's overall linearity correction is achieved by correcting the internal DAC's capacitor mismatch. Each capacitor is compared eight times against all remaining smaller value capacitors and any errors are averaged. A correction coefficient is then created and stored in one of the thirteen internal linearity correction registers. An internal state machine, using patterns stored in an internal 16 x 8-bit ROM, executes each calibration algorithm.

Once calibrated, an internal arithmetic logic unit (ALU) uses the offset correction coefficient and the 13 linearity correction coefficients to reduce the conversion's offset error and linearity error, in the background, during the 12-bit + sign conversion. The 8-bit + sign conversion and comparison modes use only the offset coefficient. The 8-bit + sign mode performs a conversion in less than half the time used by the 12-bit + sign conversion mode.

The LM12L454/8's "watchdog" mode is used to monitor a single-ended or differential signal's amplitude. Each sampled signal has two limits. An interrupt can be generated if the input signal is above or below either of the two limits. This allows interrupts to be generated when analog voltage inputs are "inside the window" or, alternatively, "outside the window". After a "watchdog" mode interrupt, the processor can then request a conversion on the input signal and read the signal's magnitude.

The analog input multiplexer can be configured for any combination of single-ended or fully differential operation. Each input is referenced to ground when a multiplexer channel operates in the single-ended mode. Fully differential analog input channels are formed by pairing any two channels together.

The LM12L454's multiplexer outputs and S/H inputs (MUXOUT+, MUXOUT− and S/H IN+, S/H IN−) provide the option for additional analog signal processing. Fixed-gain amplifiers, programmable-gain amplifiers, filters, and other processing circuits can operate on the signal applied to the selected multiplexer channel(s). If external processing is not used, connect MUXOUT+ to S/H IN+ and MUXOUT− to S/H IN−.

The LM12L454/8's internal S/H is designed to operate at its minimum acquisition time (1.5 μs, 12 bits) when the source impedance, R_S, is $\leq 80\Omega$ ($f_{CLK} \leq 6$ MHz). When $80\Omega < R_S \leq 5.56\ k\Omega$, the internal S/H's acquisition time can be increased to a maximum of 6.5 μs (12 bits, $f_{CLK} =$ 6 MHz). See Section 2.1 (Instruction RAM "00") Bits 12–15 for more information.

Microprocessor overhead is reduced through the use of the internal conversion FIFO. Thirty-two consecutive conversions can be completed and stored in the FIFO without any microprocessor intervention. The microprocessor can, at any time, interrogate the FIFO and retrieve its contents. It can also wait for the LM12L454/8 to issue an interrupt when the FIFO is full or after any number ($\leq$32) of conversions have been stored.

Conversion sequencing, internal timer interval, multiplexer configuration, and many other operations are programmed and set in the Instruction RAM.

A diagnostic mode is available that allows verification of the LM12L458's operation. The diagnostic mode is disabled in the LM12L454. This mode internally connects the voltages present at the V_{REF+}, V_{REF-}, and GND pins to the internal V_{IN+} and V_{IN-} S/H inputs. This mode is activated by setting the Diagnostic bit (Bit 11) in the Configuration register to a "1". More information concerning this mode of operation can be found in Section 2.2.

2.0 Internal User-Programmable Registers

2.1 INSTRUCTION RAM

The instruction RAM holds up to eight sequentially executable instructions. Each 48-bit long instruction is divided into three 16-bit sections. READ and WRITE operations can be issued to each 16-bit section using the instruction's address and the 2-bit ''RAM pointer'' in the Configuration register. The eight instructions are located at addresses 0000 through 0111 (A4–A1, BW = 0) when using a 16-bit wide data bus or at addresses 00000 through 01111 (A4–A0, BW = 1) when using an 8-bit wide data bus. They can be accessed and programmed in random order.

Any Instruction RAM READ or WRITE can affect the sequencer's operation:

The Sequencer should be stopped by setting the RESET bit to a ''1'' or by resetting the START bit in the Configuration Register and waiting for the current instruction to finish execution before any Instruction RAM READ or WRITE is initiated.

A soft RESET should be issued by writing a ''1'' to the Configuration Register's RESET bit after any READ or WRITE to the Instruction RAM.

The three sections in the Instruction RAM are selected by the Configuration Register's 2-bit ''RAM Pointer'', bits D8 and D9. The first 16-bit Instruction RAM section is selected with the RAM Pointer equal to ''00''. This section provides multiplexer channel selection, as well as resolution, acquisition time, etc. The second 16-bit section holds ''watchdog'' limit #1, its sign, and an indicator that shows that an interrupt can be generated if the input signal is greater or less than the programmed limit. The third 16-bit section holds ''watchdog'' limit #2, its sign, and an indicator that shows that an interrupt can be generated if the input signal is greater or less than the programmed limit.

Instruction RAM ''00''

Bit 0 is the LOOP bit. It indicates the last instruction to be executed in any instruction sequence when it is set to a ''1''. The next instruction to be executed will be instruction 0.

Bit 1 is the PAUSE bit. This controls the Sequencer's operation. When the PAUSE bit is set (''1''), the Sequencer will stop after reading the current instruction, but before executing it and the start bit, in the Configuration register, is automatically reset to a ''0''. Setting the PAUSE also causes an interrupt to be issued. The Sequencer is restarted by placing a ''1'' in the Configuration register's Bit 0 (Start bit).

After the Instruction RAM has been programmed and the RESET bit is set to ''1'', the Sequencer retrieves Instruction 000, decodes it, and waits for a ''1'' to be placed in the Configuration's START bit. The START bit value of ''0'' ''overrides'' the action of Instruction 000's PAUSE bit when the Sequencer is started. Once started, the Sequencer executes Instruction 000 and retrieves, decodes, and executes each of the remaining instructions. No PAUSE Interrupt (INT 5) is generated the first time the Sequencer executes Instruction 000 having a PAUSE bit set to ''1''. When the Sequencer encounters a LOOP bit or completes all eight instructions, Instruction 000 is retrieved and decoded. A set PAUSE bit in Instruction 000 now halts the Sequencer before the instruction is executed.

Bits 2–4 select which of the eight input channels (''000'' to ''111'' for IN0–IN7) will be configured as non-inverting inputs to the LM12L458's ADC. (See Page 22, Table I.) They select which of the four input channels (''000'' to ''011'' for IN0–IN4) will be configured as non-inverting inputs to the LM12L454's ADC. (See Page 22, Table II.)

Bits 5–7 select which of the seven input channels (''001'' to ''111'' for IN1 to IN7) will be configured as inverting inputs to the LM12L458's ADC. (See Page 22, Table I.) They select which of the three input channels (''001'' to ''011'' for IN1–IN4) will be configured as inverting inputs to the LM12L454's ADC. (See Page 22, Table II.) Fully differential operation is created by selecting two multiplexer channels, one operating in the non-inverting mode and the other operating in the inverting mode. A code of ''000'' selects ground as the inverting input for single ended operation.

Bit 8 is the SYNC bit. Setting Bit 8 to ''1'' causes the Sequencer to suspend operation at the end of the internal S/H's acquisition cycle and to wait until a rising edge appears at the SYNC pin. When a rising edge appears, the S/H acquires the input signal magnitude and the ADC performs a conversion on the clock's next rising edge. When the SYNC pin is used as an input, the Configuration register's ''I/O Select'' bit (Bit 7) must be set to a ''0''. With SYNC configured as an input, it is possible to synchronize the start of a conversion to an external event. This is useful in applications such as digital signal processing (DSP) where the exact timing of conversions is important.

When the LM12L454/8 are used in the ''watchdog'' mode with external synchronization, two rising edges on the SYNC input are required to initiate two comparisons. The first rising edge initiates the comparison of the selected analog input signal with Limit #1 (found in Instruction RAM ''01'') and the second rising edge initiates the comparison of the same analog input signal with Limit #2 (found in Instruction RAM ''10'').

Bit 9 is the TIMER bit. When Bit 9 is set to ''1'', the Sequencer will halt until the internal 16-bit Timer counts down to zero. During this time interval, no ''watchdog'' comparisons or analog-to-digital conversions will be performed.

Bit 10 selects the ADC conversion resolution. Setting Bit 10 to ''1'' selects 8-bit + sign and when reset to ''0'' selects 12-bit + sign.

Bit 11 is the ''watchdog'' comparison mode enable bit. When operating in the ''watchdog'' comparison mode, the selected analog input signal is compared with the programmable values stored in Limit #1 and Limit #2 (see Instruction RAM ''01'' and Instruction RAM ''10''). Setting Bit 11 to ''1'' causes two comparisons of the selected analog input signal with the two stored limits. When Bit 11 is reset to ''0'', an 8-bit + sign or 12-bit + sign (depending on the state of Bit 10 of Instruction RAM ''00'') conversion of the input signal can take place.

2.0 Internal User-Programmable Registers (Continued)

A4	A3	A2	A1	Purpose	Type	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0 to 1	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 00)	R/W	Acquisition Time				Watch-dog	8/12	Timer	Sync	$V_{IN}-$ (MUXOUT−)*			$V_{IN}+$ (MUXOUT+)*			Pause	Loop
0	0 to 1	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 01)	R/W	Don't Care						> / <	Sign	Limit #1							
0	0 to 1	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 10)	R/W	Don't Care						> / <	Sign	Limit #2							
1	0	0	0	Configuration Register	R/W	Don't Care				DIAG†	Test = 0	RAM Pointer		I/O Sel	Auto $Zero_{ec}$	Chan Mask	Stand-by	Full CAL	Auto-Zero	Reset	Start
1	0	0	1	Interrupt Enable Register	R/W	Number of Conversions in Conversion FIFO to Generate INT2					Sequencer Address to Generate INT1			INT7	Don't Care	INT5	INT4	INT3	INT2	INT1	INT0
1	0	1	0	Interrupt Status Register	R	Actual Number of Conversion Results in Conversion FIFO					Address of Sequencer Instruction being Executed			INST7	"0"	INST5	INST4	INST3	INST2	INST1	INST0
1	0	1	1	Timer Register	R/W	Timer Preset High Byte								Timer Preset Low Byte							
1	1	0	0	Conversion FIFO	R	Address or Sign			Sign	Conversion Data: MSBs				Conversion Data: LSBs							
1	1	0	1	Limit Status Register	R	Limit #2: Status								Limit #1: Status							

*LM12L454 (Refer to Table II).
†LM12L458 only. Must be set to "0" for the LM12L454.

FIGURE 9. LM12L454/8 Memory Map for 16-Bit Wide Databus (BW = "0", Test Bit = "0" and A0 = Don't Care)

2.0 Internal User-Programmable Registers (Continued)

A4	A3	A2	A1	A0	Purpose	Type	D7	D6	D5	D4	D3	D2	D1	D0
0	0 to 1	0 to 1	0 to 1	0	Instruction RAM (RAM Pointer = 00)	R/W	V_{IN-} (MUXOUT−)*			V_{IN+} (MUXOUT+)*			Pause	Loop
0	0 to 1	0 to 1	0 to 1	1		R/W	Acquisition Time				Watch-dog	8/12	Timer	Sync
0	0 to 1	0 to 1	0 to 1	0	Instruction RAM (RAM Pointer = 01)	R/W	Comparison Limit #1							
0	0 to 1	0 to 1	0 to 1	1		R/W	Don't Care						> / <	Sign
0	0 to 1	0 to 1	0 to 1	0	Instruction RAM (RAM Pointer = 10)	R/W	Comparison Limit #2							
0	0 to 1	0 to 1	0 to 1	1		R/W	Don't Care						> / <	Sign
1	0	0	0	0	Configuration Register	R/W	I/O Sel	Auto $Zero_{ec}$	Chan Mask	Stand-by	Full Cal	Auto-Zero	Reset	Start
1	0	0	0	1		R/W	Don't Care				DIAG†	Test = 0	RAM Pointer	
1	0	0	1	0	Interrupt Enable Register	R/W	INT7	Don't Care	INT5	INT4	INT3	INT2	INT1	INT0
1	0	0	1	1		R/W	Number of Conversions in Conversion FIFO to Generate INT2					Sequencer Address to Generate INT1		
1	0	1	0	0	Interrupt Status Register	R	INST7	"0"	INST5	INST4	INST3	INST2	INST1	INST0
1	0	1	0	1		R	Actual Number of Conversions Results in Conversion FIFO					Address of Sequencer Instruction being Executed		
1	0	1	1	0	Timer Register	R/W	Timer Preset: Low Byte							
1	0	1	1	1		R/W	Timer Preset: High Byte							
1	1	0	0	0	Conversion FIFO	R	Conversion Data: LSBs							
1	1	0	0	1		R	Address or Sign			Sign	Conversion Data: MSBs			
1	1	0	1	0	Limit Status Register	R	Limit #1 Status							
1	1	0	1	1		R	Limit #2 Status							

*LM12L454 (Refer to Table II).

†LM12L458 only. Must be set to "0" for the LM12L454.

FIGURE 10. LM12L454/8 Memory Map for 8-Bit Wide Databus (BW = "1" and Test Bit = "0")

2.0 Internal User-Programmable Registers (Continued)

Bits 12–15 are used to store the user-programmable acquisition time. The Sequencer keeps the internal S/H in the acquisition mode for a fixed number of clock cycles (nine clock cycles, for 12-bit + sign conversions and two clock cycles for 8-bit + sign conversions or ''watchdog'' comparisons) plus a variable number of clock cycles equal to twice the value stored in Bits 12–15. Thus, the S/H's acquisition time is (9 + 2D) clock cycles for 12-bit + sign conversions and (2 + 2D) clock cycles for 8-bit + sign conversions or ''watchdog'' comparisons, where D is the value stored in Bits 12–15. The minimum acquisition time compensates for the typical internal multiplexer series resistance of 2 kΩ, and any additional delay created by Bits 12–15 compensates for source resistances greater than 80Ω. (For this acquisition time discussion, numbers in ( ) are shown for the LM12L454/8 operating at 6 MHz. The necessary acquisition time is determined by the source impedance at the multiplexer input. If the source resistance (R_S) < 80Ω and the clock frequency is 6 MHz, the value stored in bits 12–15 (D) can be 0000. If R_S > 80Ω, the following equations determine the value that should be stored in bits 12–15.

$$D = 0.45 \times R_S \times f_{CLK}$$

for 12-bits + sign

$$D = 0.36 \times R_S \times f_{CLK}$$

for 8-bits + sign and ''watchdog''

R_S is in kΩ and f_{CLK} is in MHz. Round the result to the next higher integer value. If D is greater than 15, it is advisable to lower the source impedance by using an analog buffer between the signal source and the LM12L458's multiplexer inputs. The value of D can also be used to compensate for the settling or response time of external processing circuits connected between the LM12L454's MUXOUT and S/H IN pins.

Instruction RAM ''01''

The second Instruction RAM section is selected by placing a ''01'' in Bits 8 and 9 of the Configuration register.

Bits 0–7 hold ''watchdog'' **limit #1**. When Bit 11 of Instruction RAM ''00'' is set to a ''1'', the LM12L454/8 performs a ''watchdog'' comparison of the sampled analog input signal with the limit #1 value first, followed by a comparison of the same sampled analog input signal with the value found in limit #2 (Instruction RAM ''10'').

Bit 8 holds limit #1's sign.

Bit 9's state determines the limit condition that generates a ''watchdog'' interrupt. A ''1'' causes a voltage greater than limit #1 to generate an interrupt, while a ''0'' causes a voltage less than limit #1 to generate an interrupt.

Bits 10–15 are not used.

Instruction RAM ''10''

The third Instruction RAM section is selected by placing a ''10'' in Bits 8 and 9 of the Configuration register.

Bits 0–7 hold ''watchdog'' **limit #2**. When Bit 11 of Instruction RAM ''00'' is set to a ''1'', the LM12L454/8 performs a ''watchdog'' comparison of the sampled analog input signal with the limit #1 value first (Instruction RAM ''01''), followed by a comparison of the same sampled analog input signal with the value found in limit #2.

Bit 8 holds limit #2's sign.

Bit 9's state determines the limit condition that generates a ''watchdog'' interrupt. A ''1'' causes a voltage greater than limit #2 to generate an interrupt, while a ''0'' causes a voltage less than limit #2 to generate an interrupt.

Bits 10–15 are not used.

2.2 CONFIGURATION REGISTER

The Configuration register, 1000 (A4–A1, BW = 0) or 1000x (A4–A0, BW = 1) is a 16-bit control register with read/write capability. It acts as the LM12L454's and LM12L458's ''control panel'' holding global information as well as start/stop, reset, self-calibration, and stand-by commands.

Bit 0 is the START/STOP bit. Reading Bit 0 returns an indication of the Sequencer's status. A ''0'' indicates that the Sequencer is stopped and waiting to execute the next instruction. A ''1'' shows that the Sequencer is running. Writing a ''0'' halts the Sequencer when the current instruction has finished execution. The next instruction to be executed is pointed to by the instruction pointer found in the status register. A ''1'' restarts the Sequencer with the instruction currently pointed to by the instruction pointer. (See Bits 8–10 in the Interrupt Status register.)

Bit 1 is the LM12L454/8's system RESET bit. Writing a ''1'' to Bit 1 stops the Sequencer (resetting the Configuration register's START/STOP bit), resets the Instruction pointer to ''000'' (found in the Interrupt Status register), clears the Conversion FIFO, and resets all interrupt flags. The RESET bit will return to ''0'' after two clock cycles unless it is forced high by writing a ''1'' into the Configuration register's Stand-by bit. A reset signal is internally generated when power is first applied to the part. No operation should be started until the RESET bit is ''0''.

Writing a ''1'' to **Bit 2** initiates an auto-zero offset voltage calibration. Unlike the eight-sample auto-zero calibration performed during the full calibration procedure, Bit 2 initiates a ''short'' auto-zero by sampling the offset once and creating a correction coefficient (full calibration averages eight samples of the converter offset voltage when creating a correction coefficient). If the Sequencer is running when Bit 2 is set to ''1'', an auto-zero starts immediately after the conclusion of the currently running instruction. Bit 2 is reset automatically to a ''0'' and an interrupt flag (Bit 3, in the Interrupt Status register) is set at the end of the auto-zero (76 clock cycles). After completion of an auto-zero calibration, the Sequencer fetches the next instruction as pointed to by the Instruction RAM's pointer and resumes execution. If the Sequencer is stopped, an auto-zero is performed immediately at the time requested.

Writing a ''1'' to **Bit 3** initiates a complete calibration process that includes a ''long'' auto-zero offset voltage correction (this calibration averages eight samples of the comparator offset voltage when creating a correction coefficient) followed by an ADC linearity calibration. This complete calibration is started after the currently running instruction is completed if the Sequencer is running when Bit 3 is set to ''1''. Bit 3 is reset automatically to a ''0'' and an interrupt flag (Bit 4, in the Interrupt Status register) will be generated at the end of the calibration procedure (4944 clock cycles). After completion of a full auto-zero and linearity calibration, the Sequencer fetches the next instruction as pointed to by the Instruction RAM's pointer and resumes execution. If the Sequencer is stopped, a full calibration is performed immediately at the time requested.

2.0 Internal User-Programmable Registers (Continued)

Bit 4 is the Standby bit. Writing a ''1'' to Bit 4 immediately places the LM12L454/8 in Standby mode. Normal operation returns when Bit 4 is reset to a ''0''. The Standby command (''1'') disconnects the external clock from the internal circuitry, decreases the LM12L454/8's internal analog circuitry power supply current, and preserves all internal RAM contents. After writing a ''0'' to the Standby bit, the LM12L454/8 returns to an operating state identical to that caused by exercising the RESET bit. A Standby completion interrupt is issued after a power-up completion delay that allows the analog circuitry to settle. The Sequencer should be restarted only after the Standby completion is issued. The Instruction RAM can still be accessed through read and write operations while the LM12L454/8 are in Standby Mode.

Bit 5 is the Channel Address Mask. If Bit 5 is set to a ''1'', Bits 13–15 in the conversion FIFO will be equal to the sign bit (Bit 12) of the conversion data. Resetting Bit 5 to a ''0'' causes conversion data Bits 13 through 15 to hold the instruction pointer value of the instruction to which the conversion data belongs.

Bit 6 is used to select a ''short'' auto-zero correction for every conversion. The Sequencer automatically inserts an auto-zero before every conversion or ''watchdog'' comparison if Bit 6 is set to ''1''. No automatic correction will be performed if Bit 6 is reset to ''0''.

The LM12L454/8's offset voltage, after calibration, has a typical drift of 0.1 LSB over a temperature range of −40°C to +85°C. This small drift is less than the variability of the change in offset that can occur when using the auto-zero correction with each conversion. This variability is the result of using only one sample of the offset voltage to create a correction value. This variability decreases when using the full calibration mode because eight samples of the offset voltage are taken, averaged, and used to create a correction value.

Bit 7 is used to program the SYNC pin (29) to operate as either an input or an output. The SYNC pin becomes an output when Bit 7 is a ''1'' and an input when Bit 7 is a ''0''. With SYNC programmed as an input, the rising edge of any logic signal applied to pin 29 will start a conversion or ''watchdog'' comparison. Programmed as an output, the logic level at pin 29 will go high at the start of a conversion or ''watchdog'' comparison and remain high until either have finished. See Instruction RAM ''00'', Bit 8.

Bits 8 and **9** form the RAM Pointer that is used to select each of a 48-bit instruction's three 16-bit sections during read or write actions. A ''00'' selects Instruction RAM section one, ''01'' selects section two, and ''10'' selects section three.

Bit 10 activates the Test mode that is used only during production testing. Leave this bit reset to ''0''.

Bit 11 is the Diagnostic bit and is available only in the LM12L458. It can be activated by setting it to a ''1'' (the Test bit must be reset to a ''0''). The Diagnostic mode, along with a correctly chosen instruction, allows verification that the LM12L458's ADC is performing correctly. When activated, the inverting and non-inverting inputs are connected as shown in Table I. As an example, an instruction with ''001'' for both $V_{IN}+$ and $V_{IN}-$ while using the Diagnostic mode typically results in a full-scale output.

2.3 INTERRUPTS

The LM12L454 and LM12L458 have eight possible interrupts, all with the same priority. Any of these interrupts will cause a hardware interrupt to appear on the $\overline{INT}$ pin (31) if they are not masked (by the Interrupt Enable register). The Interrupt Status register is then read to determine which of the eight interrupts has been issued.

TABLE I. LM12L458 Input Multiplexer Channel Configuration Showing Normal Mode and Diagnostic Mode

Channel Selection Data	Normal Mode		Diagnostic Mode	
	$V_{IN}+$	$V_{IN}-$	$V_{IN}+$	$V_{IN}-$
000	IN0	GND		
001	IN1	IN1	$V_{REF}+$	$V_{REF}-$
010	IN2	IN2	IN2	IN2
011	IN3	IN3	IN3	IN3
100	IN4	IN4	IN4	IN4
101	IN5	IN5	IN5	IN5
110	IN6	IN6	IN6	IN6
111	IN7	IN7	IN7	IN7

TABLE II. LM12L454 Input Multiplexer Channel Configuration

Channel Selection Data	MUX+	MUX−
000	IN0	GND
001	IN1	IN1
010	IN2	IN2
011	IN3	IN3
1XX	OPEN	OPEN

The Interrupt Status register, 1010 (A4–A1, BW = 0) or 1010x (A4–A0, BW = 1) must be cleared by reading it after writing to the Interrupt Enable register. This removes any spurious interrupts on the $\overline{INT}$ pin generated during an Interrupt Enable register access.

Interrupt 0 is generated whenever the analog input voltage on a selected multiplexer channel crosses a limit while the LM12L454/8 are operating in the ''watchdog'' comparison mode. Two sequential comparisons are made when the LM12L454/8 are executing a ''watchdog'' instruction. Depending on the logic state of Bit 9 in the Instruction RAM's second and third sections, an interrupt will be generated either when the input signal's magnitude is greater than or less than the programmable limits. (See the Instruction RAM, Bit 9 description.) The Limit Status register will indicate which preprogrammed limit, #1 or #2 and which instruction was executing when the limit was crossed.

Interrupt 1 is generated when the Sequencer reaches the instruction counter value specified in the Interrupt Enable register's bits 8–10. This flag appears before the instruction's execution.

Interrupt 2 is activated when the Conversion FIFO holds a number of conversions equal to the programmable value

2.0 Internal User-Programmable Registers (Continued)

stored in the Interrupt Enable register's Bits 11–15. This value ranges from 0001 to 1111, representing 1 to 31 conversions stored in the FIFO. A user-programmed value of 0000 has no meaning. See Section 3.0 for more FIFO information.

The completion of the short, single-sampled auto-zero calibration generates **Interrupt 3**.

The completion of a full auto-zero and linearity self-calibration generates **Interrupt 4**.

Interrupt 5 is generated when the Sequencer encounters an instruction that has its Pause bit (Bit 1 in Instruction RAM "00") set to "1".

Interrupt 7 is issued after a short delay (10 ms typ) while the LM12L454/8 returns from Standby mode to active operation using the Configuration register's Bit 4. This short delay allows the internal analog circuitry to settle sufficiently, ensuring accurate conversion results.

2.4 INTERRUPT ENABLE REGISTER

The Interrupt Enable register at address location 1001 (A4–A1, BW = 0) or 1001x (A4–A0, BW = 1) has READ/WRITE capability. An individual interrupt's ability to produce an external interrupt at pin 31 ($\overline{\text{INT}}$) is accomplished by placing a "1" in the appropriate bit location. Any of the internal interrupt-producing operations will set their corresponding bits to "1" in the Interrupt Status register regardless of the state of the associated bit in the Interrupt Enable register. See Section 2.3 for more information about each of the eight internal interrupts.

Bit 0 enables an external interrupt when an internal "watchdog" comparison limit interrupt has taken place.

Bit 1 enables an external interrupt when the Sequencer has reached the address stored in Bits 8–10 of the Interrupt Enable register.

Bit 2 enables an external interrupt when the Conversion FIFO's limit, stored in Bits 11–15 of the Interrupt Enable register, has been reached.

Bit 3 enables an external interrupt when the single-sampled auto-zero calibration has been completed.

Bit 4 enables an external interrupt when a full auto-zero and linearity self-calibration has been completed.

Bit 5 enables an external interrupt when an internal Pause interrupt has been generated.

Bit 6 is a "Don't Care".

Bit 7 enables an external interrupt when the LM12L454/8 return from power-down to active mode.

Bits 8–10 form the storage location of the user-programmable value against which the Sequencer's address is compared. When the Sequencer reaches an address that is equal to the value stored in Bits 8–10, an internal interrupt is generated and appears in Bit 1 of the Interrupt Status register. If Bit 1 of the Interrupt Enable register is set to "1", an external interrupt will appear at pin 31 ($\overline{\text{INT}}$).

The value stored in bits 8–10 ranges from 000 to 111, representing 0 to 7 instructions stored in the Instruction RAM. After the Instruction RAM has been programmed and the RESET bit is set to "1", the Sequencer is started by placing a "1" in the Configuration register's START bit. Setting the INT 1 trigger value to 000 **does not generate** an INT 1 the **first** time the Sequencer retrieves and decodes Instruction 000. The Sequencer **generates** INT 1 (by placing a "1" in the Interrupt Status register's Bit 1) the **second time and after** the Sequencer encounters Instruction 000. It is important to remember that the Sequencer continues to operate even if an Instruction interrupt (INT 1) is internally or externally generated. The only mechanisms that stop the Sequencer are an instruction with the PAUSE bit set to "1" (halts before instruction execution), placing a "0" in the Configuration register's START bit, or placing a "1" in the Configuration register's RESET bit.

Bits 11–15 hold the number of conversions that must be stored in the Conversion FIFO in order to generate an internal interrupt. This internal interrupt appears in Bit 2 of the Interrupt Status register. If Bit 2 of the Interrupt Enable register is set to "1", an external interrupt will appear at pin 31 (INT).

2.5 INTERRUPT STATUS REGISTER

This read-only register is located at address 1010 (A4–A1, BW = 0) or 1010x (A4–A0, BW = 1). The corresponding flag in the Interrupt Status register goes high ("1") any time that an interrupt condition takes place, whether an interrupt is enabled or disabled in the Interrupt Enable register. Any of the active ("1") Interrupt Status register flags are reset to "0" whenever this register is read or a device reset is issued (see Bit 1 in the Configuration Register).

Bit 0 is set to "1" when a "watchdog" comparison limit interrupt has taken place.

Bit 1 is set to "1" when the Sequencer has reached the address stored in Bits 8–10 of the Interrupt Enable register.

Bit 2 is set to "1" when the Conversion FIFO's limit, stored in Bits 11–15 of the Interrupt Enable register, has been reached.

Bit 3 is set to "1" when the single-sampled auto-zero has been completed.

Bit 4 is set to "1" when an auto-zero and full linearity self-calibration has been completed.

Bit 5 is set to "1" when a Pause interrupt has been generated.

Bit 6 is a "Don't Care".

Bit 7 is set to "1" when the LM12L454/8 return from power-down to active mode.

Bits 8–10 hold the Sequencer's actual instruction address while it is running.

Bits 11–15 hold the actual number of conversions stored in the Conversion FIFO while the Sequencer is running.

2.6 LIMIT STATUS REGISTER

The read-only register is located at address 1101 (A4–A1, BW = 0) or 1101x (A4–A0, BW = 1). This register is used in tandem with the Limit #1 and Limit #2 registers in the Instruction RAM. Whenever a given instruction's input voltage exceeds the limit set in its corresponding Limit register (#1 or #2), a bit, corresponding to the instruction number, is set in the Limit Status register. Any of the active ("1") Limit Status flags are reset to "0" whenever this register is

2.0 Internal User-Programmable Registers (Continued)

read or a device reset is issued (see Bit 1 in the Configuration register). This register holds the status of limits #1 and #2 for each of the eight instructions.

Bits 0–7 show the Limit #1 status. Each bit will be set high (''1'') when the corresponding instruction's input voltage exceeds the threshold stored in the instruction's Limit #1 register. When, for example, instruction 3 is a ''watchdog'' operation (Bit 11 is set high) and the input for instruction 3 meets the magnitude and/or polarity data stored in instruction 3's Limit #1 register, Bit 3 in the Limit Status register will be set to a ''1''.

Bits 8–15 show the Limit #2 status. Each bit will be set high (''1'') when the corresponding instruction's input voltage exceeds the threshold stored in the instruction's Limit #2 register. When, for example, the input to instruction 6 meets the value stored in instruction 6's Limit #2 register, Bit 14 in the Limit Status register will be set to a ''1''.

2.7 TIMER

The LM12L454/8 have an on-board 16-bit timer that includes a 5-bit pre-scaler. It uses the clock signal applied to pin 23 as its input. It can generate time intervals of 0 through 2^{21} clock cycles in steps of 2^5. This time interval can be used to delay the execution of instructions. It can also be used to slow the conversion rate when converting slowly changing signals. This can reduce the amount of redundant data stored in the FIFO and retrieved by the controller.

The user-defined timing value used by the Timer is stored in the 16-bit READ/WRITE Timer register at location 1011 (A4–A1, BW = 0) or 1011x (A4–A0, BW = 1) and is preloaded automatically. Bits 0–7 hold the preset value's low byte and Bits 8–15 hold the high byte. The Timer is activated by the Sequencer only if the current instruction's Bit 9 is set (''1''). If the equivalent decimal value ''N'' ($0 \leq N \leq 2^{16} - 1$) is written inside the 16-bit Timer register and the Timer is enabled by setting an instruction's bit 9 to a ''1'', the Sequencer will delay the same instruction's execution by halting at state 3 (S3), as shown in *Figure 11,* for $32 \times N + 2$ clock cycles.

2.8 DMA

The DMA works in tandem with Interrupt 2. An active DMA Request on pin 32 (DMARQ) requires that the FIFO interrupt be enabled. The voltage on the DMARQ pin goes high when the number of conversions in the FIFO equals the 5-bit value stored in the Interrupt Enable register (bits 11–15). The voltage on the $\overline{INT}$ pin goes low at the same time as the voltage on the DMARQ pin goes high. The voltage on the DMARQ pin goes low when the FIFO is emptied. The Interrupt Status register must be read to clear the FIFO interrupt flag in order to enable the next DMA request.

DMA operation is optimized through the use of the 16-bit databus connection (a logic ''0'' applied to the BW pin). Using this bus width allows DMA controllers that have single address Read/Write capability to easily unload the FIFO. Using DMA on an 8-bit databus is more difficult. Two read operations (low byte, high byte) are needed to retrieve each conversion result from the FIFO. Therefore, the DMA controller must be able to repeatedly access two constant addresses when transferring data from the LM12L454/8 to the host system.

3.0 FIFO

The result of each conversion stored in an internal read-only FIFO (First-In, First-Out) register. It is located at 1100 (A4–A1, BW = 0) or 1100x (A4–A0, BW = 1). This register has 32 16-bit wide locations. Each location holds 13-bit data. Bits 0–3 hold the four LSB's in the 12 bits + sign mode or ''1110'' in the 8 bits + sign mode. Bits 4–11 hold the eight MSB's and Bit 12 holds the sign bit. Bits 13–15 can hold either the sign bit, extending the register's two's complement data format to a full sixteen bits or the instruction address that generated the conversion and the resulting data. These modes are selected according to the logic state of the Configuration register's Bit 5.

The FIFO status should be read in the Interrupt Status register (Bits 11–15) to determine the number of conversion results that are held in the FIFO before retrieving them. This will help prevent conversion data corruption that may take place if the number of reads are greater than the number of conversion results contained in the FIFO. Trying to read the FIFO when it is empty may corrupt new data being written into the FIFO. Writing more than 32 conversion data into the FIFO by the ADC results in loss of the first conversion data. Therefore, to prevent data loss, it is recommended that the LM12L454/8's interrupt capability be used to inform the system controller that the FIFO is full.

The lower portion (A0 = 0) of the data word (Bits 0–7) should be read first followed by a read of the upper portion (A0 = 1) when using the 8-bit bus width (BW = 1). Reading the upper portion first causes the data to shift down, which results in loss of the lower byte.

Bits 0–12 hold 12-bit + sign conversion data. **Bits 0–3** will be 1110 (LSB) when using 8-bit plus sign resolution.

Bits 13–15 hold either the instruction responsible for the associated conversion data or the sign bit. Either mode is selected with Bit 5 in the Configuration register.

Using the FIFO's full depth is achieved as follows. Set the value of the Interrupt Enable registers's Bits 11–15 to 1111 and the Interrupt Enable register's Bit 2 to a ''1''. This generates an external interrupt when the 31st conversion is stored in the FIFO. This gives the host processor a chance to send a ''0'' to the LM12L454/8's Start bit (Configuration register) and halt the ADC before it completes the 32nd conversion. The Sequencer halts after the current (32) conversion is completed. The conversion data is then transferred to the FIFO and occupies the 32nd location. FIFO overflow is avoided if the Sequencer is halted before the start of the 32nd conversion by placing a ''0'' in the Start bit (Configuration register). It is important to remember that the Sequencer **continues to operate even if a FIFO interrupt (INT 2) is internally or externally generated**. The only mechanisms that stop the Sequencer are an instruction with the PAUSE bit set to ''1'' (halts before instruction execution), placing a ''0'' in the Configuration register's START bit, or placing a ''1'' in the Configuration register's RESET bit.

4.0 Sequencer

The Sequencer uses a 3-bit counter (Instruction Pointer, or IP, in *Figure 7)* to retrieve the programmable conversion instructions stored in the Instruction RAM. The 3-bit counter is reset to 000 during chip reset or if the current executed instruction has its Loop bit (Bit 1 in any Instruction RAM ''00'') set high (''1''). It increments at the end of the currently executed instruction and points to the next instruction. It will continue to increment up to 111 unless an instruction's Loop bit is set. If this bit is set, the counter resets to ''000'' and execution begins again with the first instruction. If all instructions have their Loop bit reset to ''0'', the Sequencer will execute all eight instructions continuously. Therefore, it is important to realize that if less than eight instructions are programmed, the Loop bit on the last instruction must be set. Leaving this bit reset to ''0'' allows the Sequencer to execute ''unprogrammed'' instructions, the results of which may be unpredictable.

The Sequencer's Instruction Pointer value is readable at any time and is found in the Status register at Bits 8–10. The Sequencer can go through eight states during instruction execution:

State 0: The current instruction's first 16 bits are read from the Instruction RAM ''00''. This state is one clock cycle long.

State 1: Checks the state of the Calibration and Start bits. This is the ''rest'' state whenever the Sequencer is stopped using the reset, a Pause command, or the Start bit is reset low (''0''). When the Start bit is set to a ''1'', this state is one clock cycle long.

State 2: Perform calibration. If bit 2 or bit 6 of the Configuration register is set to a ''1'', state 2 is 76 clock cycles long. If the Configuration register's bit 3 is set to a ''1'', state 2 is 4944 clock cycles long.

State 3: Run the internal 16-bit Timer. The number of clock cycles for this state varies according to the value stored in the Timer register. The number of clock cycles is found by using the expression below

$$32T + 2$$

where $0 \leq T \leq 2^{16} - 1$.

State 7: Run the acquisition delay and read Limit #1's value if needed. The number of clock cycles for 12-bit + sign mode varies according to

$$9 + 2D$$

where D is the user-programmable 4-bit value stored in bits 12–15 of Instruction RAM ''00'' and is limited to $0 \leq D \leq 15$.

The number of clock cycles for 8-bit + sign or ''watchdog'' mode varies according to

$$2 + 2D$$

where D is the user-programmable 4-bit value stored in bits 12–15 of Instruction RAM ''00'' and is limited to $0 \leq D \leq 15$.

State 6: Perform first comparison. This state is 5 clock cycles long.

State 4: Read Limit #2. This state is 1 clock cycle long.

State 5: Perform a conversion or second comparison. This state takes 44 clock cycles when using the 12-bit + sign mode or 21 clock cycles when using the 8-bit + sign mode. The ''watchdog'' mode takes 5 clock cycles.

4.0 Sequencer (Continued)

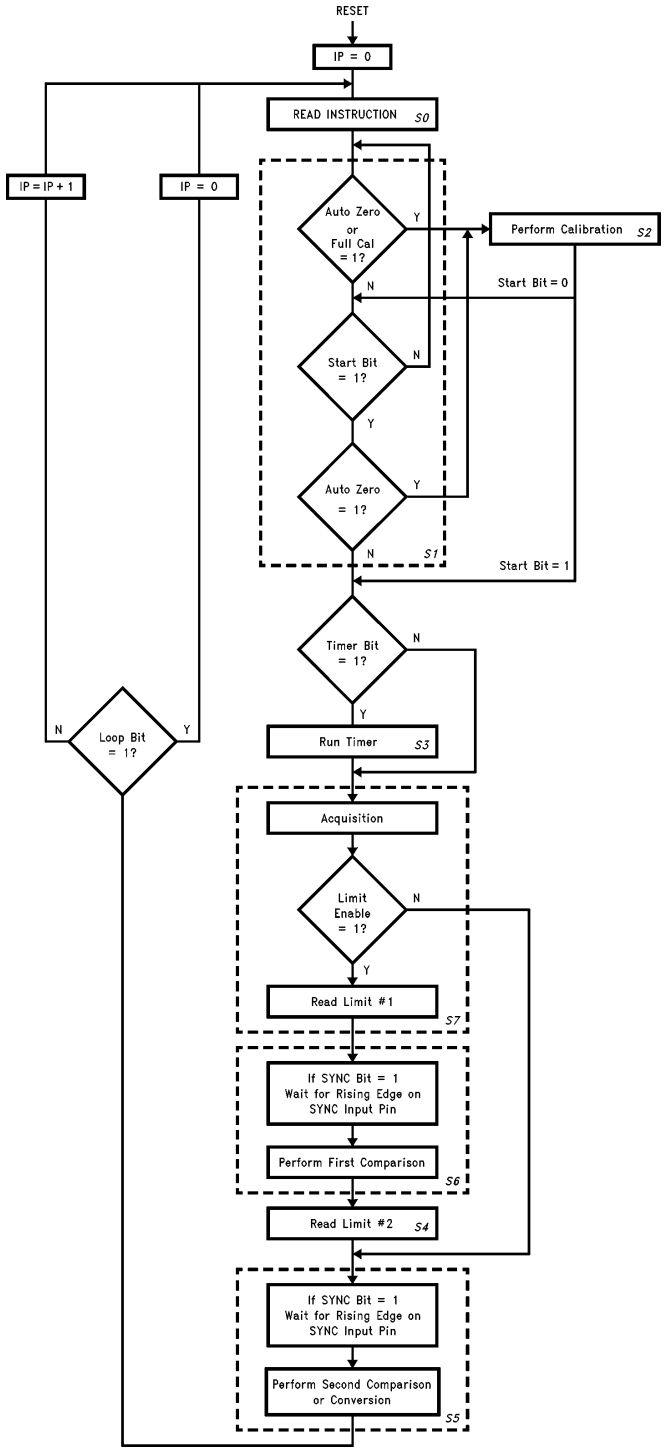

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FIGURE 11. Sequencer Logic Flow Chart (IP = Instruction Pointer)

5.0 Analog Considerations

5.1 REFERENCE VOLTAGE

The difference in the voltages applied to the V_{REF+} and V_{REF-} defines the analog input voltage span (the difference between the voltages applied between two multiplexer inputs or the voltage applied to one of the multiplexer inputs and analog ground), over which 4095 positive and 4096 negative codes exist. The voltage sources driving V_{REF+} or V_{REF-} must have very low output impedance and noise. The circuit in *Figure 12* is an example of a very stable reference appropriate for use with the LM12L454/8.

The ADC can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC's reference voltage. When this voltage is the system power supply, the V_{REF+} pin is connected to V_A^+ and V_{REF-} is connected to GND. This technique relaxes the system reference stability requirements because the analog input voltage and the ADC reference voltage move together. This maintains the same output code for given input conditions.

For absolute accuracy, where the analog input voltage varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage's magnitude will require an initial adjustment to null reference voltage induced full-scale errors.

5.2 INPUT RANGE

The LM12L454/8's fully differential ADC and reference voltage inputs generate a two's-complement output that is found by using the equation below.

$$\text{output code} = \frac{V_{IN+} - V_{IN-}}{V_{REF+} - V_{REF-}} (4096) - \tfrac{1}{2} \qquad \text{(12-bit)}$$

$$\text{output code} = \frac{V_{IN+} - V_{IN-}}{V_{REF+} - V_{REF-}} (256) - \tfrac{1}{2} \qquad \text{(8-bit)}$$

Round up to the next integer value between −4096 to 4095 for 12-bit resolution and between −256 to 255 for 8-bit resolution if the result of the above equation is not a whole number. As an example, V_{REF+} = 2.5V, V_{REF-} = 1V, V_{IN+} = 1.5V and V_{IN-} = GND. The 12-bit + sign output code is positive full-scale, or 0,1111,1111,1111. If V_{REF+} = 3.3V, V_{REF-} = 1V, V_{IN+} = 3V, and V_{IN-} = GND, the 12-bit + sign output code is 0,1100,0000,0000.

5.3 INPUT CURRENT

A charging current flows into or out of (depending on the input voltage polarity) the analog input pins, IN0–IN7 at the start of the analog input acquisition time (t_{ACQ}). This current's peak value will depend on the actual input voltage applied.

5.4 INPUT SOURCE RESISTANCE

For low impedance voltage sources (<80Ω for 6 MHz operation) the input charging current will decay, before the end of the S/H's acquisition time, to a value that will not introduce any conversion errors. For higher source impedances, the S/H's acquisition time can be increased. As an example, operating with a 6 MHz clock frequency and maximum acquisition time, the LM12L454/8's analog inputs can handle source impedance as high as 5.56 kΩ. Refer to Section 2.1, Instruction RAM "00", Bits 12–15 for further information.

5.5 INPUT BYPASS CAPACITANCE

External capacitors (0.01 μF–0.1 μF) can be connected between the analog input pins, IN0–IN7, and analog ground to filter any noise caused by inductive pickup associated with long input leads. It will not degrade the conversion accuracy.

5.6 NOISE

The leads to each of the analog multiplexer input pins should be kept as short as possible. This will minimize input noise and clock frequency coupling that can cause conversion errors. Input filtering can be used to reduce the effects of the noise sources.

5.7 POWER SUPPLIES

Noise spikes on the V_A^+ and V_D^+ supply lines can cause conversion errors; the comparator will respond to the noise. The ADC is especially sensitive to any power supply spikes that occur during the auto-zero or linearity correction. Low inductance tantalum capacitors of 10 μF or greater paralleled with 0.1 μF monolithic ceramic capacitors are recom-

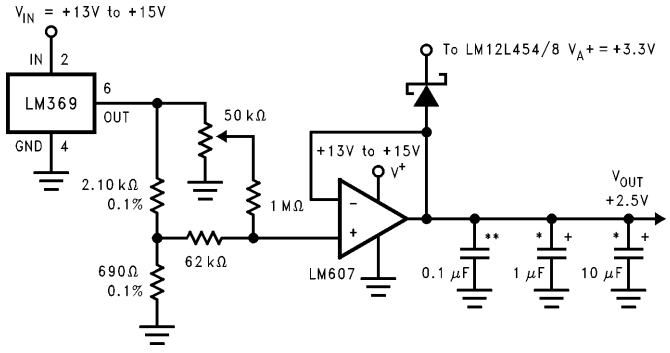


FIGURE 12. Low Drift Extremely Stable Reference Circuit

5.0 Analog Considerations (Continued)

mended for supply bypassing. Separate bypass capacitors should be used for the V_A+ and V_D+ supplies and placed as close as possible to these pins.

5.8 GROUNDING

The LM12L454/8's nominal high resolution performance can be maximized through proper grounding techniques. These include the use of separate analog and digital ground planes. The digital ground plane is placed under all components that handle digital signals, while the analog ground plane is placed under all analog signal handling circuitry. The digital and analog ground planes are connected at only one point, the power supply ground. This greatly reduces the occurrence of ground loops and noise.

It is recommended that stray capacitance between the analog inputs or outputs (LM12L454: IN0–IN3, MUXOUT+, MUXOUT−, S/H IN+, S/H IN−; LM12L458: IN0–IN7, $V_{REF}+$, and $V_{REF}-$) be reduced by increasing the clearance (+1/16th inch) between the analog signal and reference pins and the ground plane.

5.9 CLOCK SIGNAL LINE ISOLATION

The LM12L454/8's performance is optimized by routing the analog input/output and reference signal conductors (pins 34–44) as far as possible from the conductor that carries the clock signal to pin 23. Ground traces parallel to the clock signal trace can be used on printed circuit boards to reduce clock signal interference on the analog input/output pins.

6.0 Application Circuits

6.1 PC EVALUATION/INTERFACE BOARD

Figure 13 is the schematic of an evaluation/interface board designed to interface the LM12(H)454 or LM12(H)458 with an XT or AT style computer. The LM12(H)454/8 is the 5V version of the Data Acquisition System. It is functionally equivalent to the LM12L454/8. See the LM12(H)454/8 datasheet for further information. The board can be used to develop both software and hardware for applications using the LM12L454/8. The board hardwires the BW (Bus Width) pin to a logic high, selecting an 8-bit wide databus. Therefore, it is designed for an 8-bit expansion slot on the computer's motherboard.

The circuit operates on a single +5V supply derived from the computer's +12V supply using an LM340 regulator. This greatly attenuates noise that may be present on the computer's power supply lines. However, your application may only need an LC filter.

Figure 13 also shows the recommended supply (V_A+ and V_D+) and reference input ($V_{REF}+$ and $V_{REF}-$) bypassing. The digital and analog supply pins can be connected together to the same supply voltage. However, they need separate, multiple bypass capacitors. Multiple capacitors on the supply pins and the reference inputs ensures a low impedance bypass path over a wide frequency range.

All digital interface control signals (IOR, IOW, and AEN), data lines (DB0–DB7), address lines (A0–A9), and IRQ (interrupt request) lines (IRQ2, IRQ3, and IRQ5) connections are made through the motherboard slot connector. All analog signals applied to, or received by, the input multiplexer (IN0–IN7 for the LM12(H)458 and IN0–IN3, MUXOUT+, MUXOUT−, S/H IN+ and S/H IN− for the LM12(H)454), $V_{REF}+$, $V_{REF}-$, V_{REFOUT}, and the SYNC signal input/output are applied through a DB-37 connector on the rear side of the board. *Figure 13* shows that there are numerous analog ground connections available on the DB-37 connector.

The voltage applied to $V_{REF}-$ and $V_{REF}+$ is selected using two jumpers, JP1 and JP2. JP1 selects between the voltage applied to the DB-37's pin 24 or GND and applies it to the LM12(H)454/8's $V_{REF}-$ input. JP2 selects between the LM12(H)454/8's internal reference output, V_{REFOUT}, and the voltage applied to the DB-37's pin 22 and applies it to the LM12(H)454/8's $V_{REF}+$ input.

TABLE III. LM12(H)454/8 Evaluation/Interface Board SW DIP-8 Switch Settings for Available I/O Memory Locations

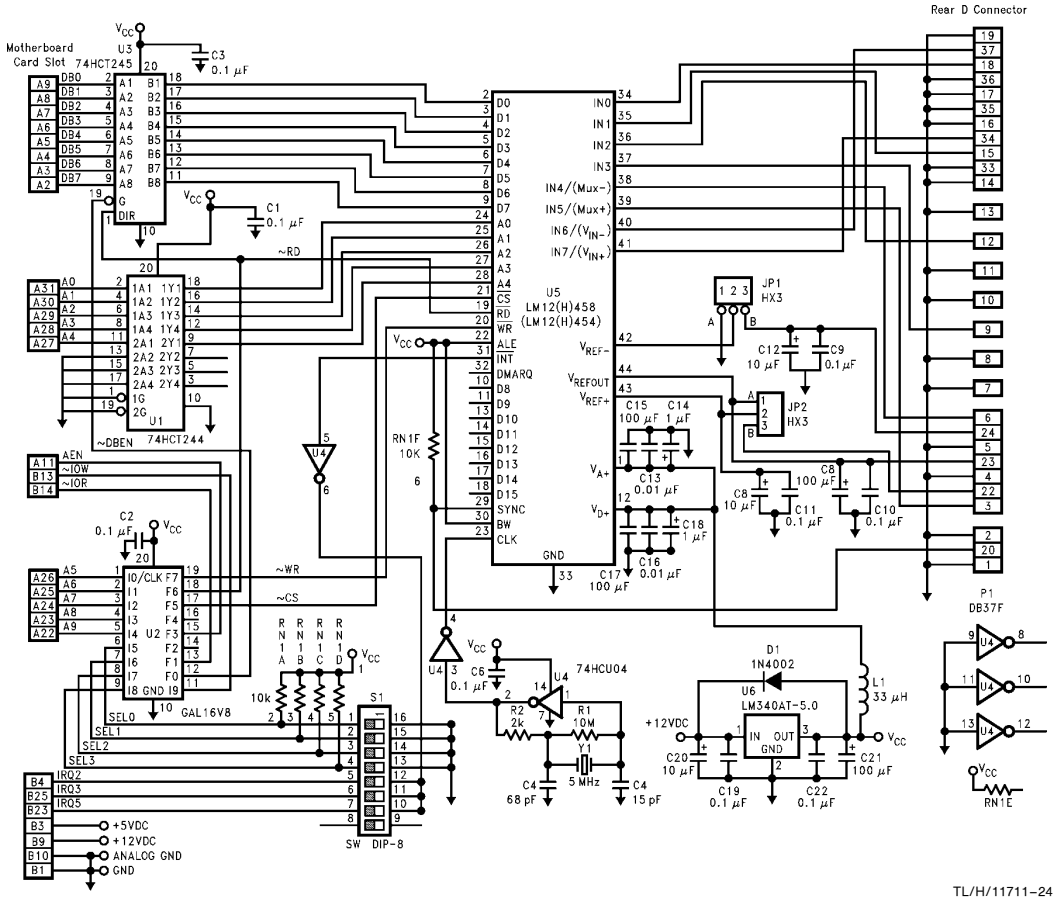
Hexidecimal I/O Memory Base Address	SW DIP-8			
	SW1 (SEL0)	SW2 (SEL1)	SW3 (SEL2)	SW4 (SEL3)
100	ON	ON	ON	ON
120	OFF	ON	ON	ON
140	ON	OFF	ON	ON
160	OFF	OFF	ON	ON
180	ON	ON	OFF	ON
1A0	OFF	ON	OFF	ON
1C0	ON	OFF	OFF	ON
300	OFF	OFF	OFF	ON
340	ON	ON	ON	OFF
280	OFF	ON	ON	OFF
2A0	ON	OFF	ON	OFF

The board allows the use of one of three Interrupt Request (IRQ) lines IRQ2, IRQ3, and IRQ5. The individual IRQ line can be selected using switches 5, 6, and 7 of SW DIP-8. When using any of these three IRQs, the user needs to ensure that there are no conflicts between the evaluation board and any other boards attached to the computer's motherboard.

Switches 1–4, along with address lines A5–A9 are used as inputs to GAL16V8 Programmable Gate Array (U2). This device forms the interface between the computer's control and address lines and generates the control signals used by the LM12(H)454/8 for $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$. It also generates the signal that controls the data buffers. Several address ranges within the computer's I/O memory map are available. Refer to Table III for the switch settings that gives the desired I/O memory address range. Selection of an address range must be done so that there are no conflicts between the evaluation board and any other boards attached to the computer's motherboard. The GAL equations are shown in *Figure 14*. The GAL functional block diagram is shown in *Figure 15*.

Figures 16–19 show the layout of each layer in the 3-layer evaluation/interface board plus the silk-screen layout showing parts placement. *Figure 17* is the top or component side, *Figure 18* is the middle or ground plane layer, *Figure 19* is the circuit side, and *Figure 16* is the parts layout.

6.0 Application Circuits (Continued)



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Note: The layout utilizes a split ground plane. The analog ground plane is placed under all analog signals and U5 pins 1, 34–44. The remaining signals and pins are placed over the digital ground. The single point ground connection is at U6, pin 2, and this is connected to the motherboard pin B1.

Parts List:

Y1	HC49U, 8 MHz crystal
D1	1N4002
L1	33 μH
P1	DB37F; parallel connector
R1	10 MΩ, 5%, ¼W
R2	2 kΩ, 5%, ¼W
RN1	10 kΩ, 6 resistor SIP, 5%, ⅛W
JP1, JP2	HX3, 3-pin jumper
S1	SW DIP-8; 8 SPST switches
C1–3, C6, C9–11, C19, C22	0.1 μF, 50V, monolithic ceramic
C4	68 pF, 50V, ceramic disk
C5	15 pF, 50V, ceramic disk
C7, C21	100 μF, 25V, electrolytic
C8, C12, C20	10 μF, 35V, electrolytic
C13, C16	0.01 μF, 50V, monolithic ceramic
C14, C18	1 μF, 35V, tantalum
C15, C17	100 μF, 50V, ceramic disk
U1	MM74HCT244N
U2	GAL16V8-20LNC
U3	MM74HCT245N
U4	MM74HCU04N
U5	LM12H458CIV or LM12H454CIV
U6	LM340AT-5.0
SK1	44-pin PLCC socket
A1	LM12H458/4 Rev. D PC Board

FIGURE 13. Schematic and Parts List for the LM12(H)454/8 Evaluation/Interface Board for XT and AT Style Computers, Order Number LM12458EVAL

6.0 Application Circuits (Continued)

```
;I/O Decode Lines
io_A5           1
io_A6           2
io_A7           3
io_A8           4
io_A9           5

;Select Lines for Zone Decode
SEL0            6
SEL1            7
SEL2            8
SEL3            9

;Physical I/O Controls
AEN                     15
!io_WR          11
!io_RD          13

;Physical Outputs
!CS                     17
!WR                     19
!RD                     18
!DBEN           12

;Intermediate Terms:
DEC0            16
FILT            14

Equations
;Decode of Select Lines:
SL0             =       !SEL2 & !SEL1 & !SEL0;
SL1             =       !SEL2 & !SEL1 &  SEL0;
SL2             =       !SEL2 &  SEL1 & !SEL0;
SL3             =       !SEL2 &  SEL1 &  SEL0;
SL4             =        SEL2 & !SEL1 & !SEL0;
SL5             =        SEL2 & !SEL1 &  SEL0;
SL6             =        SEL2 &  SEL1 & !SEL0;
SL7             =        SEL2 &  SEL1 &  SEL0;

;Decode of Address Lines:
AL00    =       SL0 & !io_A7 & !io_A6 & !io_A5;
AL20    =       SL1 & !io_A7 & !io_A6 &  io_A5;
AL40    =       SL2 & !io_A7 &  io_A6 & !io_A5;
AL60    =       SL3 & !io_A7 &  io_A6 &  io_A5;
AL80    =       SL4 &  io_A7 & !io_A6 & !io_A5;
ALA0    =       SL5 &  io_A7 & !io_A6 &  io_A5;
ALC0    =       SL6 &  io_A7 &  io_A6 & !io_A5;

AH01    =       !SEL3 & !io_A9 &  io_A8;
AH02    =        SEL3 &  io_A9 & !io_A8 &  io_A7 & !io_A6;
AH03    =        SEL3 &  io_A9 &  io_A8 & !io_A7 & !io_A5;

;Intermediate Address Groups:
DEC0    =       !AEN & (AL00 + AL20 + AL40 + AL60 + AL80 + ALA0 + ALC0);

;DAS Chip Select Decode:
FILT    =       CS & ( io_WR + io_RD);
CS              =       ( io_WR  + io_RD) & DEC0 & ( AH01 + AH02 + AH03);
DBEN    =       CS & DEC0 & ( io_WR + io_RD);

;Delayed Read/ Write Decodes:
WR              =       io_WR & FILT;
RD              =       io_RD & FILT;
```

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FIGURE 14. Logic Equations Used to Program the GAL16V8

6.0 Application Circuits (Continued)

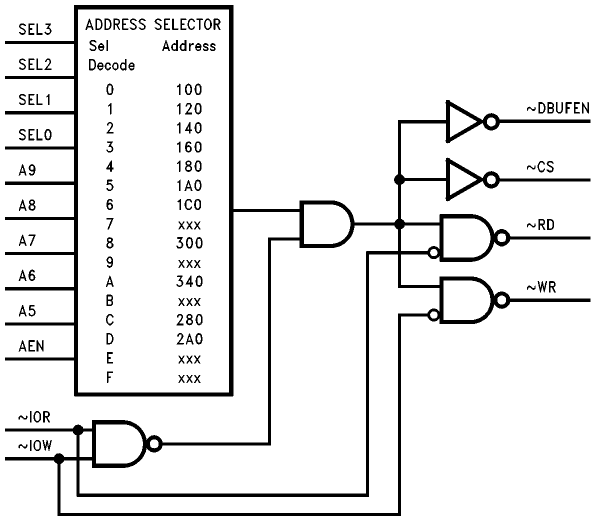

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FIGURE 15. GAL Functional Block Diagram

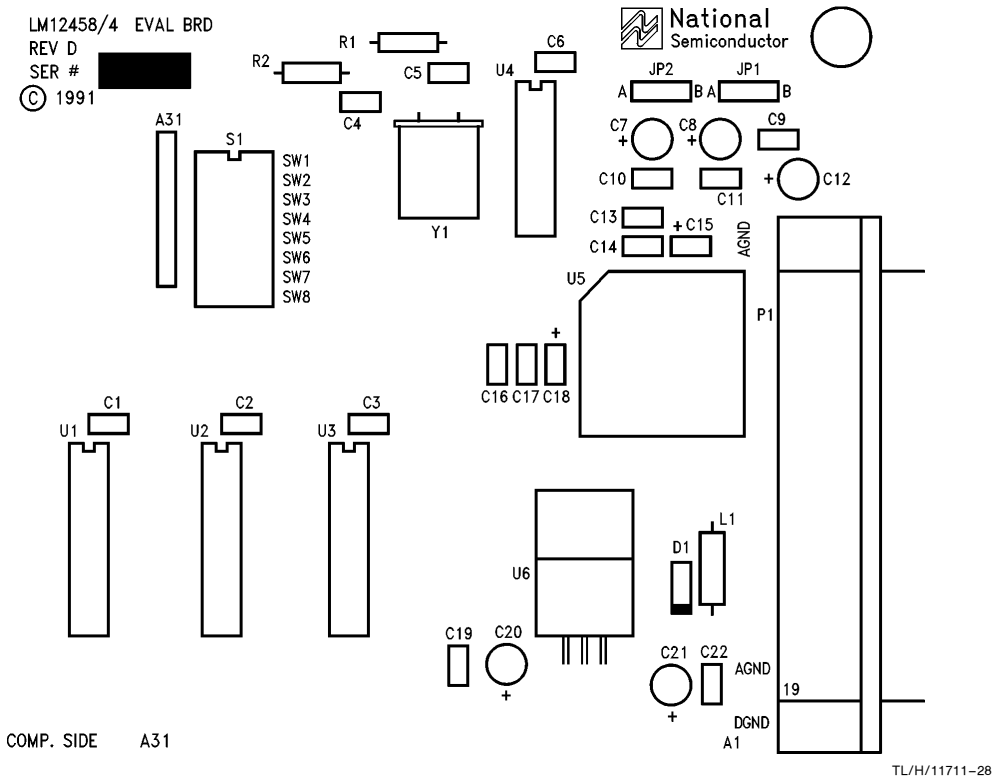

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FIGURE 16. Silk-Screen Layout Showing Parts Placement on the LM12(H)454/8 Evaluation/Interface Board

6.0 Application Circuits (Continued)

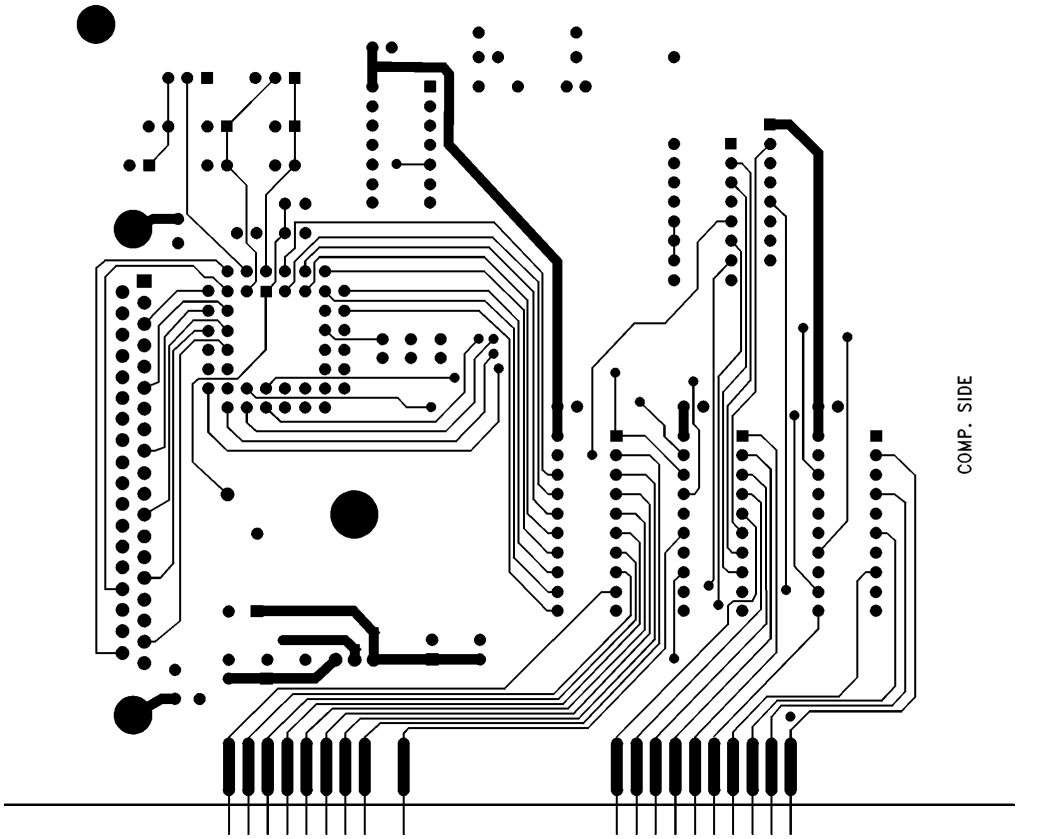

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FIGURE 17. LM12(H)454/8 Evaluation/Interface Board Component-Side Layout Positive

6.0 Application Circuits (Continued)

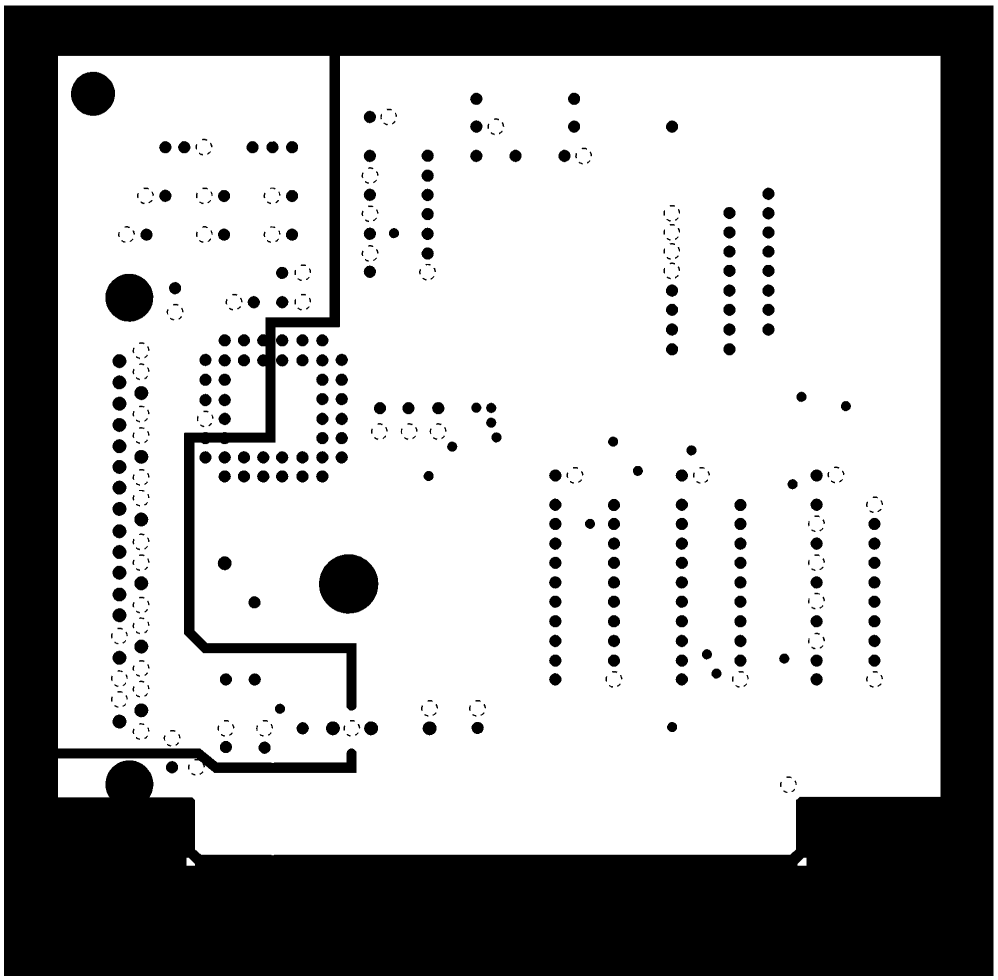

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FIGURE 18. LM12(H)454/8 Evaluation/Interface Board Ground-Plane Layout Negative

6.0 Application Circuits (Continued)

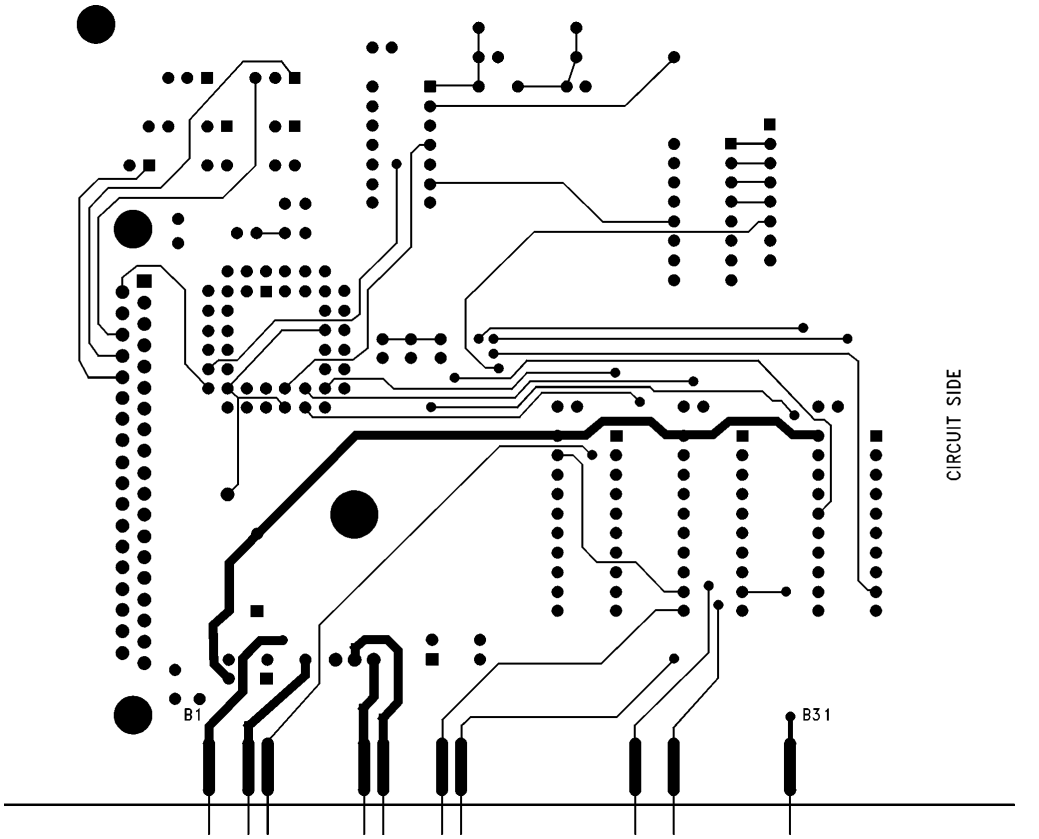

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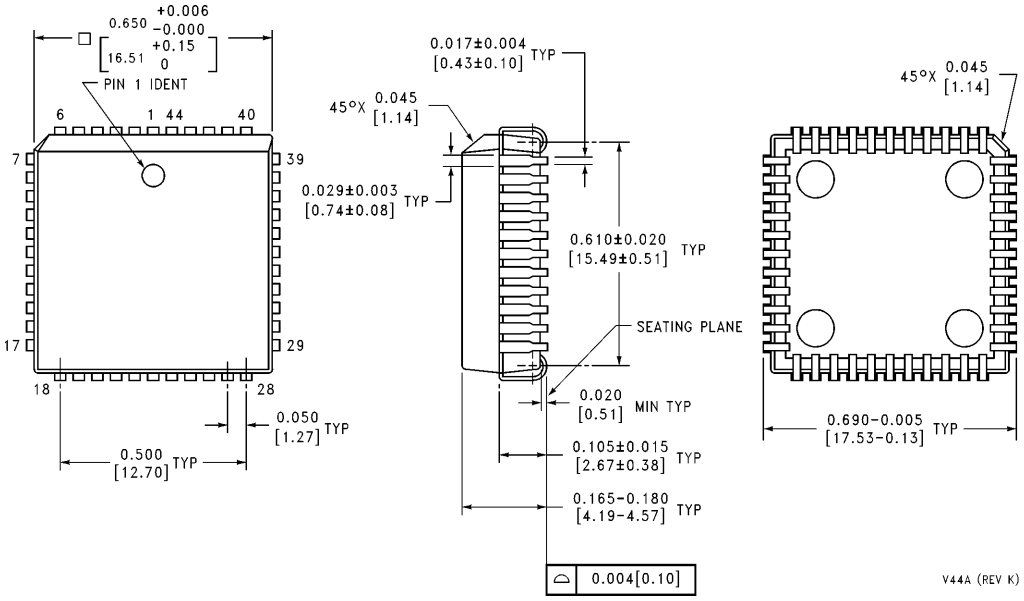
FIGURE 19. LM12(H)454/8 Evaluation/Interface Circuit-Side Layout Positive

Physical Dimensions inches (millimeters)



Order Number LM12L454CIV or LM12L458CIV
NS Package Number V44A

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