National Semiconductor

June 1998

DS90C402
Dual Low Voltage Differential Signaling (LVDS) Receiver

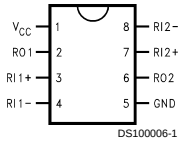
General Description

The DS90C402 is a dual receiver device optimized for high data rate and low power applications. This device along with the DS90C401 provides a pair chip solution for a dual high speed point-to-point interface. The device is in a PCB space saving 8 lead small outline package. The receiver offers ±100 mV threshold sensitivity, in addition to common-mode noise protection.

Features

- Ultra Low Power Dissipation
- Operates above 155.5 Mbps
- Standard TIA/EIA-644
- 8 Lead SOIC Package saves PCB space
- V_{CM} ±1V center around 1.2V
- ±100 mV Receiver Sensitivity

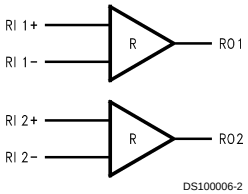
Connection Diagram



DS100006-1

Order Number DS90C402M
See NS Package Number M08A

Functional Diagram



DS100006-2

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
Input Voltage (R_{IN+}, R_{IN-})	−0.3V to (V_{CC} + 0.3V)
Output Voltage (R_{OUT})	−0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation @ +25˚C	
M Package	1025 mW
Derate M Package	8.2 mW/˚C above +25˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature Range Soldering (4 sec.)	+260˚C
Maximum Junction Temperature	+150˚C
ESD Rating (Note 4)	
(HBM, 1.5 kΩ, 100 pF)	≥ 3,500V
(EIAJ, 0 Ω, 200 pF)	≥ 250V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Receiver Input Voltage	GND		2.4	V
Operating Free Air Temperature (T_A)	−40	+25	+85	˚C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} = + 1.2V		R_{IN+}, R_{IN-}			+100	mV
V_{TL}	Differential Input Low Threshold				−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V		−10	±1	+10	µA
		V_{IN} = 0V			−10	± 1	+10	µA
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		R_{OUT}	3.8	4.9		V
		I_{OH} = −0.4mA, Inputs terminated			3.8	4.9		V
		I_{OH} = −0.4mA, Inputs Open			3.8	4.9		V
		I_{OH} = −0.4mA, Inputs Shorted				4.9		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				0.07	0.3	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 8)			−15	−60	−100	mA
I_{CC}	No Load Supply Current	Inputs Open		V_{CC}		3.5	10	mA

Switching Characteristics

V_{CC} = +5.0V ± 10%, T_A = −40˚C to +85˚C (Notes 3, 4, 5, 6, 9)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 5 pF, V_{ID} = 200 mV (*Figure 1* and *Figure 2*)	1.0	3.40	6.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	3.48	6.0	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$		0	0.08	1.2	ns
t_{SK1}	Channel-to-Channel Skew (Note 5)		0	0.6	1.5	ns
t_{SK2}	Chip to Chip Skew (Note 6)				5.0	ns
t_{TLH}	Rise Time			0.5	2.5	ns
t_{THL}	Fall Time			0.5	2.5	ns

Parameter Measurement Information

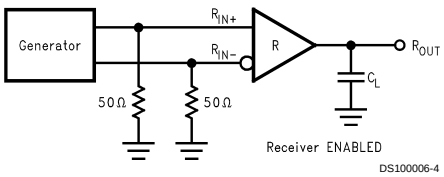


FIGURE 1. Receiver Propagation Delay and Transition Time Test Circuit

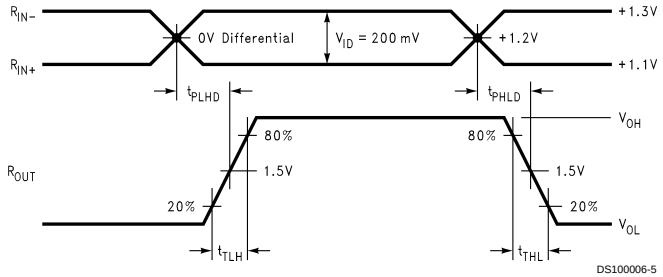


FIGURE 2. Receiver Propagation Delay and Transition Time Waveforms

Typical Application

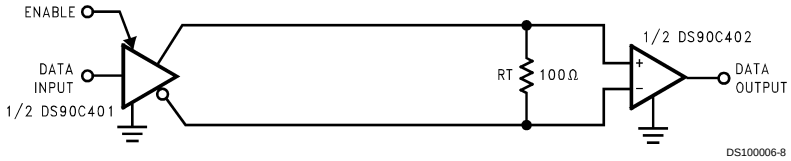


FIGURE 3. Point-to-Point Application

Applications Information

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 3*. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90C402 differential line receiver is capable of detecting signals as low as 100 mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. Both receiver input pins should honor their specified operating input voltage range of 0V to +2.4V (measured from each pin to ground), exceeding these limits may turn on the ESD protection circuitry which will clamp the bus voltages.

Fail-Safe Feature:

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DS90C402 is a dual receiver device, and if an application requires only one receiver, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

Applications Information (Continued)

2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

Pin Descriptions

Pin No.	Name	Description
2, 6	R_{OUT}	Receiver output pin
3, 7	$R_{IN}+$	Positive receiver input pin
4, 8	$R_{IN}-$	Negative receiver input pin
5	GND	Ground pin
1	V_{CC}	Positive power supply pin, +5V ± 10%

Ordering Information

Operating Temperature	Package Type/ Number	Order Number
−40˚C to +85˚C	SOP/M08A	DS90C402M

RECEIVE MODE

$R_{IN+} - R_{IN-}$	R_{OUT}
> +100 mV	H
< −100 mV	L
100 mV > & > −100 mV	X

H = Logic High Level
L = Logic Low level
X = Indeterminant State

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: All typicals are given for: V_{CC} = +5.0V, T_A = +25˚C.

Note 4: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r and t_f (0%–100%) ≤ 1 ns for R_{IN}.

Note 5: Channel-to-Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with an event on the inputs.

Note 6: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

Note 7: ESD Rating:

HBM (1.5 kΩ, 100 pF) ≥ 3,500V

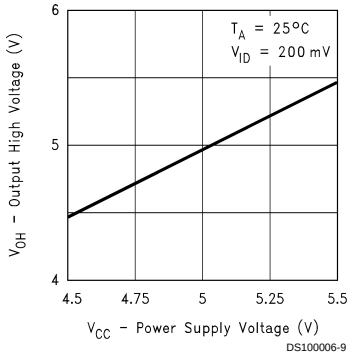
EIAJ (0Ω, 200 pF) ≥ 250V

Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Note 9: C_L includes probe and jig capacitance.

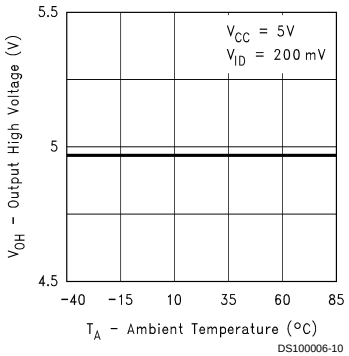
Typical Performance Characteristics

Output High Voltage vs Power Supply Voltage



DS100006-9

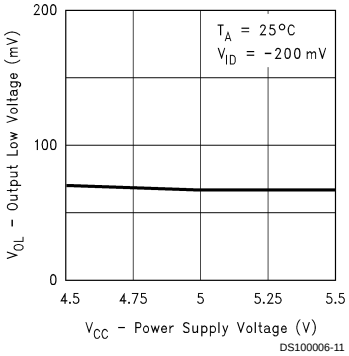
Output High Voltage vs Ambient Temperature



DS100006-10

Typical Performance Characteristics (Continued)

Output Low Voltage vs Power Supply Voltage



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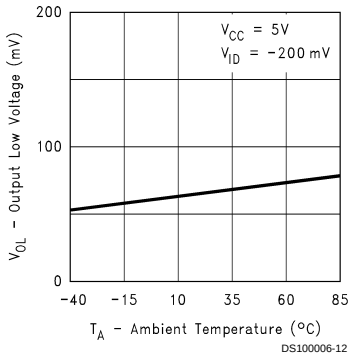
Output Low Voltage vs Ambient Temperature



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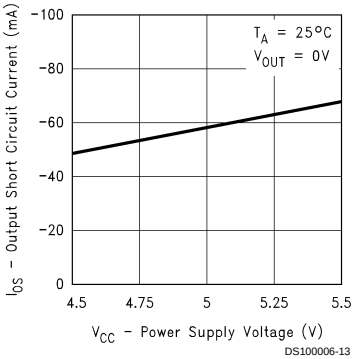
Output Short Circuit Current vs Power Supply Voltage



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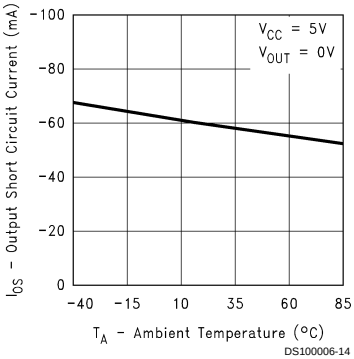
Output Short Circuit Current vs Ambient Temperature



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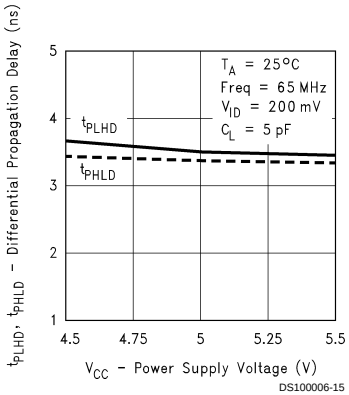
Differential Propagation Delay vs Power Supply Voltage



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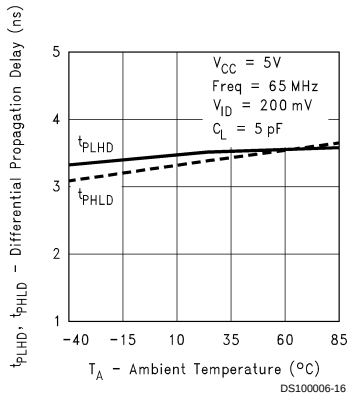
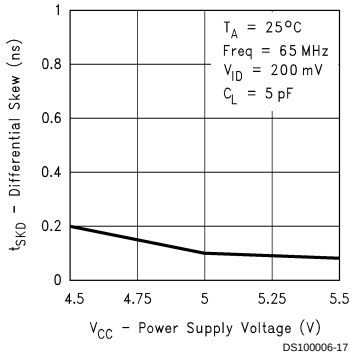
Differential Propagation Delay vs Ambient Temperature



DS100006-16

Typical Performance Characteristics (Continued)

Differential Skew vs Power Supply Voltage



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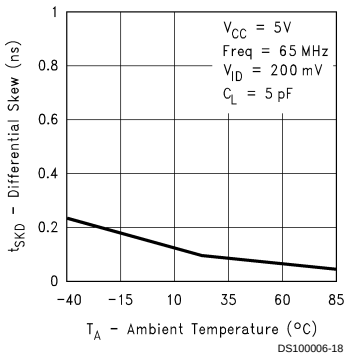
Differential Skew vs Ambient Temperature



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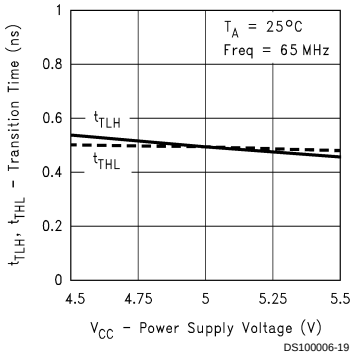
Transition Time vs Power Supply Voltage



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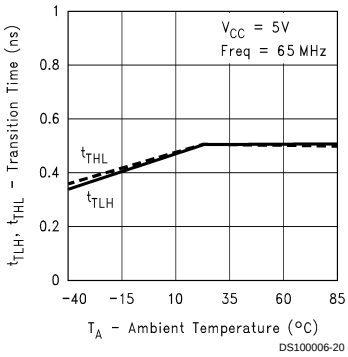
Transition Time vs Ambient Temperature



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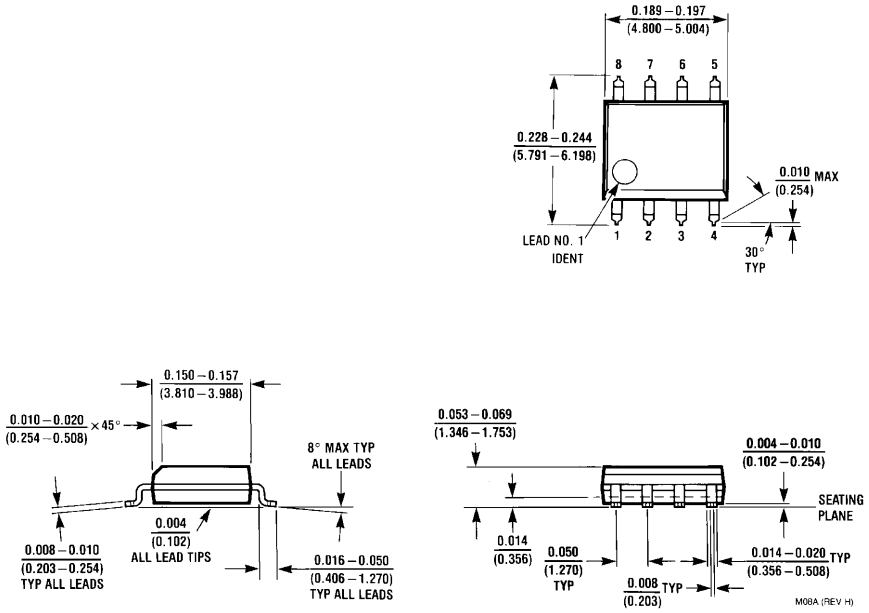
Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number DS90C402M
NS Package Number M08A

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