National Semiconductor

PRELIMINARY
August 1998

DS90C387/DS90CF388
+3.3V LVDS 24-Bit Dual Pixel Flat Panel Display (FPD) Link—SVGA to UXGA

General Description

The DS90C387/DS90CF388 transmitter/receiver pair is designed to support dual pixel data transmission between Host and Flat Panel Display up to UXGA resolutions. The transmitter converts 48 bits of CMOS/TTL data into 8 LVDS (Low Voltage Differential Signalling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a ninth LVDS link. Every cycle of the transmit clock 48 bits of RGB input data are sampled and transmitted. The receiver converts the LVDS data streams back into 48 bits of CMOS/TTL data. Control bits (FPLINE, FPFRAME and DRDY) are transmitted over 3 LVDS lines during the blanking interval. At a transmit clock frequency of 112 MHz, 48 bits of RGB data are transmitted at an effective rate of 672 Mbps per LVDS data channel. Using a 112 MHz clock, the data throughput is 672 Megabytes (5.38 Gbits) per second. The transmitter may also provide a single pixel interface to the graphic controller, accepting clock speeds up to 170MHz. Data is split into 'even' and 'odd' pixels for transmission across the LVDS interface and at the receiver outputs.

The transmitter is designed to reject cycle-to-cycle jitter which may be seen at the transmitter input clock. Very low cycle-to-cycle jitter is passed on to the transmitter outputs. This significantly reduces the impact of jitter provided by the input clock source, and improves the accuracy of data sampling. Data sampling is further enhanced by automatically calibrated data sampling strobes at the receiver inputs. Timing and control signals are sent during blanking intervals to guarantee correct reception of these critical signals.

The DS90C387/8 chipset is designed to support both notebook and monitor applications. The cable deskew circuitry, pre-emphasis and encoded dc balance support the requirements of a longer cable interface at high speeds.

The transmitter is offered with programmable edge data strobes for convenient interface with a variety of graphics controllers. The transmitter can be programmed for rising edge strobe or falling edge strobe through a dedicated pin. A rising edge transmitter will inter-operate with a falling edge receiver without any translation logic.

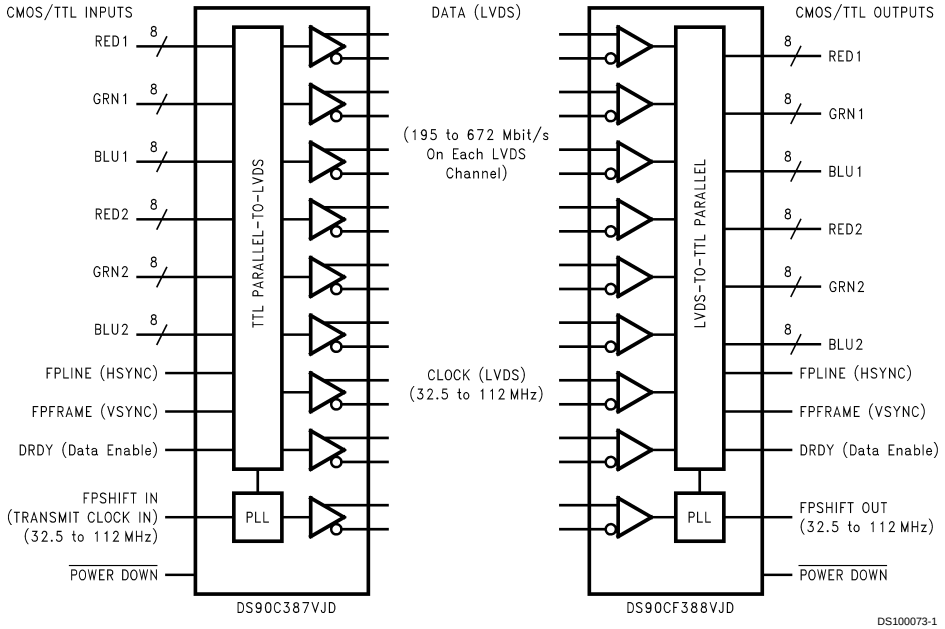
The chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

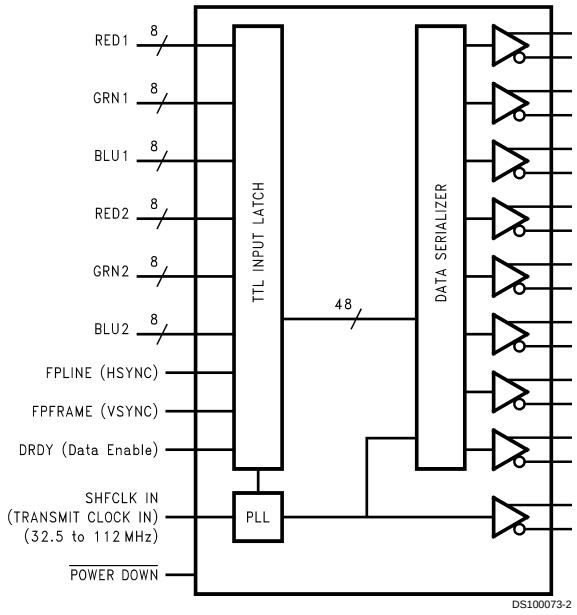
- 32.5 MHz to 112 MHz input clock supports single pixel XGA and SXGA, dual pixel UXGA
- Dual pixel architecture supports interface to GUI and timing controller; optional single pixel transmitter inputs support single pixel GUI interface
- Automatically calibrated receiver sampling strobes
- Timing and control signals transmitted during blanking interval for improved reliability
- EMI reduction circuitry
- Pre-emphasis, deskew and dc balance coding support longer cable drive (5 meters) for monitor applications
- Flow-through pinout
- 50% receiver output clock duty cycle for lower EMI and easy timing controller interface
- "Stopped RxCLKOUT" indicator pin
- Transmitter rejects cycle-to-cycle jitter
- Programmable transmitter data and control strobe select (Rising or Falling edge strobe)
- Backward compatible configuration select
- Transmitter provides optional second LVDS clock for backward compatibility
- Support for two additional user defined control signals
- Single +3.3V supply
- Up to 5.38 Gbits/sec bandwidth
- LVDS signaling reduces cable size
- Compatible with TIA/EIA-644 LVDS standard
- Designed on a non-proprietary CMOS process for easy integration

DS90C387/DS90CF388 +3.3V LVDS 24-Bit Dual Pixel Flat Panel Display (FPD) Link—SVGA to UXGA

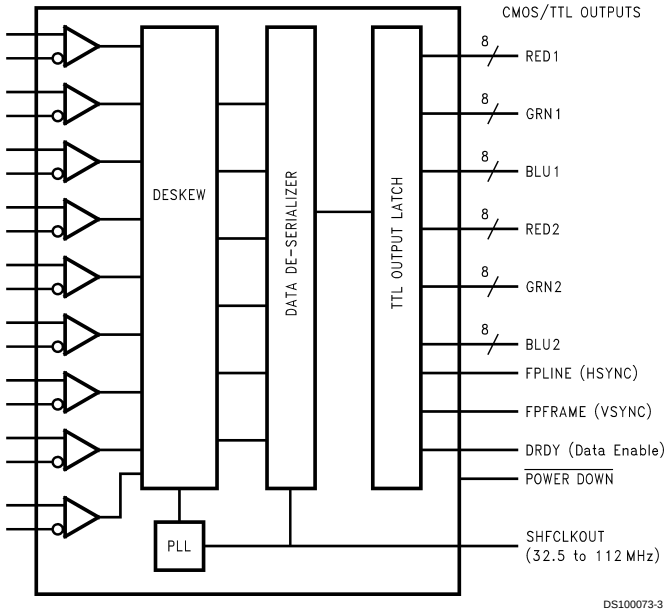
Generalized Block Diagram



Transmitter Block Diagram

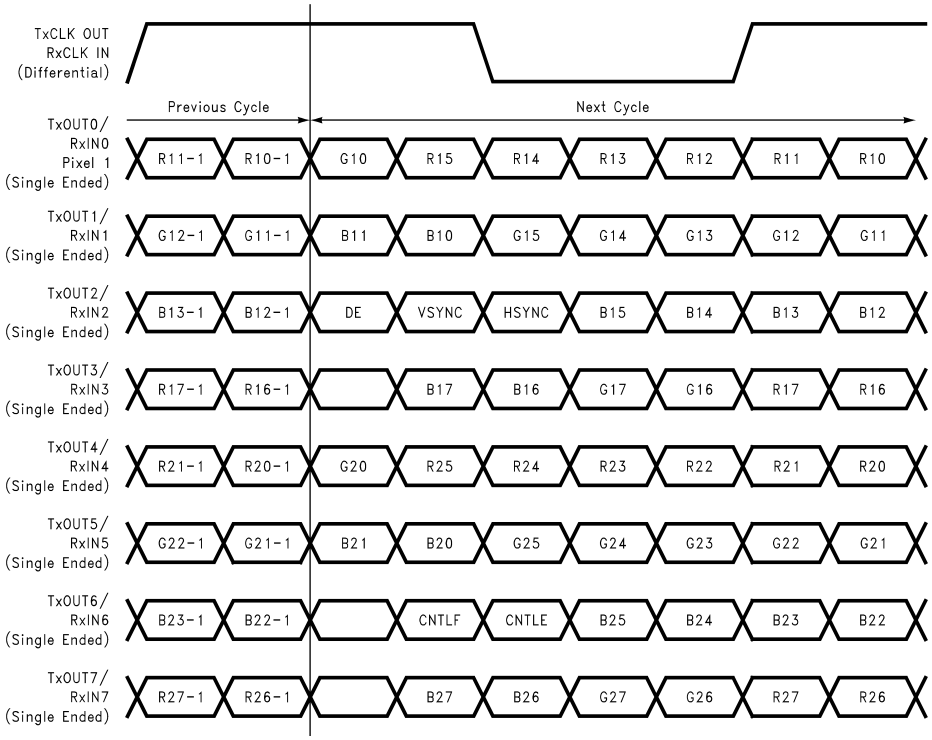


Receiver Block Diagram



LVDS Interface

TTL Data Inputs Mapped to LVDS Outputs
Non-DC Balanced Mode (Backward Compatible)



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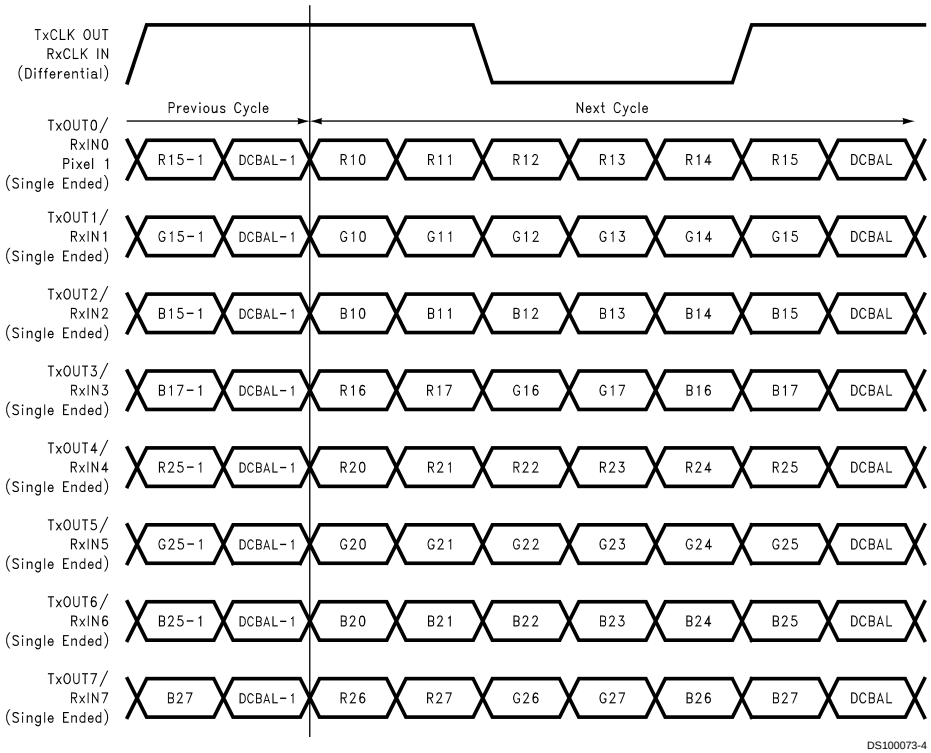
LVDS Interface (Continued)

48 Parallel TTL Data Inputs Mapped to LVDS Outputs
DC Balanced Mode - Data Enabled



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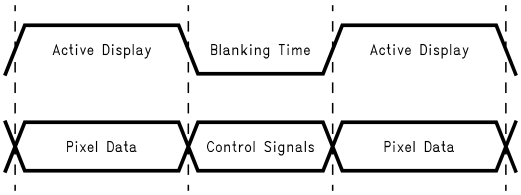
LVDS Interface (Continued)

Control Signals Transmitted During Blanking



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Control Signals Transmitted During Blanking

Control Signal	Signal Level	Channel	Pattern
DE	HIGH	TxCLKOUT	1111000 or 1110000
	LOW		1111100 or 1100000
HSYNC	HIGH	TXOUT0	1100000 or 1111100
	LOW		1110000 or 1111000
VSYNC	HIGH	TXOUT1	1100000 or 1111100
	LOW		1110000 or 1111000
CNTLF	HIGH	TXOUT4	1100000 or 1111100
	LOW		1110000 or 1111000
CNTLE	HIGH	TXOUT5	1100000 or 1111100
	LOW		1110000 or 1111000

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec.)	+260˚C
Maximum Package Power Dissipation Capacity @ 25˚C	
100 TQFP Package:	
DS90C387	TBD
DS90CF388	TBD
Package Derating:	
DS90C387	TBD mW/˚C above +25˚C
DS90CF388	TBD mW/˚C above +25˚C

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	˚C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{p-p}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		TBD	TBD		V
		I_{OH} = −2mA		TBD	TBD		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}			+1.8	+10	µA
		V_{IN} = GND		−10	0		µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	345	450	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States					35	mV
V_{os}	Offset Voltage			1.125	1.25	1.375	V
ΔV_{os}	Change in V_{os} between Complimentary Output States					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−3.5	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Powerdown}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V				±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V				±10	µA
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern (*Figures 1, 3*)	f = 32.5 MHz		TBD	TBD	mA
			f = 65 MHz		TBD	TBD	mA
			f = 112 MHz		TBD	TBD	mA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
ICCTG	Transmitter Supply Current 16 Grayscale	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern (*Figures 2, 3*)	f = 32.5 MHz		TBD	TBD	mA
			f = 65 MHz		TBD	TBD	mA
			f = 112 MHz		TBD	TBD	mA
ICCTZ	Transmitter Supply Current Power Down	$\overline{\text{Powerdown}}$ = Low Driver Outputs in TRI-STATE under Powerdown Mode			TBD	150	µA
RECEIVER SUPPLY CURRENT							
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern (*Figures 1, 4*)	f = 32.5 MHz		TBD	TBD	mA
			f = 65 MHz		TBD	TBD	mA
			f = 112 MHz		TBD	TBD	mA
ICCRG	Receiver Support Current 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern (*Figures 2, 4*)	f = 32.5 MHz		TBD	TBD	mA
			f = 65 MHz		TBD	TBD	mA
			f = 112 MHz		TBD	TBD	mA
ICCRZ	Receiver Supply Current Power Down	$\overline{\text{Powerdown}}$ = Low Receiver Outputs stay low during Power down mode.			TBD	150	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25˚C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
TCIT	TxCLK IN Transition Time (*Figure 5*)			TBD	ns
TCIP	TxCLK IN Period (*Figure 6*)	8.928	T	30.77	ns
TCIH	TxCLK in High Time (*Figure 6*)	0.35T	0.5T	0.65T	ns
TCIL	TxCLK in Low Time (*Figure 6*)	0.35T	0.5T	0.65T	ns

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time (*Figure 3*)				TBD	ns
LHLT	LVDS High-to-Low Transition Time (*Figure 3*)				TBD	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 (*Figure 14*) (Note 4)	f = 112 MHz	-200	0	+200	ps
TPPos1	Transmitter Output Pulse Position for Bit 1		1.076	1.276	1.476	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		2.351	2.551	2.751	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		3.626	3.826	4.026	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		4.902	5.102	5.302	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		6.178	6.378	6.578	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		7.453	7.653	7.853	ns
TSTC	TxIN Setup to TxCLK IN (*Figure 6*)		3.5			ns
THTC	TxIN Hold to TxCLK IN (*Figure 6*)		0.5	0		ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25˚C, V_{CC} = 3.3V (*Figure 8*)		TBD	3.7	TBD	ns
	TxCLK IN to TxCLK OUT Delay (*Figure 8*)		TBD	3.7	TBD	ns
TJCC	Transmitter Jitter Cycle-to-cycle (Figure TBD)	f = 112 MHz		TBD	TBD	ps
		f = 65 MHz		TBD	TBD	ps
		f = 32.5 MHz		TBD	TBD	ps
TPLLS	Transmitter Phase Lock Loop Set (*Figure 10*)				10	ms
TPDD	Transmitter Powerdown Delay (*Figure 12*)				100	ns

Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time (*Figure 4*)				TBD	ns
CHLT	CMOS/TTL High-to-Low Transition Time (*Figure 4*)				TBD	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (*Figure 15*) (Note 4)	f = 112 MHz	338	638	938	ps
RSPos1	Receiver Input Strobe Position for Bit 1		1.613	1.913	2.213	ns
RSPos2	Receiver Input Strobe Position for Bit 2		2.889	3.189	3.489	ns
RSPos3	Receiver Input Strobe Position for Bit 3		4.164	4.464	4.764	ns
RSPos4	Receiver Input Strobe Position for Bit 4		5.440	5.740	6.040	ns
RSPos5	Receiver Input Strobe Position for Bit 5		6.715	7.015	7.315	ns
RSPos6	Receiver Input Strobe Position for Bit 6		7.991	8.291	8.591	ns
RCOP	RxCLK OUT Period (*Figure 7*)		8.928	T	30.77	ns
RCOH	RxCLK OUT High Time (*Figure 7*)	f = 112 MHz	TBD			ns
RCOL	RxCLK OUT Low Time (*Figure 7*)	f = 112 MHz	TBD			ns
RSRC	RxOUT Setup to RxCLK OUT (*Figure 7*)	f = 112 MHz	TBD			ns
RHRC	RxOUT Hold to RxCLK OUT (*Figure 7*)	f = 112 MHz	TBD			ns
RCCD	RxCLK IN to RxCLK Out Delay @ 25˚C, V_{CC} = 3.3V (*Figure 9*)		TBD		TBD	ns
RPLLS	Receiver Phase Lock Loop Set (*Figure 11*)				10	ms
RPDD	Receiver Powerdown Delay (*Figure 13*)				1	µs
RSKM	Receiver Skew Margin without Deskew (*Figure 16*) (Note 5)	f = 112 MHz	TBD			ps
	Receiver Skew Margin with Deskew (*Figure 16*) (Note 6)		TBD			ps

Note 4: The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionally tested only on Automatic Test Equipment (ATE).

Note 5: Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account transmitter output pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window RSPOS). This margin allows for LVDS interconnect skew, intersymbol interference (both dependent on type/length of cable) and clock jitter.

RSKM ≥ cable skew (type, length) + source clock jitter (cycle to cycle).

Note 6: This limit is based on the capability of deskew circuitry. This margin allows for LVDS interconnect skew, intersymbol interference (both dependent on type/length of cable) and clock jitter.

AC Timing Diagrams

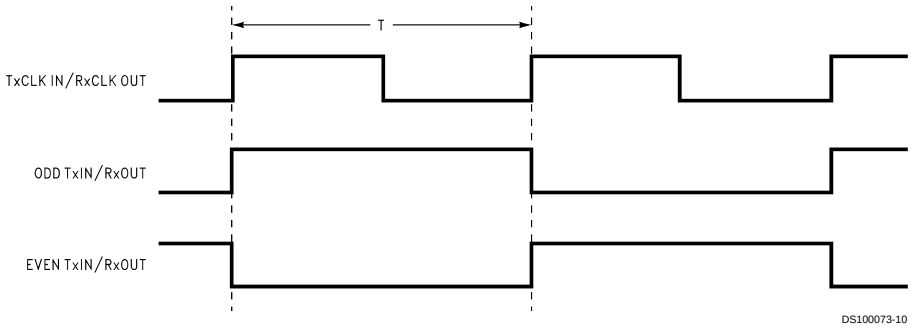


FIGURE 1. "Worst Case" Test Pattern

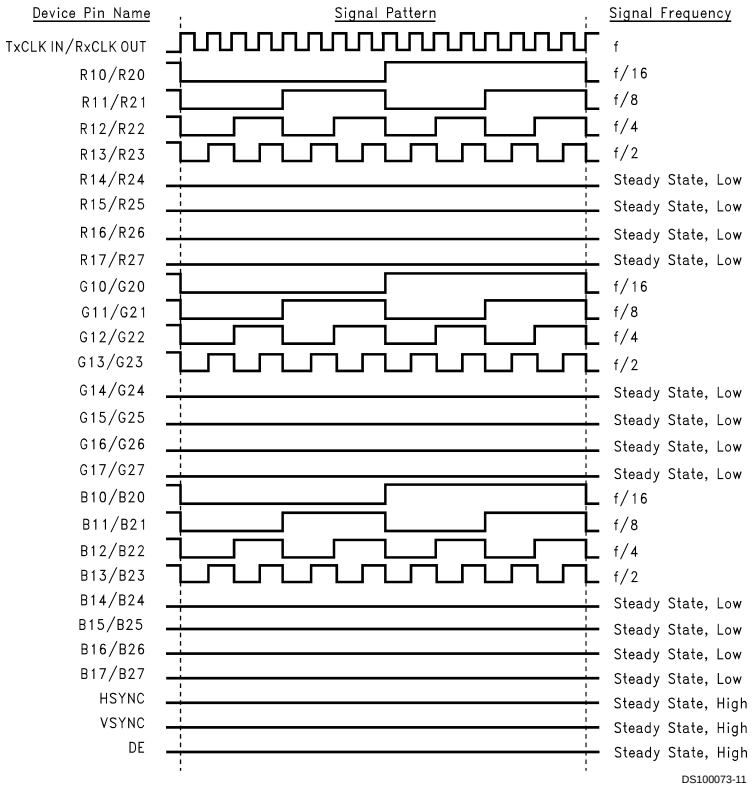


FIGURE 2. "16 Grayscale" Test Pattern (Notes 7, 8, 9)

Note 7: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 8: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 9: *Figures 1, 2* show a falling edge data strobe (TxCLK IN/RxCLK OUT).

AC Timing Diagrams (Continued)

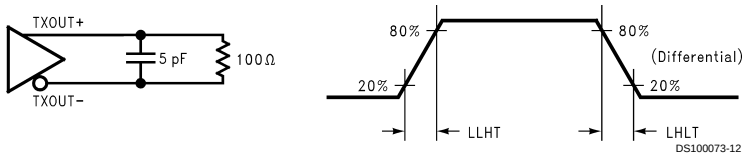


FIGURE 3. DS90C387 (Transmitter) LVDS Output Load and Transition Times

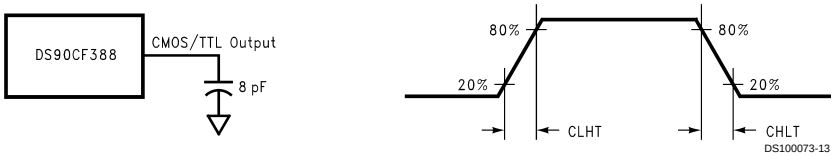


FIGURE 4. DS90CF388 (Receiver) CMOS/TTL Output Load and Transition Times

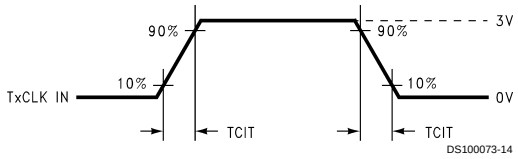


FIGURE 5. DS90C387 (Transmitter) Input Clock Transition Time

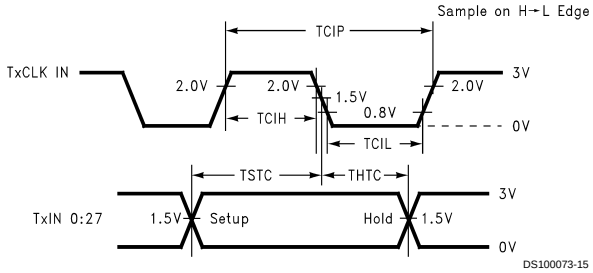


FIGURE 6. DS90C387 (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)

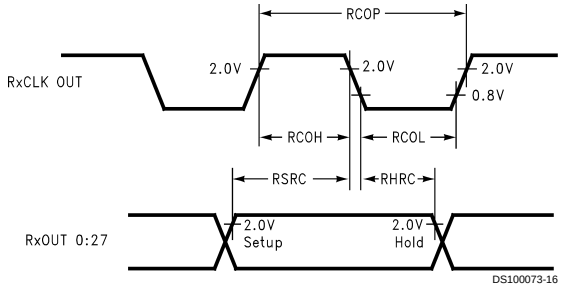


FIGURE 7. DS90CF388 (Receiver) Setup/Hold and High/Low Times

AC Timing Diagrams (Continued)

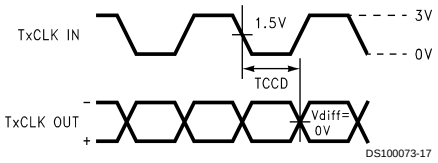


FIGURE 8. DS90C387 (Transmitter) Clock in to Clock Out Delay (Falling Edge Strobe)

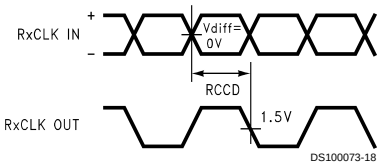


FIGURE 9. DS90CF388 (Receiver) Clock in to Clock Out Delay

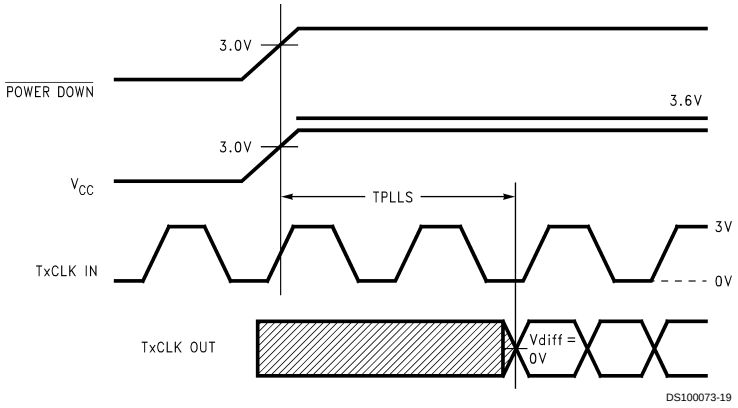


FIGURE 10. DS90C387 (Transmitter) Phase Lock Loop Set Time

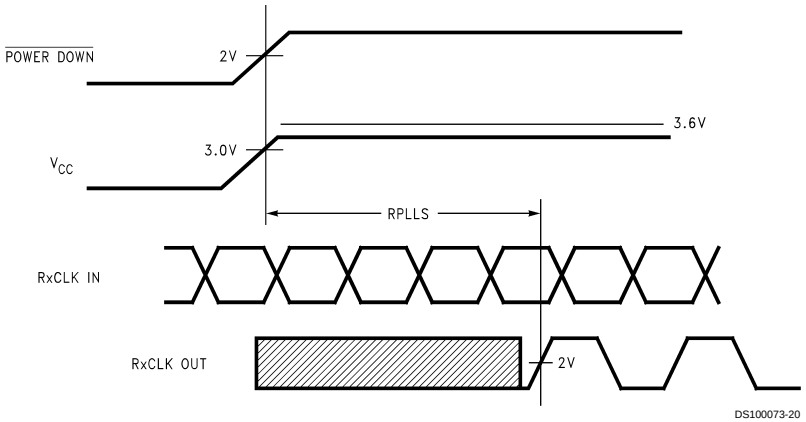


FIGURE 11. DS90CF388 (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

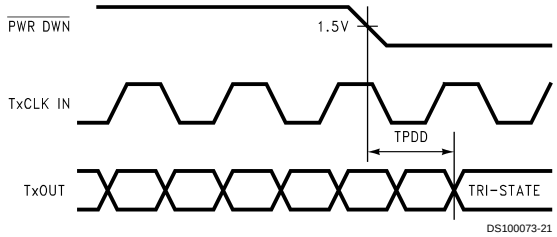


FIGURE 12. Transmitter Power Down Delay

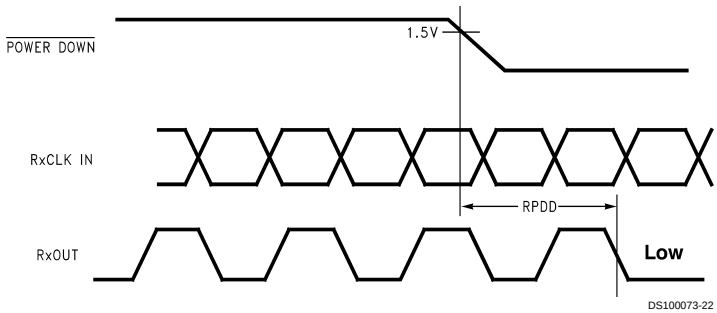


FIGURE 13. Receiver Power Down Delay

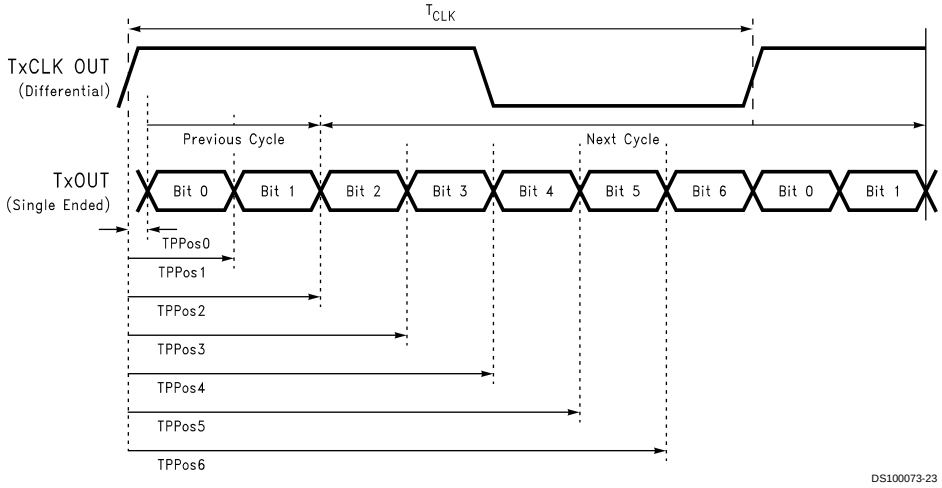


FIGURE 14. Transmitter LVDS Output Pulse Position Measurement

AC Timing Diagrams (Continued)

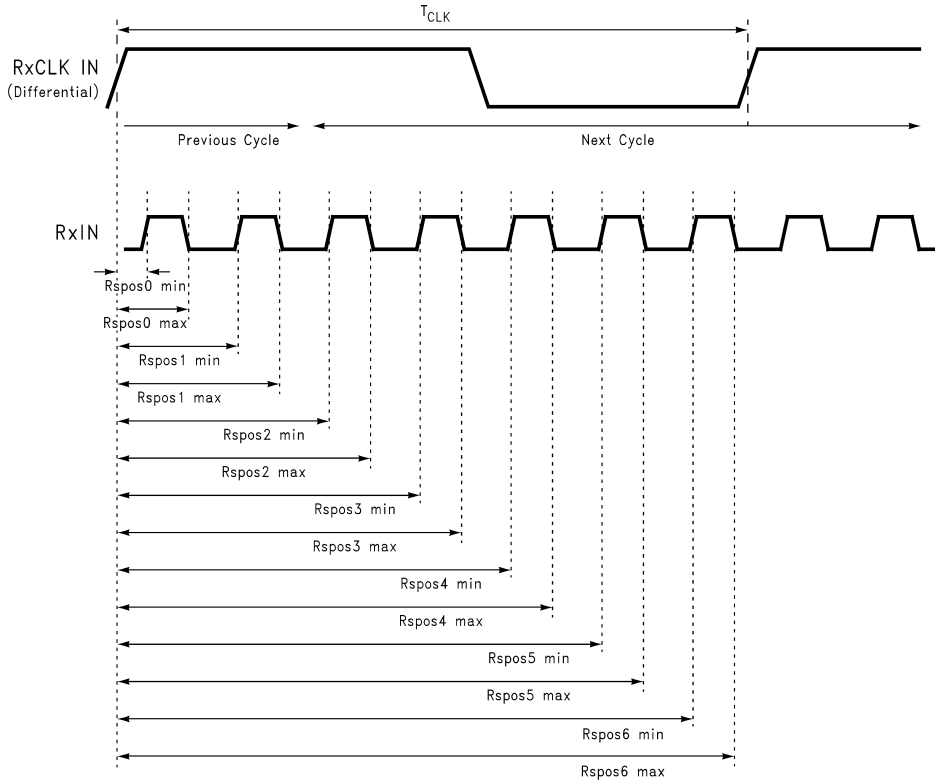
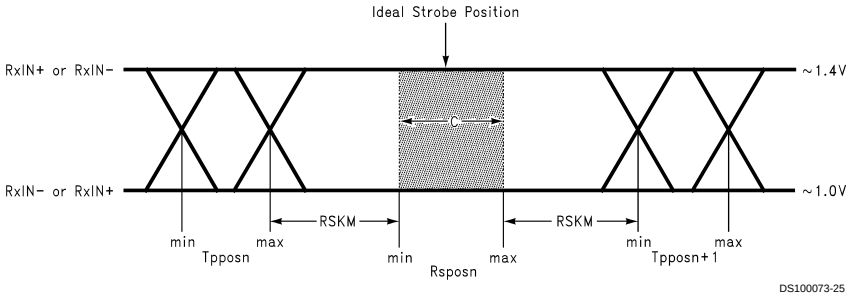


FIGURE 15. Receiver LVDS Input Strobe Position



C — Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max
Tppos — Transmitter output pulse position (min and max)
RSKM = Cable Skew (type, length) + Source Clock Jitter (cycle to cycle) (Note 10) + ISI (Inter-symbol interference) (Note 11)
Cable Skew — typically 10 ps–40 ps per foot, media dependent

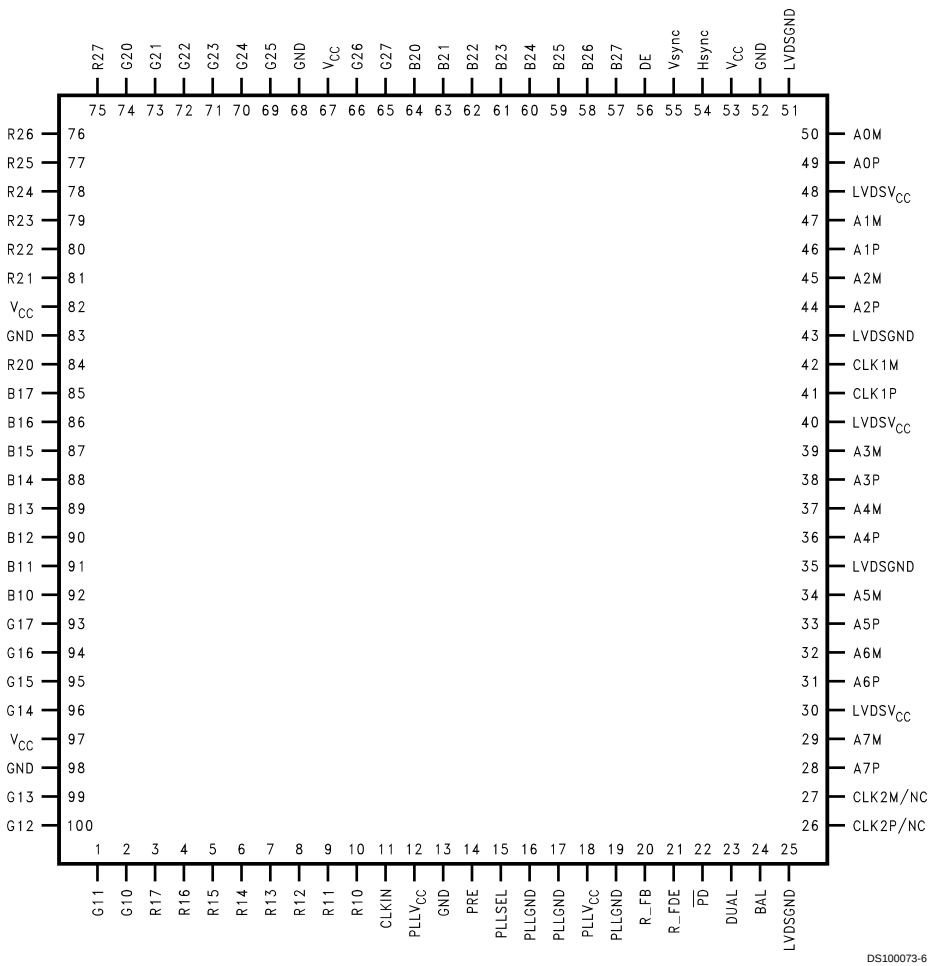
Note 10: Cycle-to-cycle jitter is less than xxx ps at 112 MHz

Note 11: ISI is dependent on interconnect length; may be zero

FIGURE 16. Receiver Skew Margin

Pin Diagram

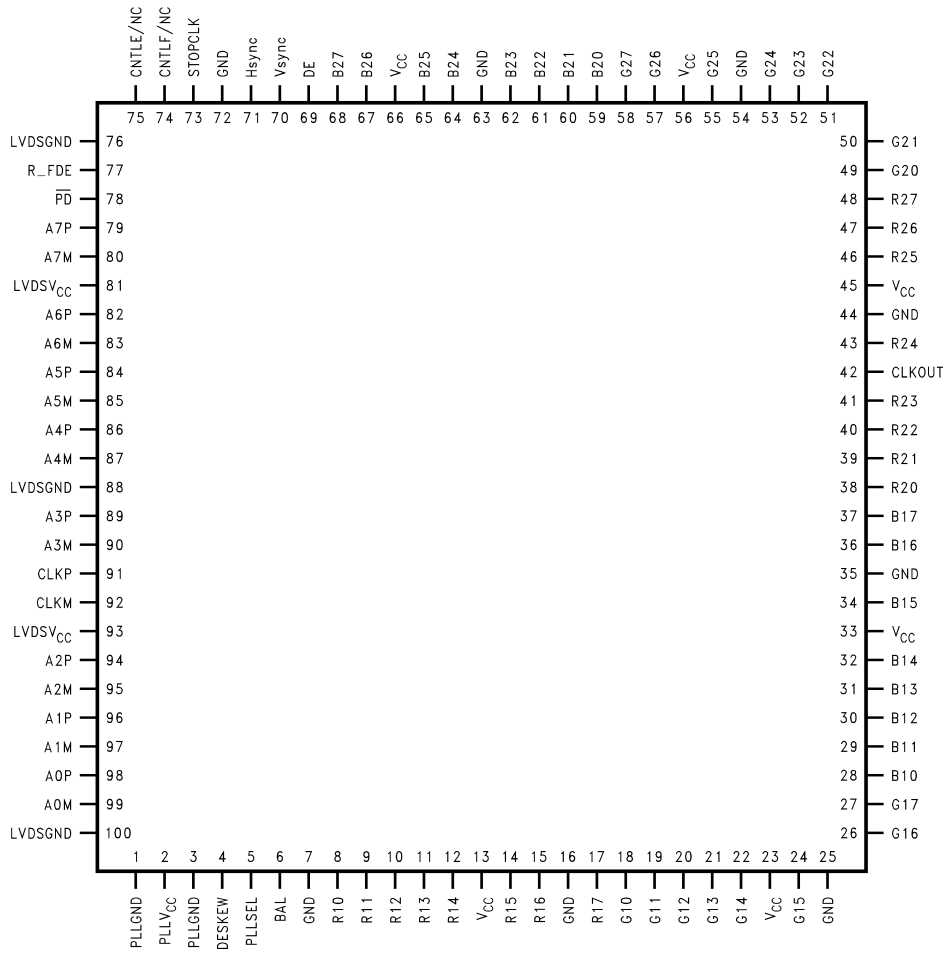
Transmitter



DS100073-6

Pin Diagram

Receiver



DS100073-7

TRUTH TABLE

TABLE 1. Programmable Transmitter / Receiver

Pin	Condition	Strobe Status
R_FB (Tx only)	R_FB = V_{CC}	Rising Edge Strobe
R_FB (Tx only)	R_FB = GND	Falling Edge Strobe
R_FDE	R_FDE = V_{CC}	Active data DE = High
R_FDE	R_FDE = GND	Active data DE = Low

DS90C387 Pin Description — FPD Link Transmitter

Pin Name	I/O	No.	Description
Rn, Gn, Bn, DE, HSYNC, VSYNC	I	51	TTL level input. This includes: 16 Red, 16 Green, 16 Blue, and 3 control lines HSYNC, VSYNC, Data Enable.
AnP	O	8	Positive LVDS differential data output.
AnM	O	8	Negative LVDS differential data output.
CLKIN	I	1	TTL level clock input.
R_FB	I	1	Programmable data strobe select. Rising data strobe edge selected when input is high. (Note 12).
R_FDE	I	1	Programmable control (DE) strobe select. Data active when DE = High when input is high. (Note 12).
CLK1P	O	1	Positive LVDS differential clock output.
CLK1M	O	1	Negative LVDS differential clock output.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) tri-states the outputs, ensuring low current at power down. (Note 12).
PLLSEL	I	1	PLL range select. External resistor network required (See Figure 17). Auto-range active when input is high.
BAL	I	1	Mode select for dc balanced (new) or non-dc balanced (backward compatible) interface. DC balance is active when input is high. (Note 12).
PRE	I	1	Pre-emphasis “on/off” select. Pre-emphasis is active when input is tied to V_{CC} through external pull-up resistor.
DUAL	I	1	Three-mode select for dual pixel, single pixel, or single pixel input to dual pixel output operation. Single pixel mode (only LVDS channels A0 thru A3 active) for power savings. Dual mode is active when input is high. *Figure 17*
V_{CC}	I	4	Power supply pins for TTL inputs.
GND	I	5	Ground pins for TTL inputs.
PLL V_{CC}	I	2	Power supply pin for PLL.
PLL GND	I	3	Ground pins for PLL.
LVDS V_{CC}	I	2	Power supply pin for LVDS outputs.
LVDS GND	I	4	Ground pins for LVDS outputs.
CLK2P NC		1	Additional positive LVDS differential clock output. Identical to CLK1P. No connect if not used.
CLK2M NC		1	Additional negative LVDS differential clock output. Identical to CLK1PM. No connect if not used.

Note 12: Inputs default to “low” when left open due to internal pull-down resistor.

DS90CF388 Pin Description — FPD Link Receiver

Pin Name	I/O	No.	Description
AnP	I	8	Positive LVDS differential data inputs..
AnM	I	8	Negative LVDS differential data inputs.
Rn, Gn, Bn, DE, HSYNC, VSYNC	O	51	TTL level data outputs. This includes: 16 Red, 16 Green, 16 Blue, and 3 control lines — HSYNC, VSYNC, Data Enable.
RxCLK INP	I	1	Positive LVDS differential clock input.
RxCLK INM	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The falling edge acts as data strobe.
R_FDE	I	1	Programmable control (DE) strobe select.
PLLSEL	I	1	PLL range select. External resistor network required (See Figure 17). Auto-range active when input is high.
BALANCED	I	1	Mode select for dc balanced (new) or non-dc balanced (backward compatible) interface. DC balance is active when input is high. (Note 12).
DSSEL	I	1	Deskew and oversampling “on/off” select. Deskew is active when input is high.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
STOPCLK	O	1	Indicates receiver clock signal is not present.
V_{CC}	I	6	Power supply pins for TTL outputs.
GND	I	8	Ground pins for TTL outputs.
PLL V_{CC}	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V_{CC}	I	2	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.
NC		2	No Connect for compatibility with TI receiver.

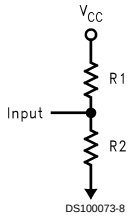


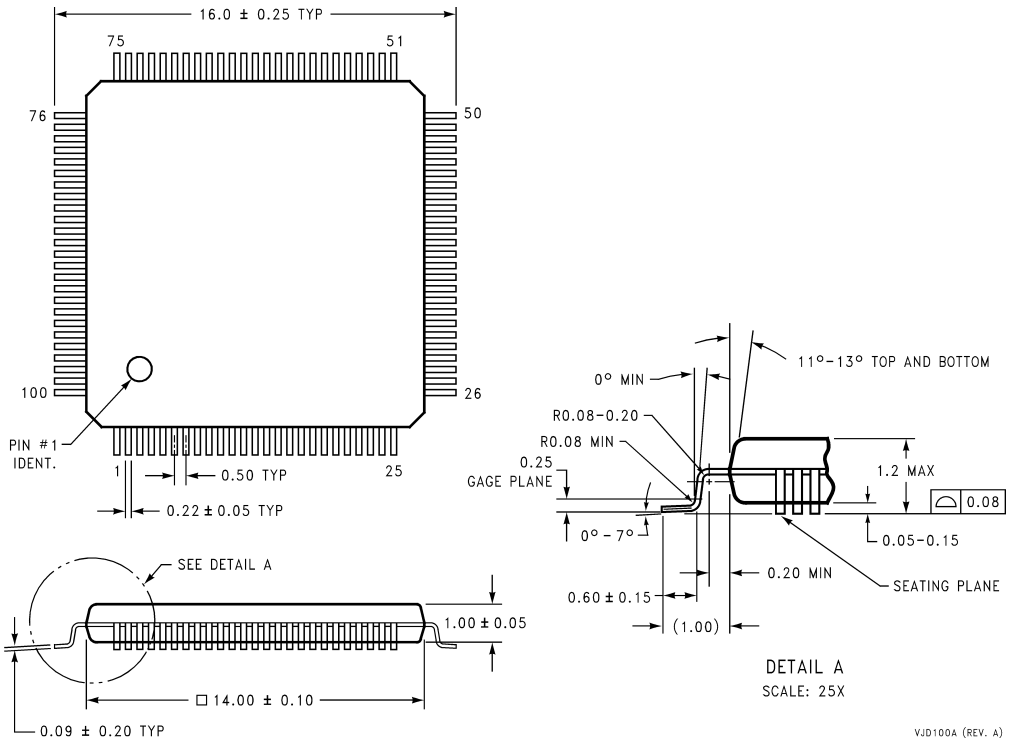
FIGURE 17. Resistor Network for Control Pin Inputs

Applications Information

The transmitter provides a second LVDS output clock. Both LVDS clocks will be identical. This feature supports backward compatibility with the previous generation of devices - the second clock allows the transmitter to interface to panels using a ’dual pixel’ configuration of two receivers.

The 387/388 will also support the transmission of two additional customer defined control signals which are active during blanking while VSYNC is low. The additional control signals, referred to as CNTLE and CNTLF, should be multiplexed with data signals and provided to the transmitter inputs. Inputs B26 and B27 are designated for this purpose. When operating in ’non-balanced’ mode, controls are transmitted on LVDS channels A4 and A5 during the blanking interval. Refer to Table (Control Signals Transmitted During Blanking) for details. These signals may be active only during blanking while VSYNC is low. Control signal levels are latched and held in the last valid state upon entering the data enabled phase. These control signals are available as TTL outputs of the receiver.

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number DS90C387VJD and DS90CF388VJD
NS Package Number VJD100A

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