National Semiconductor

June 1998

DS90C383A/DS90CF383A
+3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link-65 MHz
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DS90C383A/DS90CF383A +3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link-65 MHz, +3.3V LVDS Transmitter 24-Bit Flat Panel Display (FPD)Link-65 MHz

General Description

The DS90C383A/DS90CF383A transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 65 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 227 Mbytes/sec. The DS90C383A transmitter can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. The DS90CF383A is fixed as a Falling edge strobe transmitter. A Rising edge or Falling edge strobe transmitter will interoperate with a Falling edge strobe Receiver (DS90CF384) without any translation logic.

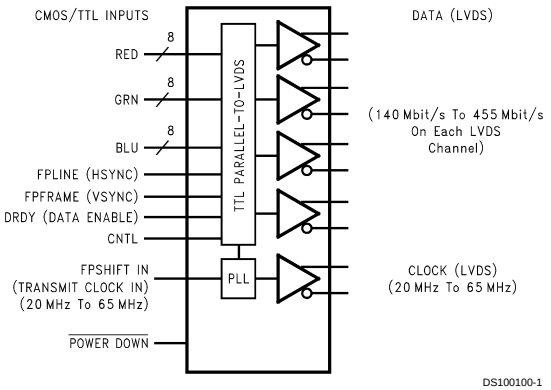
This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- 20 to 65 MHz shift clock support
- Rejects > ± 3ns Jitter from VGA chip with less than 225ps output Jitter @65MHz (TJCC)
- Best–in–Class Set & Hold Times on TxINPUTs
- Tx power consumption <130 mW (typ) @65MHz Grayscale
- >50% Less Power Dissipation than BiCMOS Alternatives
- Tx Power-down mode <200µW (max)
- ESD rating >7 kV (HBM), >500V (EIAJ)
- Supports VGA, SVGA, XGA and Dual Pixel SXGA.
- Narrow bus reduces cable size and cost
- Up to 1.8 Gbps throughput
- Up to 227 Megabytes/sec bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 56-lead TSSOP package
- Improved replacement for:
  SN75LVDS83 — DS90C383A
  SN75LVDS81 — DS90CF383A

Block Diagrams

DS90C383A/DS90CF383A



Order Number DS90C383AMTD or DS90CF383AMTD
See NS Package Number MTD56

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec)	+260˚C
Maximum Package Power Dissipation Capacity @ 25˚C	
MTD56 (TSSOP) Package: DS90C383A/DS90CF383A	1.63 W
Package Derating: DS90C383A/DS90CF383A	12.5 mW/˚C above +25˚C
ESD Rating	
(HBM, 1.5 kΩ, 100 pF)	> 7 kV
(EIAJ, 0Ω, 200 pF)	> 500V

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	˚C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{PP}
TxCLKIN frequency	18		68	MHz

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}			+1.8	+10	µA
		V_{IN} = GND		−10	0		µA
LVDS DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	345	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states					35	mV
V_{OS}	Offset Voltage (Note 4)			1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between complimentary output states					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−3.5	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		31	43	mA
			f = 37.5 MHz		33	45	mA
			f = 65 MHz		39	52	mA
ICCTG	Transmitter Supply Current 16 Grayscale	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern *(Figures 2, 4)*	f = 32.5 MHz		23	35	mA
			f = 37.5 MHz		28	40	mA
			f = 65 MHz		33	45	mA
ICCTZ	Transmitter Supply Current Power Down	$\overline{\text{Power Down}}$ = Low Driver Outputs in TRI-STATE under Power Down Mode			10	55	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: V_{OS} previously referred as V_{CM}.

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
TCIT	TxCLK IN Transition Time *(Figure 5)*			5	ns
TCIP	TxCLK IN Period *(Figure 6)*	14.7	T	55.6	ns
TCIH	TxCLK IN High Time *(Figure 6)*	0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 6)*	0.35T	0.5T	0.65T	ns

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 4)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 4)*			0.75	1.5	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figure 11)* (Note 5)	f = 65 MHz	−0.30	0	0.20	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		1.90	2.20	2.40	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		4.10	4.40	4.60	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		6.30	6.60	6.80	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		8.50	8.80	9.00	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		10.70	11.00	11.20	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		12.90	13.20	13.40	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figure 11)* (Note 5)	f = 40 MHz	−0.35	0	0.35	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		3.22	3.57	3.92	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		6.79	7.14	7.49	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		10.36	10.71	11.06	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		13.93	14.28	14.63	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		17.51	17.86	18.21	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		21.08	21.43	21.78	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figure 11)* (Note 5)	f = 32.5 MHz	−0.40	0	0.40	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		4.00	4.40	4.80	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		8.40	8.80	9.20	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		12.80	13.20	13.60	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		17.20	17.60	18.00	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		21.60	22.00	22.40	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		26.00	26.40	26.80	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 6)*		2.5			ns
THTC	TxIN Hold to TxCLK IN *(Figure 6)*		0			ns
TCCD	TxCLK IN to TxCLK OUT Delay *(Figure 7)* T_A=25˚C,V_{CC}=3.3V		3		5.5	ns
	TxCLK IN to TxCLK OUT Delay *(Figure 7)*		3		7.0	ns
TJCC	Transmitter Jitter Cycle-to-Cycle *(Figures 12, 13)* (Note 6)	f = 65 MHz		175	225	ps
		f = 40 MHz		240	380	ps
		f = 32.5 MHz		260	400	ps
TPLLS	Transmitter Phase Lock Loop Set *(Figure 8)*				10	ms
TPDD	Transmitter Power Down Delay *(Figure 10)*				100	ns

Note 5: The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

Note 6: The Limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. Output jitter is measured with a cycle-to-cycle jitter of 3ns applied to the input clock signal. A jitter event of 3ns, represents worse case jump in the clock edge from most Graphics controller VGA chips currently available. This parameter is used when calculating system margin (RSKM). See Figures 12, 13 and AN-1059.

AC Timing Diagrams

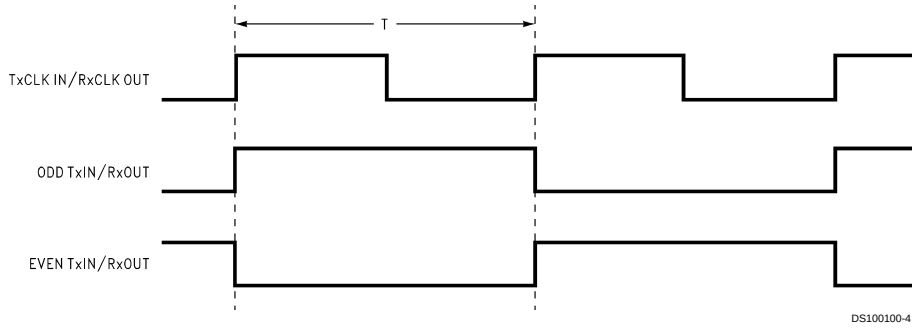


FIGURE 1. "Worst Case" Test Pattern

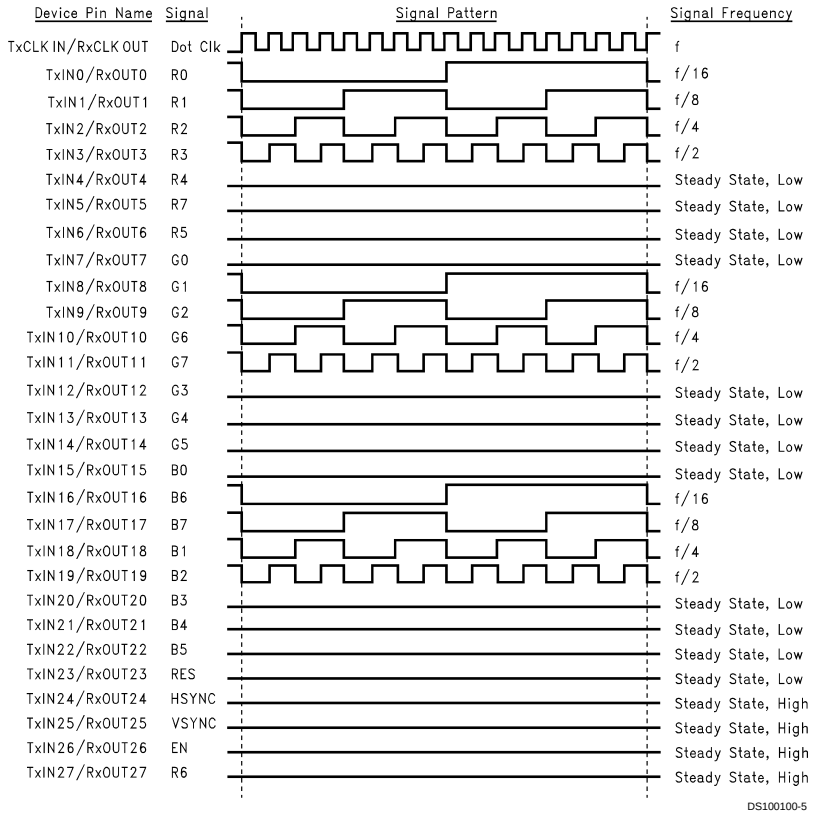


FIGURE 2. "16 Grayscale" Test Pattern (Notes 7, 8, 9, 10)

Note 7: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 8: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 9: *Figures 1, 2* show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Note 10: Recommended pin to signal mapping. Customer may choose to define differently.

AC Timing Diagrams (Continued)

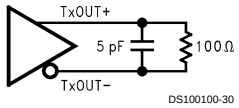


FIGURE 3. DS90C383A/DS90CF383A (Transmitter) LVDS Output Load

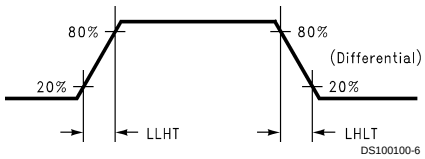


FIGURE 4. DS90C383A/DS90CF383A (Transmitter) LVDS Transition Times

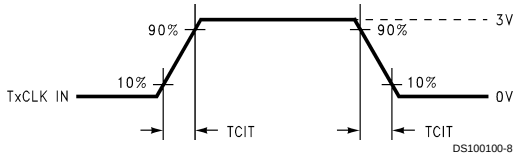


FIGURE 5. DS90C383A/DS90CF383A (Transmitter) Input Clock Transition Time

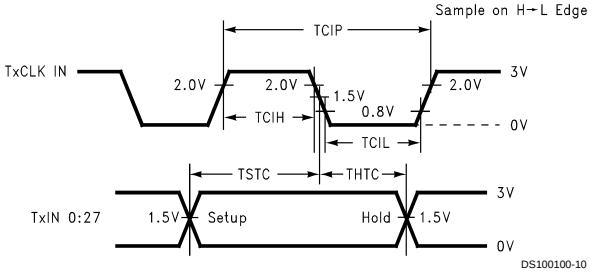


FIGURE 6. DS90C383A/DS90CF383A (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)

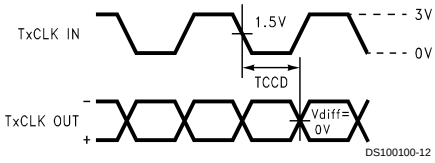


FIGURE 7. DS90C383A/DS90CF383A (Transmitter) Clock In to Clock Out Delay (Falling Edge Strobe)

AC Timing Diagrams (Continued)

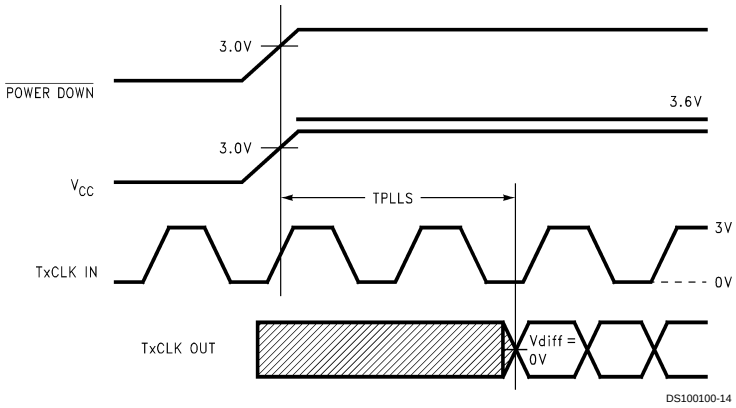


FIGURE 8. DS90C383A/DS90CF383A (Transmitter) Phase Lock Loop Set Time

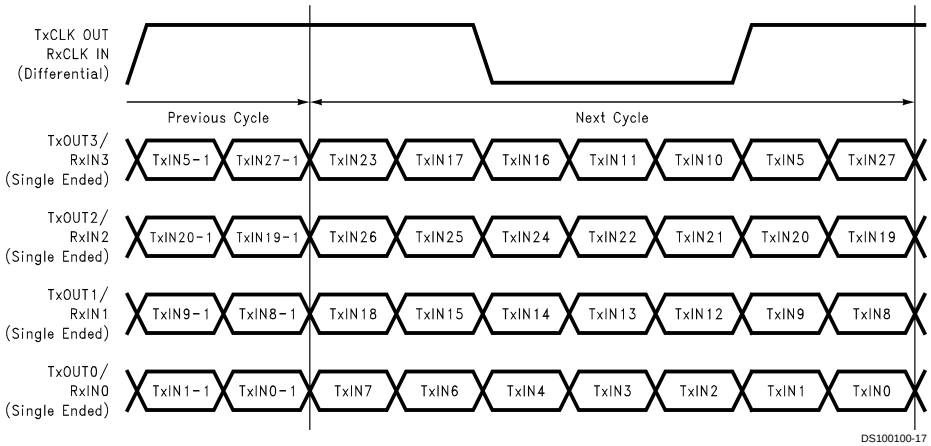


FIGURE 9. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs

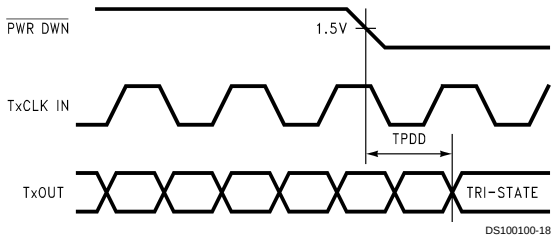


FIGURE 10. Transmitter Power Down Delay

AC Timing Diagrams (Continued)

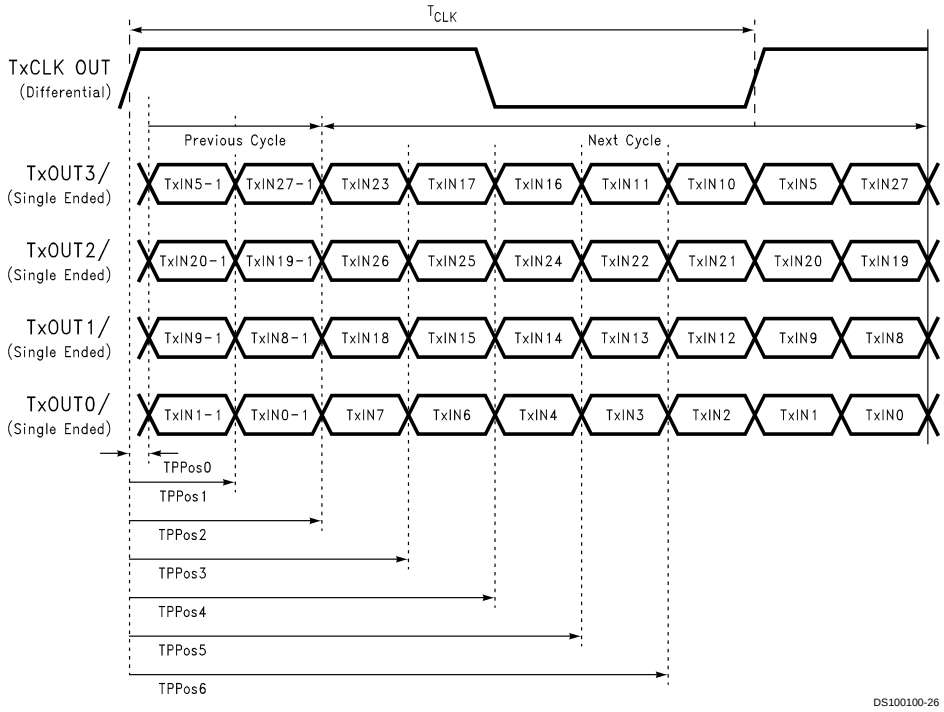


FIGURE 11. Transmitter LVDS Output Pulse Position Measurement

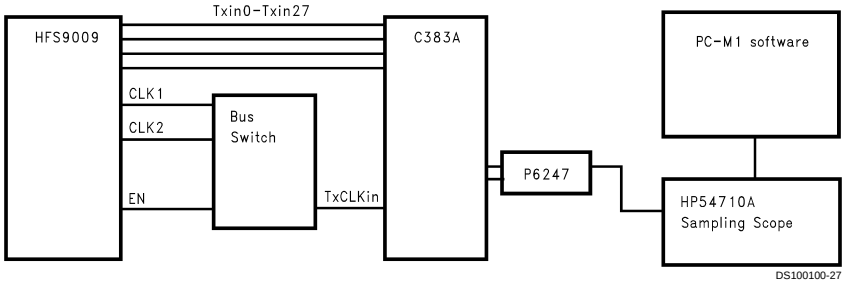


FIGURE 12. TJCC Test Setup

AC Timing Diagrams (Continued)

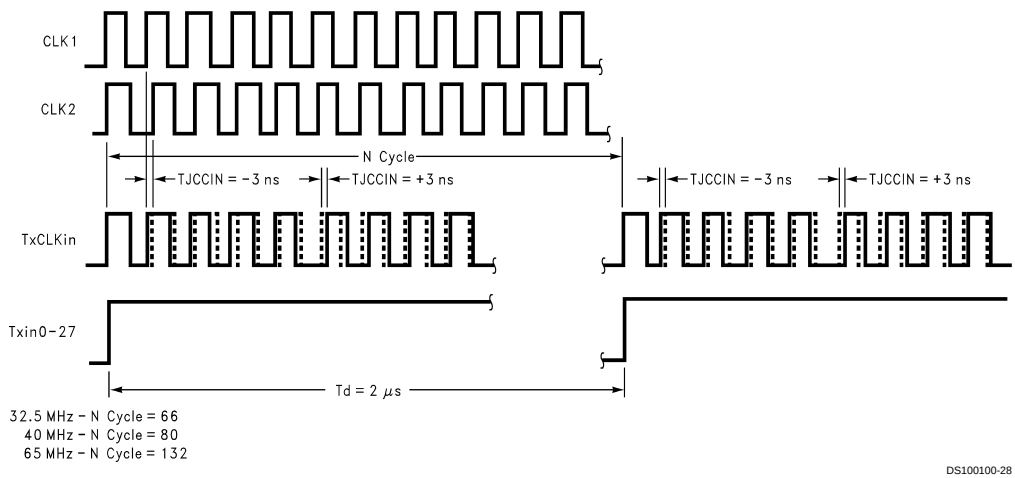


FIGURE 13. Timing Diagram of the Input cycle-to-cycle clock jitter

DS90C383A Pin Description—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable).
TxOUT+	O	4	Positive LVDS differential data output.
TxOUT−	O	4	Negative LVDS differential data output.
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe. Pin name TxCLK IN.
R_FB	I	1	Programmable strobe select (See Table 1).
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT−	O	1	Negative LVDS differential clock output.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	3	Power supply pins for TTL inputs.
GND	I	4	Ground pins for TTL inputs.
PLL V_{CC}	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.

DS90CF383A Pin Description—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable).
TxOUT+	O	4	Positive LVDS differential data output.
TxOUT−	O	4	Negative LVDS differential data output.
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe. Pin name TxCLK IN.
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT−	O	1	Negative LVDS differential clock output.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) TRI-STATES the outputs, ensuring low current at power down.

DS90CF383A Pin Description — FPD Link Transmitter (Continued)

Pin Name	I/O	No.	Description
V_{CC}	I	4	Power supply pins for TTL inputs.
GND	I	4	Ground pins for TTL inputs.
PLL V_{CC}	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.

Applications Information

The DS90C383A/DS90CF383A are backward compatible with the DS90C383/DS90CF383 and are a pin-for-pin replacement. The device (DS90C383A/DS90CF383A) utilizes a different PLL architecture employing an internal 7X clock for enhanced pulse position control.

This device (DS90C383A/DS90CF383A) also features reduced variation of the TCCD parameter which is important for dual pixel applications. (See AN-1084) TCCD variation has been measured to be less than 250ps at 65MHz under normal operating conditions.

This device may also be used as a replacement for the DS90CF583 (5V, 65MHz) and DS90CF581 (5V, 40MHz) FPD-Link Transmitters with certain considerations/ modifications:

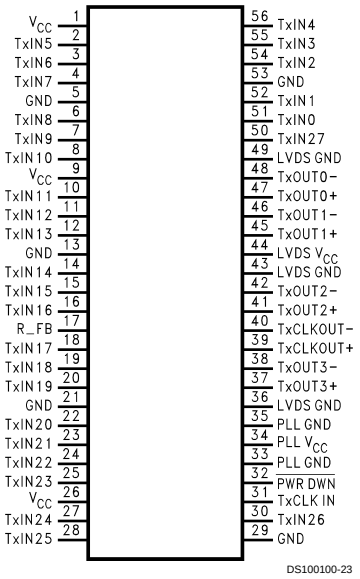
1. Change 5V power supply to 3.3V. Provide this supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC} of the transmitter.
2. The DS90C383A transmitter input and control inputs accept 3.3V TTL/CMOS levels. They are not 5V tolerant.
3. To implement a falling edge device for the DS90C383A, the R_FB pin (pin 17) may be tied to ground OR left unconnected (an internal pull-down resistor biases this pin low). Biasing this pin to Vcc implements a rising edge device.

Transmitter Clock Jitter Cycle-to-Cycle

Figures 12 and 13 illustrate the timing of the input clock relative to the input data. The input clock (TxCLKin) is intentionally shifted to the left −3ns and +3ns to the right when data (Txin0-27) is high. This 3ns of cycle-to-cycle clock jitter is repeated at a period of 2µs, which is the period of the input data (1µs high, 1µs low). At different operating frequencies the N Cycle is changed to maintain the desired 3ns cycle-to-cycle jitter at 2µs period.

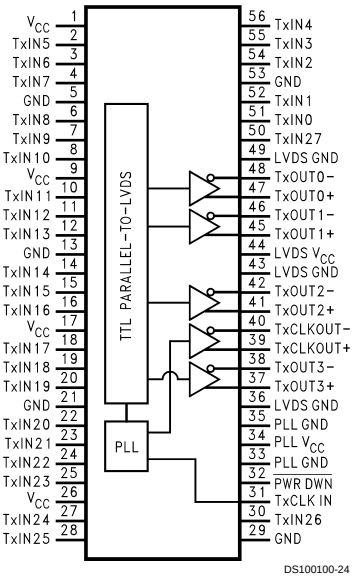
Pin Diagram

DS90C383A



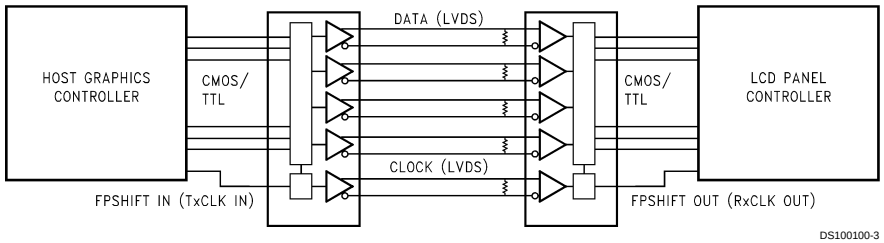
DS100100-23

DS90CF383A



DS100100-24

Application



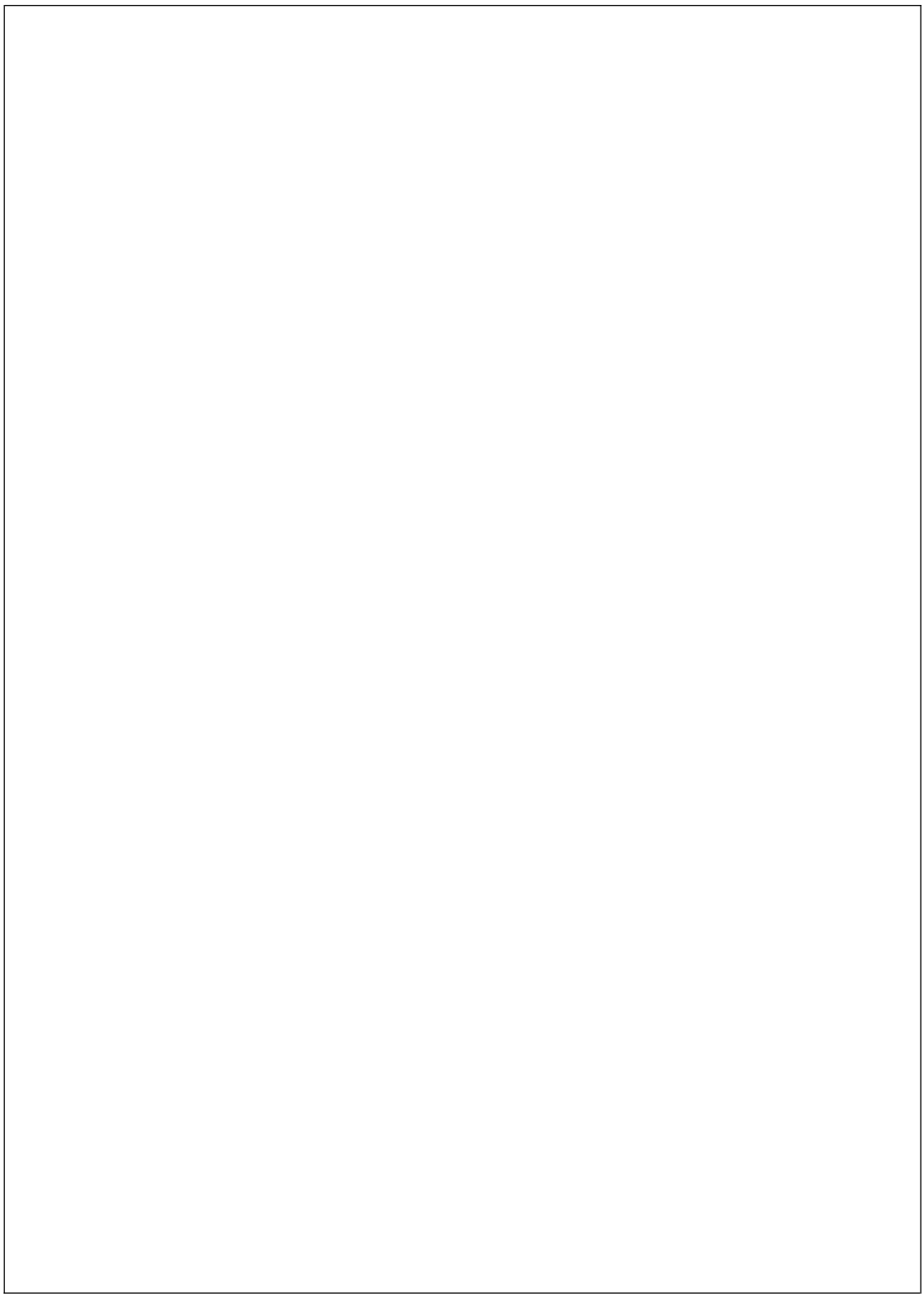
DS100100-3

Truth Table

TABLE 1. Programmable Transmitter (DS90C383A)

Pin	Condition	Strobe Status
R_FB	R_FB = V_{CC}	Rising edge strobe
R_FB	R_FB = GND or NC	Falling edge strobe

Book Extract End



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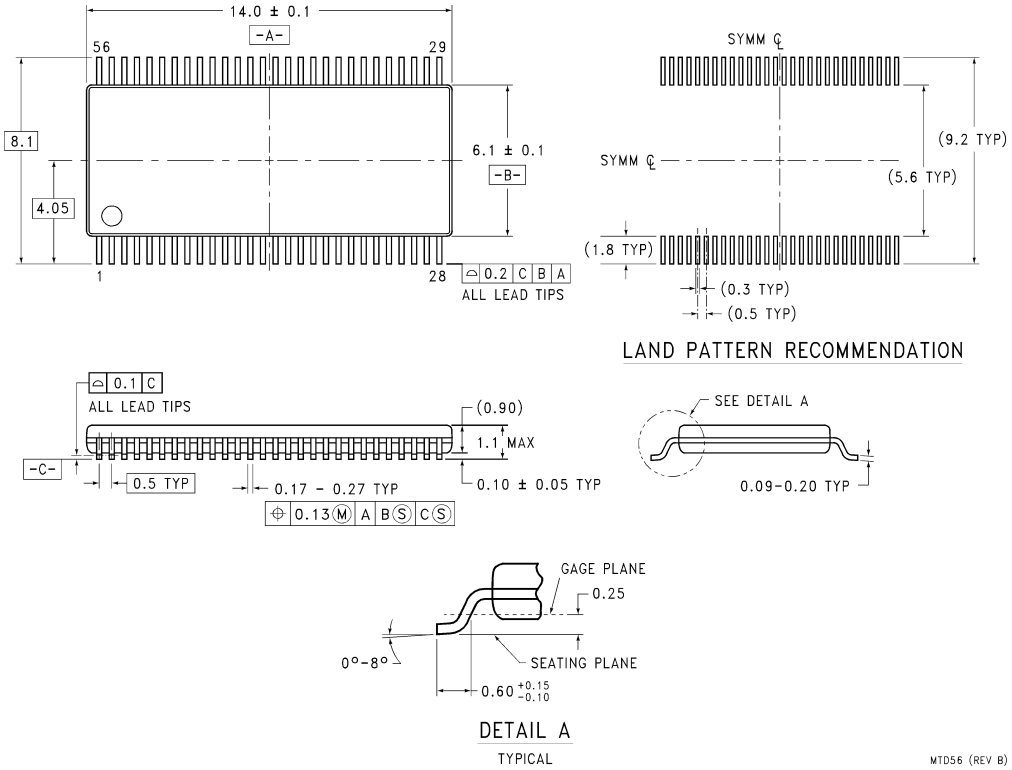
Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Molded Thin Shrink Small Outline Package, JEDEC
Order Number DS90C383AMTD, DS90CF383AMTD
NS Package Number MTD56

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