

DS3662 Quad High Speed Trapezoidal™ Bus Transceiver

General Description

The DS3662 is a quad high speed Schottky bus transceiver intended for use with terminated 120Ω impedance lines. It is specifically designed to reduce noise in unbalanced transmission systems. The open collector drivers generate precise trapezoidal waveforms with rise and fall times of 15 ns (typical), which are relatively independent of capacitive loading conditions on the outputs. This reduces noise coupling to the adjacent lines without any appreciable impact on the maximum data rate obtainable with high speed bus transceivers. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity. Tightly controlled threshold levels on the receiver provide equal rejection to both negative and positive going noise pulses on the bus.

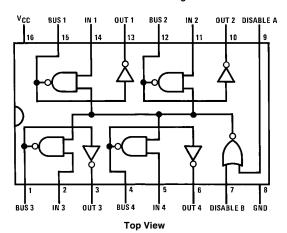
The external termination is intended to be a 180 Ω resistor from the bus to 5V logic supply, together with a 390 Ω resistor from the bus to ground. The bus can be terminated at one or both ends. A two input NOR gate is provided to disable all drivers in a package simultaneously.

Features

- Pin to pin functional replacement for DS8641
- Guaranteed AC specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Temperature insensitive receiver thresholds track bus logic level
- Trapezoidal bus waveforms reduce noise coupling to adiacent lines
- Precision receiver thresholds provide maximum noise immunity and symmetrical response to positive and negative going pulses
- Open collector driver output allows wire-OR connection
- High speed Schottky technology
- \blacksquare 15 μA typical bus termination current with normal V_{CC} or with $V_{CC}=0 \, V$
- Glitch free power up/down protection on the driver output
- TTL compatible driver and disable inputs, and receiver outputs

Block and Connection Diagram

Dual-In-Line Package



TL/F/5803-1

Order Number DS3662J, DS3662N or DS3662WM See NS Package Number J16A, N16A or M16B

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7V
Input and Output Voltage 5.5V
Storage Temperature Range -65°C to +150°C

Maximum Power Dissipation* at 25°C

Cavity Package 1509 mW Molded Package 1476 mW Lead Temperature (Soldering, 4 sec.) 260°C

Recommended Operating Conditions

MinMaxUnitsSupply Voltage (V_{CC})4.755.25VTemperature Range (T_A)070°C*Derate cavity package 10.1 mW/°C above 25°C; derate molder package 11.8 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Тур	Max	Units				
DRIVER AND DISABLE INPUTS										
V_{IH}	Logical "1" Input Voltage		2.0			V				
V_{IL}	Logical "0" Input Voltage				0.8	V				
II	Logical "1" Input Current	$V_{IN} = 5.5V$			1	mA				
I _{IH}	Logical "1" Input Current	$V_{IN} = 2.4V$			40	μΑ				
I _{IL}	Logical "0" Input Current	$V_{IN} = 0.4V$		-1	-1.6	mA				
V_{CL}	Input Diode Clamp Voltage	$I_{CLAMP} = -12 \text{ mA}$		-0.8	-1.5	V				
DRIVER C	OUTPUT/RECEIVER INPUT									
V_{OLB}	Low Level Bus Voltage	$V_{\text{DIS}} = 0.8V$, $V_{\text{IN}} = 2V$, $I_{\text{BUS}} = 100 \text{ mA}$		0.6	0.9	V				
I _{IHB}	Maximum Bus Current	$V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = 5.25V$		10	100	μΑ				
I_{ILB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = 0V$			100	μΑ				
V_{IH}	High Level Receiver Threshold	$V_{IN} = 0.8V, V_{OL} = 16 \text{ mA}$	1.90	1.70		V				
V_{IL}	Low Level Receiver Threshold	$V_{IN} = 0.8V$, $I_{OH} = -400 \mu A$		1.70	1.50	V				
RECEIVE	R OUTPUT									
V_{OH}	Logical "1" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $I_{OH} = -400 \mu A$	2.4	3.2		V				
V_{OL}	Logical "0" Output Voltage	$V_{\text{IN}} = 0.8V$, $V_{\text{BUS}} = 4V$, $I_{\text{OL}} = 16 \text{ mA}$		0.35	0.5	V				
los	Output Short Circuit Current	$V_{DIS} = 0.8V, V_{IN} = 0.8V, V_{BUS} = 0.5V, V_{OS} = 0V, V_{CC} = 5.25V, (Note 4)$	-40	-70	-100	mA				
Icc	Supply Current	$V_{DIS} = 0V, V_{IN} = 2V$		50	90	mA				

Switching Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Тур	Max	Units				
PROPAGATION DELAYS										
t _{PLHD}	Disable to Bus "1"	Figure 1		25	35	ns				
t _{PHLD}	Disable to Bus "0"			25	35	ns				
t _{PLHB}	Driver Input to Bus "1"	Figure 2		20	30	ns				
t _{PHLB}	Driver Input to Bus "0"			20	30	ns				
t _{PLHR}	Bus to Logical "1" Receiver Output	Figure 3		25	40	ns				
t _{PHLR}	Bus to Logical "0" Receiver Output			25	40	ns				
NOISE IMN	MUNITY									
t _{rB} , t _{fB}	Rise and Fall Times (10%-90%) of the Driver Output	Figure 2	10	15	20	ns				
t _{nR}	Receiver Noise Rejection Pulse Width	No Response at Receiver Output as per Figure 4		20	10	ns				

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" and "Recommended Operating Conditions" provide conditions for actual device operation.

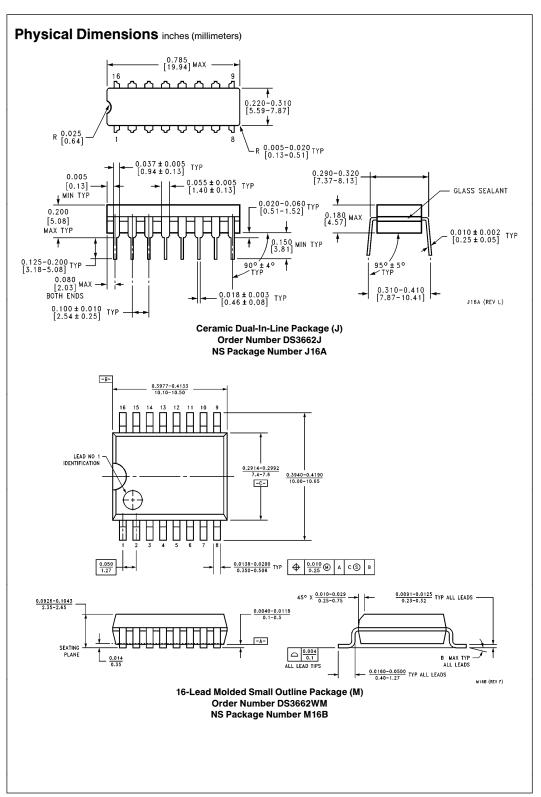
Note 2: Unless otherwise specified min/max limits apply across the supply and temperature range listed in the table of "Recommended Operating Conditions". All typical values are for $T_A = 25^{\circ}C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

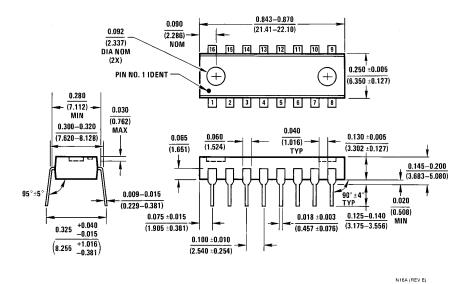
Note 4: Only one output at a time should be shorted.

AC Test Circuits and Switching Waveforms 1.7V ^tPLHD tpHLD. ENABLE TO BUS (LOW LEVEL) TL/F/5803-3 Note: $t_{\rm f}=t_{\rm f}=$ 2.5 ns. Pulse width = 500 ns measured between 1.5V levels. f = 1 MHz. FIGURE 1. Disable Delays DRIVER INPUT TO BUS (LOW LEVEL) DRIVER INPUT TO BUS (HIGH LEVEL) TL/F/5803-4 TL/F/5803-5 Note: $t_f = t_f = 2.5$ ns. Pulse width = 500 ns measured between 1.5V levels. f = 1 MHz. FIGURE 2. Driver Propagation Delays 500 ns RECEIVER ^tPHLR ¹PLHR TL/F/5803-6 TL/F/5803-7 Note: $t_{\rm f}=t_{\rm f}=15~{\rm ns.~Pulse}$ width $=500~{\rm ns}$ measured between 1.7V levels. $f=1~{\rm MHz.}$ FIGURE 3. Receiver Propagation Delays RECEIVER $= t_f = 2.5 \text{ ns}$ (a) Receiver Output (V_O) to Remain Greater than 2.2V BUS LOGIC HIGH LEVEL TL/F/5803-8 TL/F/5803-10 $t_r = t_f = 2.5 \text{ ns}$ (b) Receiver Output (V_O) to Remain Less than 0.7V

FIGURE 4. Receiver Noise Immunity: "No Response at Output" Input Waveforms



Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N) Order Number DS3662N NS Package Number N16A

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