National Semiconductor

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DS26LV32AT
3V Enhanced CMOS Quad Differential Line Receiver

General Description

The DS26LV32A is a high speed quad differential CMOS receiver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS26LV32AT features typical low static I_{CC} of 9 mA which makes it ideal for battery powered and power conscious applications. The TRI-STATE® enables, EN and EN*, allow the device to be active High or active Low. The enables are common to all four receivers.

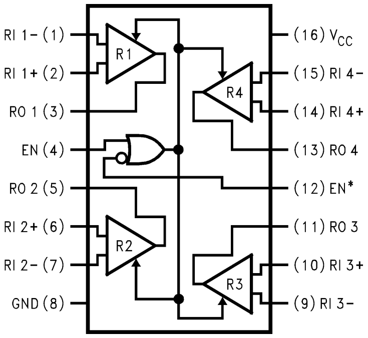
The receiver output (RO) is guaranteed to be High when the inputs are left open. The receiver can detect signals as low as ±200 mV over the common mode range of ±10V. The receiver outputs (RO) are compatible with TTL and LVCMOS levels.

Features

- Low Power CMOS design (30 mW typical)
- Interoperable with existing 5V RS-422 networks
- Industrial Temperature Range
- Meets TIA/EIA-422-B (RS-422) and ITU-T V.11 Recommendation
- 3.3V Operation
- ±7V Common Mode Range @ V_{ID} = 3V
- ±10V Common Mode Range @ V_{ID} = 0.2V
- Receiver OPEN input failsafe feature
- Guaranteed AC Parameter:
  Maximum Receiver Skew: 4 ns
  Maximum Transition Time: 10 ns
- Pin compatible with DS26C32AT
- 32 MHz Toggle Frequency
- > 6.5k ESD Tolerance (HBM)
- Available in SOIC Packaging

Connection Diagram

Dual-In-Line Package



Top View
Order Number DS26LV32ATM
or DS26LV32ATN
See NS Package Number M16A or N16E

Truth Table

Enables		Inputs	Output
EN	EN*	RI+–RI−	RO
L	H	X	Z
All Other Combinations of Enable Inputs		$V_{ID} \geq +0.2V$	H
		$V_{ID} \leq -0.2V$	L
		Open†	H

† Open, not terminated
L = Logic Low
H = Logic High
X = Irrelevant
Z = TRI-STATE

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7V
Enable Input Voltage (EN, EN*)	−0.5V to V_{CC} +0.5V
Receiver Input Voltage (V_{ID}: RI+, RI−)	±14V
Receiver Input Voltage (VCM: RI+, RI−)	±14V
Receiver Output Voltage (RO)	−0.5V to V_{CC} +0.5V
Receiver Output Current (RO)	±25 mA Maximum
Maximum Package Power Dissipation @ +25˚C	
M Package	1190 mW
N Package	1645 mV
Derate M Package 9.8 mW/˚C above +25˚C	
Derate N Package 13.9 mW/˚C above +25˚C	
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature Range Soldering (4 Sec.)	+260˚C
ESD Ratings (HBM, 1.5 kΩ, 100 pF)	
Receiver Inputs and Enables	≥ 6.5 kV
Other Pins	≥ 2 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	˚C

Electrical Characteristics (Notes 2, 3)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{TH}	Differential Input Threshold	$V_{OUT} = V_{OH}$ or V_{OL} V_{CM} = −7V to +7V	RI+, RI−	−200	±17.5	+200	mV
V_{HY}	Hysteresis	V_{CM} = 1.5V			35		mV
V_{IH}	Minimum High Level Input Voltage		EN, EN*	2.0			V
V_{IL}	Maximum Low Level Input Voltage					0.8	V
R_{IN}	Input Resistance	V_{IN} = −7V, +7V (Other Input = GND)	RI+, RI−	5.0	8.5		kΩ
I_{IN}	Input Current (Other Input = 0V, Power On, or V_{CC} = 0V)	V_{IN} = +10V		0	1.1	1.8	mA
		V_{IN} = +3V		0	0.27		mA
		V_{IN} = 0.5V			−0.02		mA
		V_{IN} = −3V		0	−0.43		mA
		V_{IN} = −10V		0	−1.26	−2.2	mA
I_{EN}	Input Current	V_{IN} = 0V to V_{CC}	EN, EN*			±1	µA
V_{OH}	High Level Output Voltage	I_{OH} = −6 mA, V_{ID} = +1V I_{OH} = −6 mA, V_{ID} = OPEN	RO	2.4	3		V
V_{OH}	High Level Output Voltage	I_{OH} = −100 µA, V_{ID} = +1V I_{OH} = − 100 µA, V_{ID} = OPEN			V_{CC} −0.1		V
V_{OL}	Low Level Output Voltage	I_{OL} = +6 mA, V_{ID} = −1V			0.13	0.5	V
I_{OZ}	Output TRI-STATE Leakage Current	V_{OUT} = V_{CC} or GND EN = V_{IL}, EN* = V_{IH}				±50	µA
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{ID} ≥ |200 mV| (Note 4)		−10	−35	−70	mA
I_{CC}	Power Supply Current	No Load, All RI+, R1− = OPEN, EN, EN* = V_{CC} or GND	V_{CC}		9	15	mA

Switching Characteristics (Notes 3, 7, 9, 10)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay High to Low	C_L = 15 pF (*Figures 1, 2*)	6	17.5	35	ns
t_{PLH}	Propagation Delay Low to High		6	17.8	35	ns
t_r	Rise Time (20% to 80%)			4.1	10	ns
t_f	Fall Time (80% to 20%)			3.3	10	ns
t_{PHZ}	Disable Time	C_L = 50 pF (*Figures 3, 4*)			40	ns
t_{PLZ}	Disable Time				40	ns
t_{PZH}	Enable Time				40	ns
t_{PZL}	Enable Time				40	ns
t_{SK1}	Skew, $\|t_{PHL} - t_{PLH}\|$ (Note 5)	C_L = 15 pF		0.3	4	ns
t_{SK2}	Skew, Pin to Pin (Note 6)			0.6	4	ns
t_{SK3}	Skew, Part to Part (Note 7)			7	17	ns
f_{MAX}	Maximum Operating Frequency (Note 8)	C_L = 15 pF	32			MHz

Note 1: “Absolute Maximum ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{ID}.

Note 3: All typicals are given for: V_{CC} = +3.3V, T_A = +25˚C.

Note 4: Short one output at a time to ground. Do not exceed package.

Note 5: t_{SK1} is the $|t_{PHL} - t_{PLH}|$ of a channel.

Note 6: t_{SK2} is the maximum skew between any two channels within a device, either edge.

Note 7: t_{SK3} is the difference in propagation delay times between any channels of any devices. This specification (maximum limit) applies to devices within V_{CC} ±0.1V of one another,and a Delta T_A = ±5˚C (between devices) within the operating temperature range. This parameter is guaranteed by design and characterization.

Note 8: All channels switching, Output Duty Cycle criteria is 40%/60% measured at 50%. Input = 1V to 2V, 50% Duty Cycle, $t_r/t_f \leq$ 5 ns. This parameter is guaranteed by design and characterization.

Parameter Measurement Information

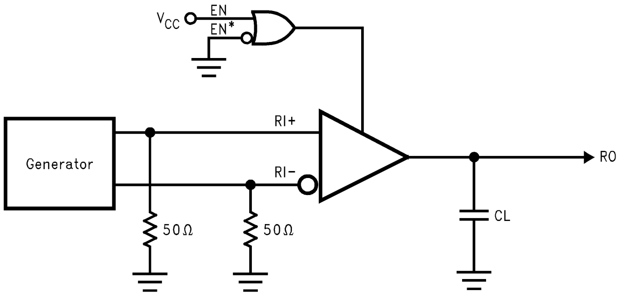

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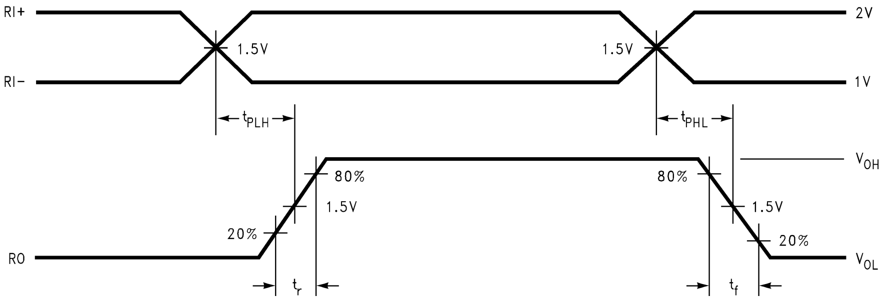
FIGURE 1. Receiver Propagation Delay and Transition Time Test Circuit (Notes 9, 10)

Parameter Measurement Information (Continued)



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Note 9: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Duty Cycle = 50%, Z_O = 50Ω, $t_r \le 10$ ns, $t_f \le 10$ ns.

Note 10: C_L includes probe and jig capacitance.

FIGURE 2. Receiver Propagation Delay and Transition Time Waveform (Notes 9, 10)

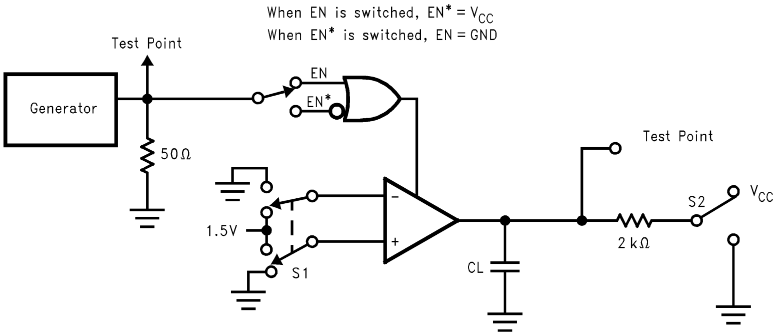

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FIGURE 3. Receive TRI-STATE Test Circuit

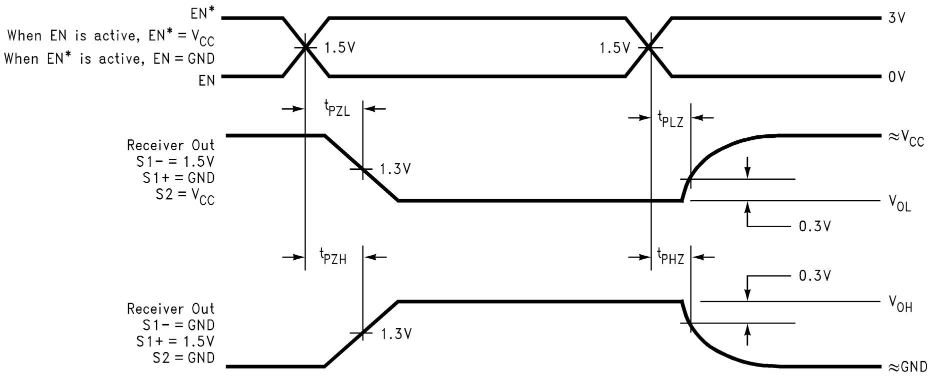

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FIGURE 4. Receiver TRI-STATE Output Enable and Disable Waveforms (Notes 9, 10)

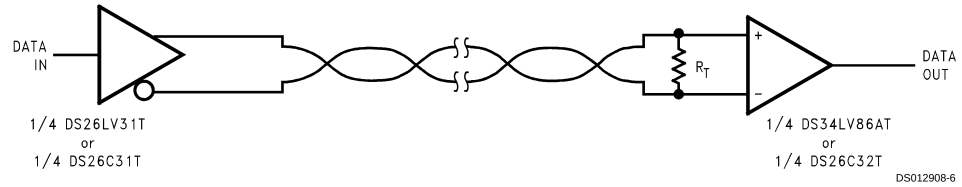
Typical Application Information

General application guidelines and hints for differential drivers and receivers may be found in the following application notes:

AN-214, AN-457, AN-805, AN-847, AN-903, AN-912, AN-916

Power Decoupling Recommendations:

Bypass caps must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1 µF in parallel with 0.01 µF at the power supply pin. A 10 µF or greater solid tantalum or electrolytic should be connected at the power entry point on the printed circuit board.



R_T is optional although highly recommended to reduce reflection

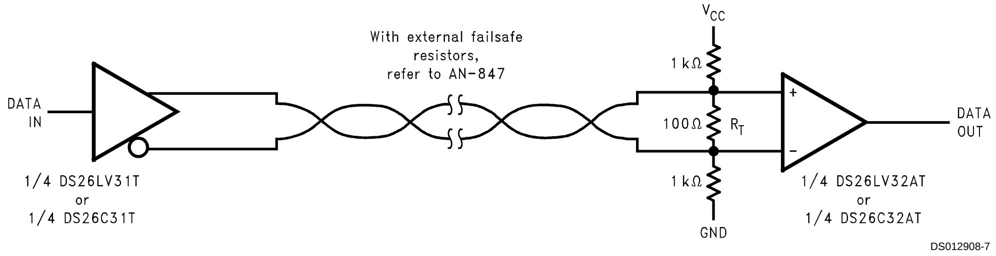


FIGURE 5. Typical Receiver Connections

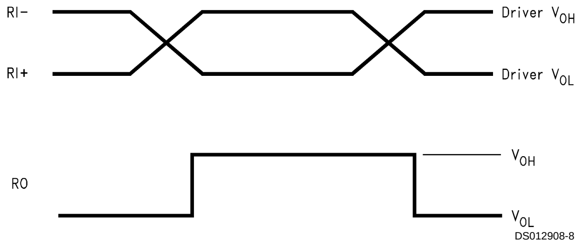


FIGURE 6. Typical Receiver Output Waveforms

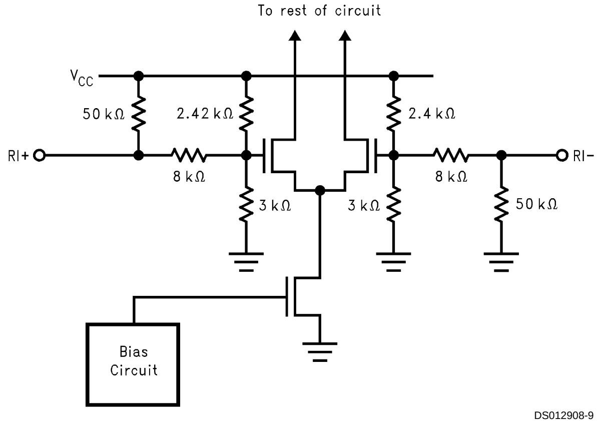


FIGURE 7. Typical Receiver Input Circuit

Typical Application Information (Continued)

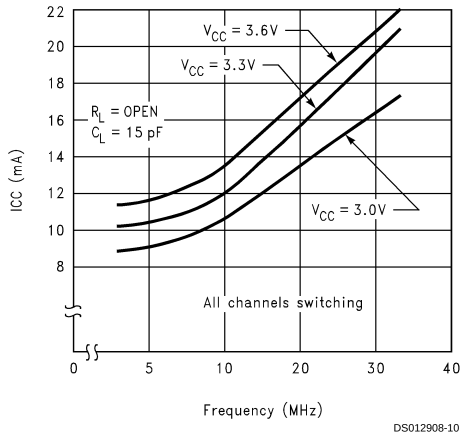


FIGURE 8. Typical I_{CC} vs Frequency

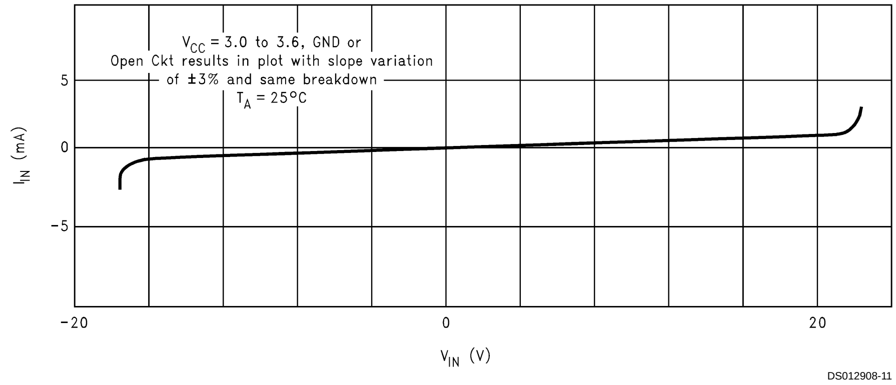


FIGURE 9. Receiver I_{IN} vs V_{IN} (Power On or Power Off)

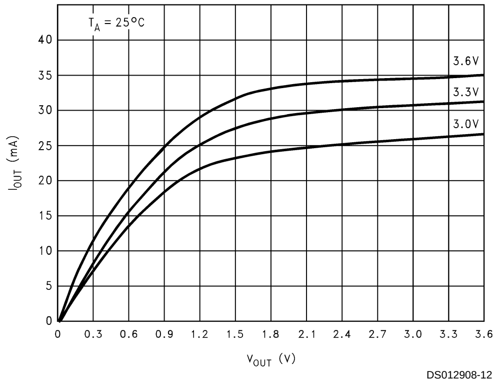


FIGURE 10. I_{OL} vs V_{OL}

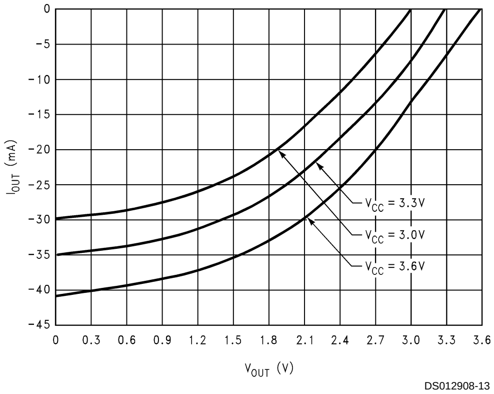
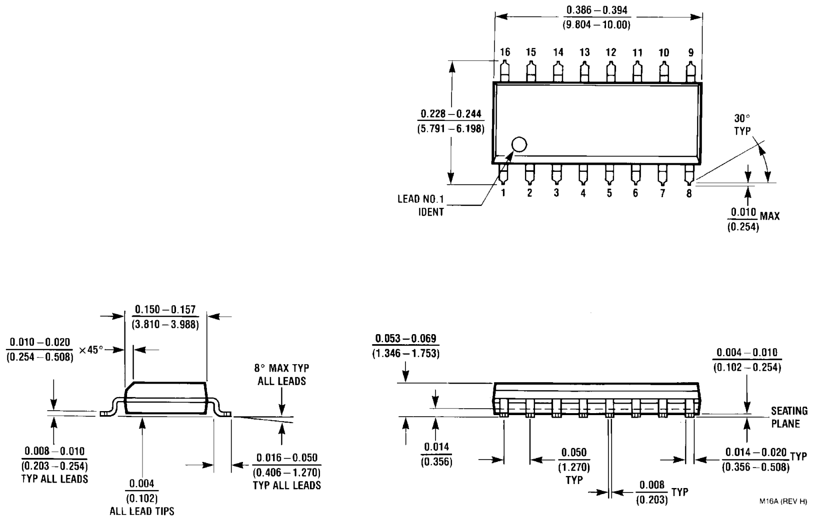


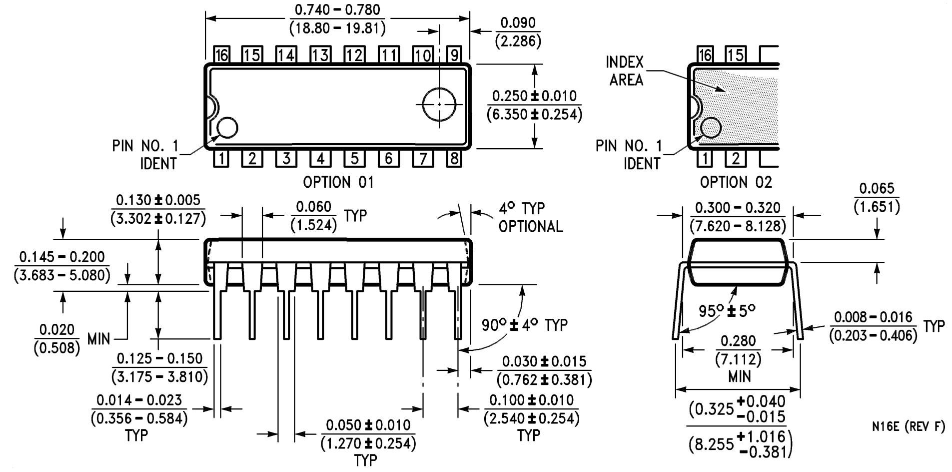
FIGURE 11. I_{OH} vs V_{OH}

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number DS26LV32ATM
NS Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Order Number DS26LV32ATN
NS Package Number N16E

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