National Semiconductor

PRELIMINARY
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DP83952
Repeater Interface Controller with Security Features (RIC™ II)

General Description

The DP83952 RIC II Repeater Interface Controller is an "Enhanced" version of the DP83950 RIC. RIC II is fully backward pin and functional compatible with the RIC. The DP83952 RIC II has the same basic architecture as the RIC with additional feature enhancements. RIC II provides additional network security options, additional statistics for repeater activities, and a faster processor interface. When RIC II is used in a "non-secure" mode, it functions in the same manner as the DP83950 RIC. When RIC II is used in a "secure" mode, it restricts unauthorized nodes from intruding and/or eavesdropping into the network. The RIC II utilizes internal CAMs to store/compare addresses of valid nodes when network security is desired.

RIC II implements the IEEE 802.3 multiport repeater unit specifications. It is fully compliant with the 802.3 repeater specification for the repeater, segment partition, and jabber lockup protection state machines. (Continued)

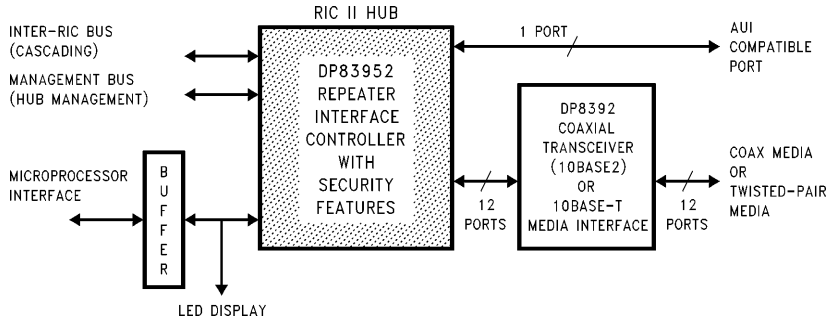
Features

- Compliant with the IEEE 802.3 Repeater Specification
- 13 network connections (ports) per chip
- Selectable on-chip twisted-pair transceivers
- Cascadable for large hub applications
- Compatible with AUI compliant transceivers
- On-chip Elasticity Buffer, Manchester encoder and decoder
- Separate Partition state machines for each port
- Compatible with 802.3k Hub Management requirements
- Provides port status information for LED displays including: receive, collision, partition, link status, and jabber
- Power-up configuration options:
  Repeater and Partition Specifications, Transceiver Interface, Status Display, Processor Operations
- Simple processor interface for repeater management and port disable
- On-chip Event Counters and Event Flag Arrays
- Serial Management Bus Interface to combine packet and repeater status information
- CMOS process for low power dissipation
- Single 5V supply

Security Features

- Power-up configuration options
- Prevents unauthorized eavesdropping and/or intrusion on a per port basis
- 58 on-chip CAMs (Content Addressable Memory) allow storage of acceptable addresses
- Learn mode automatically records addresses of attached nodes

1.0 System Diagram



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General Description (Continued)

The RIC II repeater design consists of two major functional blocks: Segment Specific Block, and Shared Functional Blocks. The Segment Specific Block implements the IEEE repeater requirements on a per network port basis, while the Shared Functional Blocks implement the core logic blocks for the IEEE repeater unit. The Shared Functional Blocks consist of repeater receive multiplexor, an on chip phase lock loop (PLL) decoder for Manchester data, an Elasticity Buffer for preamble regeneration, transmit encoder and demultiplexor for Manchester data.

The DP83952 RIC II can be connected up to 13 cable segments via its network interface ports. One port is fully AUI compatible and is able to connect to an external MAU using the maximum length of AUI cable. The other 12 ports have integrated 10BASE-T transceivers. These transceiver functions may be bypassed so that the RIC II may be used with external transceivers, such as the DP8392 coaxial transceivers.

A large repeater unit can be constructed by cascading RIC IIs together via the Inter-RIC™ bus. All the cascaded RIC IIs form a single repeater unit.

The RIC II is configurable for specific applications. It provides port status information for LED array displays, and a simple interface for system processors. The RIC II possesses multi-function counters and status flag arrays to facilitate network statistics gathering. A serial Hub Management Interface is available for the collection of data in Managed Hub applications.

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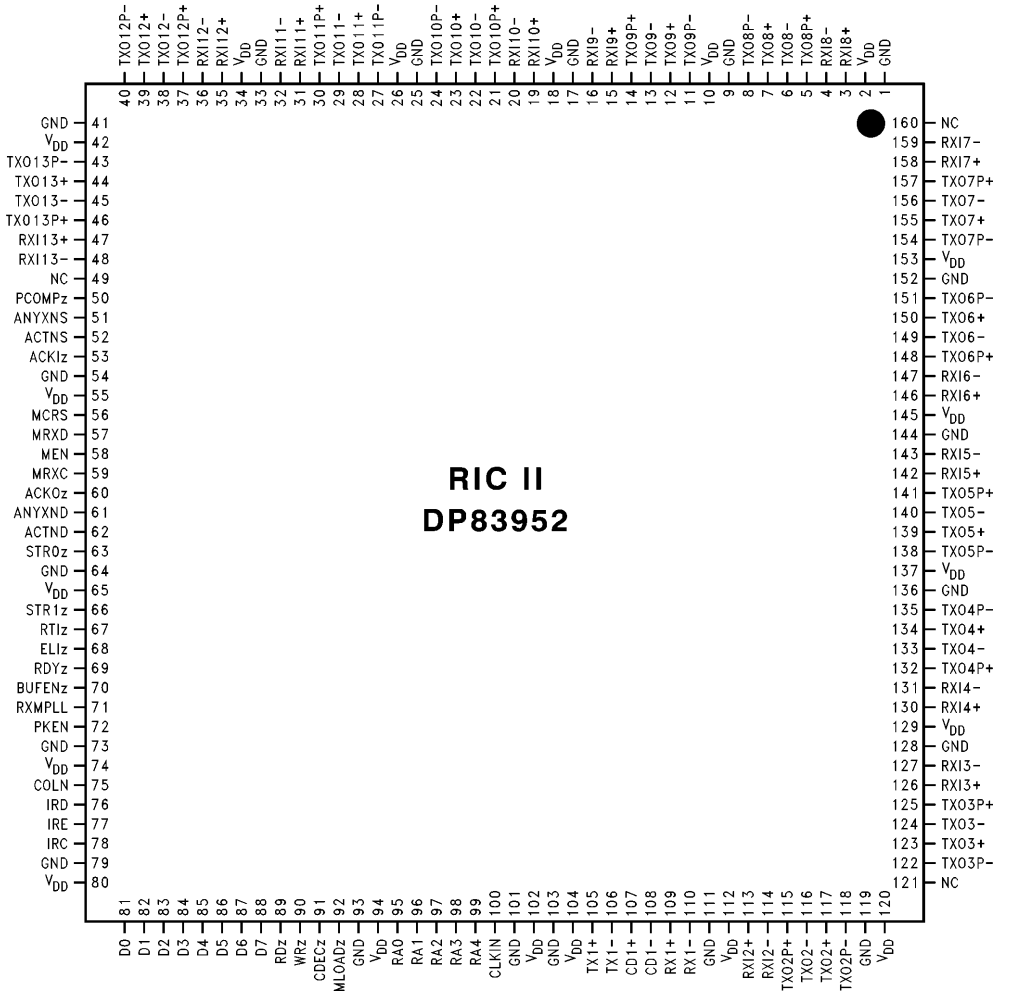
2.0 Connection Diagrams

Pin Table (12 T.P. Ports + 1 AUI Bottom View)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TXO12P−	40	V_{CC}	80	V_{CC}	120	NC	160
TXO12+	39	GND	79	GND	119	RXI7−	159
TXO12−	38	IRC	78	TXO2P−	118	RXI7+	158
TXO12P+	37	IRE	77	TXO2+	117	TXO7P+	157
RXI12−	36	IRD	76	TXO2−	116	TXO7−	156
RXI12+	35	COLN	75	TXO2P+	115	TXO7+	155
V_{CC}	34	V_{CC}	74	RXI2−	114	TXO7P−	154
GND	33	GND	73	RXI2+	113	V_{CC}	153
RXI11−	32	PKEN	72	V_{CC}	112	GND	152
RXI11+	31	RXMPLL	71	GND	111	TXO6P−	151
TXO11P+	30	$\overline{BUFEN}$	70	RX1−	110	TXO6+	150
TXO11−	29	$\overline{RDY}$	69	RX1+	109	TXO6−	149
TXO11+	28	$\overline{ELI}$	68	CD1−	108	TXO6P+	148
TXO11P−	27	$\overline{RTI}$	67	CD1+	107	RXI6−	147
V_{CC}	26	$\overline{STR1}$	66	TX1−	106	RXI6+	146
GND	25	V_{CC}	65	TX1+	105	V_{CC}	145
TXO10P−	24	GND	64	V_{CC}	104	GND	144
TXO10+	23	$\overline{STR0}$	63	GND	103	RXI5−	143
TXO10−	22	ACTND	62	V_{CC}	102	RXI5+	142
TXO10P+	21	ANYXND	61	GND	101	TXO5P+	141
RXI10−	20	$\overline{ACKO}$	60	CLKIN	100	TXO5−	140
RXI10+	19	MRXC	59	PA4	99	TXO5+	139
V_{CC}	18	MEN	58	PA3	98	TXO5P−	138
GND	17	MRXD	57	PA2	97	V_{CC}	137
RXI9−	16	MCRS	56	PA1	96	GND	136
RXI9+	15	V_{CC}	55	PA0	95	TXO4P−	135
TXO9P+	14	GND	54	V_{CC}PLL	94	TXO4+	134
TXO9−	13	$\overline{ACKI}$	53	GNDPLL	93	TXO4−	133
TXO9+	12	ACTNS	52	$\overline{MLOAD}$	92	TXO4P+	132
TXO9P−	11	ANYXNS	51	$\overline{CDEC}$	91	RXI4−	131
V_{CC}	10	$\overline{PCOMP}$	50	$\overline{WR}$	90	RXI4+	130
GND	9	NC	49	$\overline{RD}$	89	V_{CC}	129
TXO8P−	8	RXI13−	48	D7	88	GND	128
TXO8+	7	RXI13+	47	D6	87	RXI3−	127
TXO8−	6	TXO13P+	46	D5	86	RXI3+	126
TXO8P+	5	TXO13−	45	D4	85	TXO3P+	125
RXI8−	4	TXO13+	44	D3	84	TXO3−	124
RXI8+	3	TXO13P−	43	D2	83	TXO3+	123
V_{CC}	2	V_{CC}	42	D1	82	TXO3P−	122
GND	1	GND	41	D0	81	NC	121

Note: NC = No Connect

2.0 Connection Diagrams (Continued)



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Ports 2–13 TP
Port 1 AUI

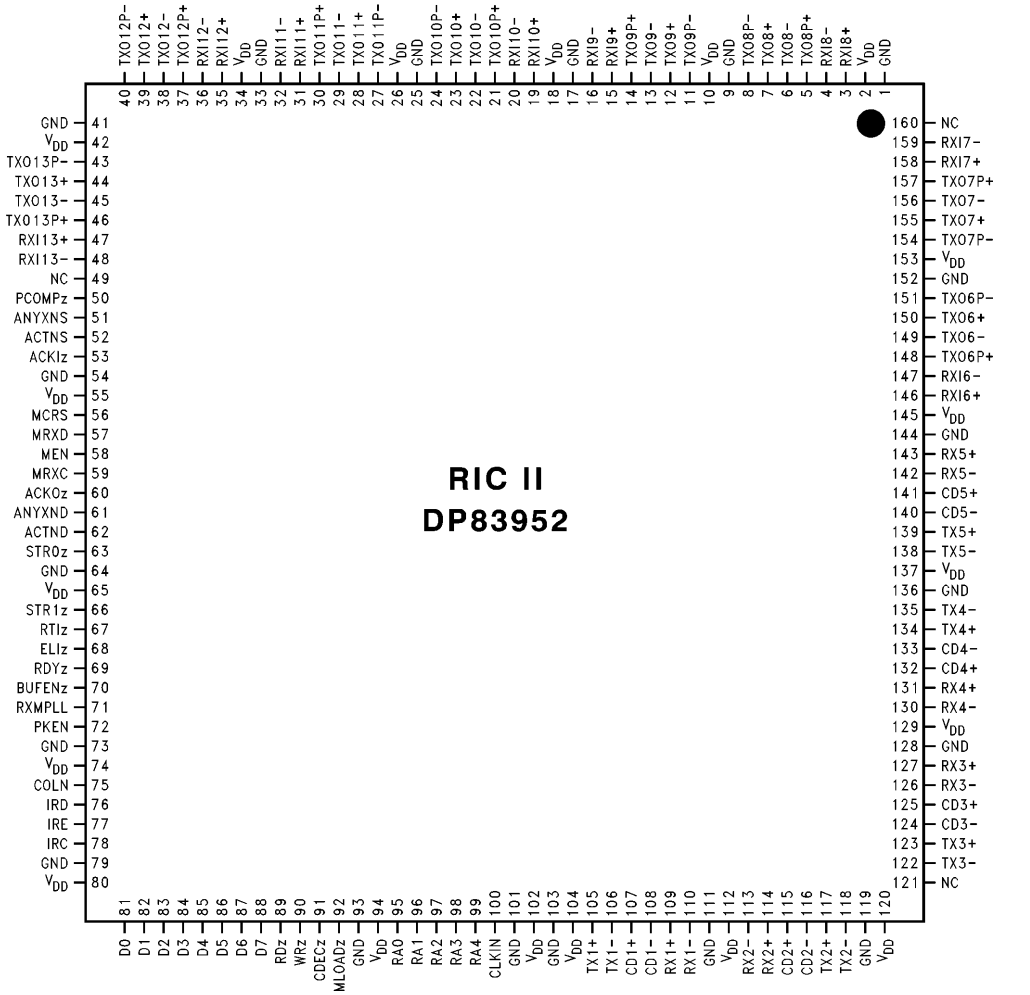
2.0 Connection Diagrams (Continued)

Pin Table (1–5 AUI + 6–13 T.P. Ports)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TXO12P−	40	V_{CC}	80	V_{CC}	120	NC	160
TXO12+	39	GND	79	GND	119	RXI7−	159
TXO12−	38	IRC	78	TX2−	118	RXI7+	158
TXO12P+	37	IRE	77	TX2+	117	TXO7P+	157
RXI12−	36	IRD	76	CD2−	116	TXO7−	156
RXI12+	35	COLN	75	CD2+	115	TXO7+	155
V_{CC}	34	V_{CC}	74	RX2+	114	TXO7P−	154
GND	33	GND	73	RX2−	113	V_{CC}	153
RXI11−	32	PKEN	72	V_{CC}	112	GND	152
RXI11+	31	RXMPLL	71	GND	111	TXO6P−	151
TXO11P+	30	$\overline{BUFEN}$	70	RX1−	110	TXO6+	150
TXO11−	29	$\overline{RDY}$	69	RX1+	109	TXO6−	149
TXO11+	28	$\overline{ELI}$	68	CD1−	108	TXO6P+	148
TXO11P−	27	$\overline{RTI}$	67	CD1+	107	RXI6−	147
V_{CC}	26	$\overline{STR1}$	66	TX1−	106	RXI6+	146
GND	25	V_{CC}	65	TX1+	105	V_{CC}	145
TXO10P−	24	GND	64	V_{CC}	104	GND	144
TXO10+	23	$\overline{STR0}$	63	GND	103	RX5+	143
TXO10−	22	ACTND	62	V_{CC}	102	RX5−	142
TXO10P+	21	ANYXND	61	GND	101	CD5+	141
RXI10−	20	$\overline{ACKO}$	60	CLKIN	100	CD5−	140
RXI10+	19	MRXC	59	PA4	99	TX5+	139
V_{CC}	18	MEN	58	PA3	98	TX5−	138
GND	17	MRXD	57	PA2	97	V_{CC}	137
RXI9−	16	MCRS	56	PA1	96	GND	136
RXI9+	15	V_{CC}	55	PA0	95	TX4−	135
TXO9P+	14	GND	54	V_{CC}PLL	94	TX4+	134
TXO9−	13	$\overline{ACKI}$	53	GNDPLL	93	CD4−	133
TXO9+	12	ACTNS	52	$\overline{MLOAD}$	92	CD4+	132
TXO9P−	11	ANYXNS	51	$\overline{CDEC}$	91	RX4+	131
V_{CC}	10	$\overline{PCOMP}$	50	$\overline{WR}$	90	RX4−	130
GND	9	NC	49	$\overline{RD}$	89	V_{CC}	129
TXO8P−	8	RXI13−	48	D7	88	GND	128
TXO8+	7	RXI13+	47	D6	87	RX3+	127
TXO8−	6	TXO13P+	46	D5	86	RX3−	126
TXO8P+	5	TXO13−	45	D4	85	CD3+	125
RXI8−	4	TXO13+	44	D3	84	CD3−	124
RXI8+	3	TXO13P−	43	D2	83	TX3+	123
V_{CC}	2	V_{CC}	42	D1	82	TX3−	122
GND	1	GND	41	D0	81	NC	121

Note: NC = No Connect

2.0 Connection Diagrams (Continued)



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Ports 6–13 TP
Ports 1–5 AUI

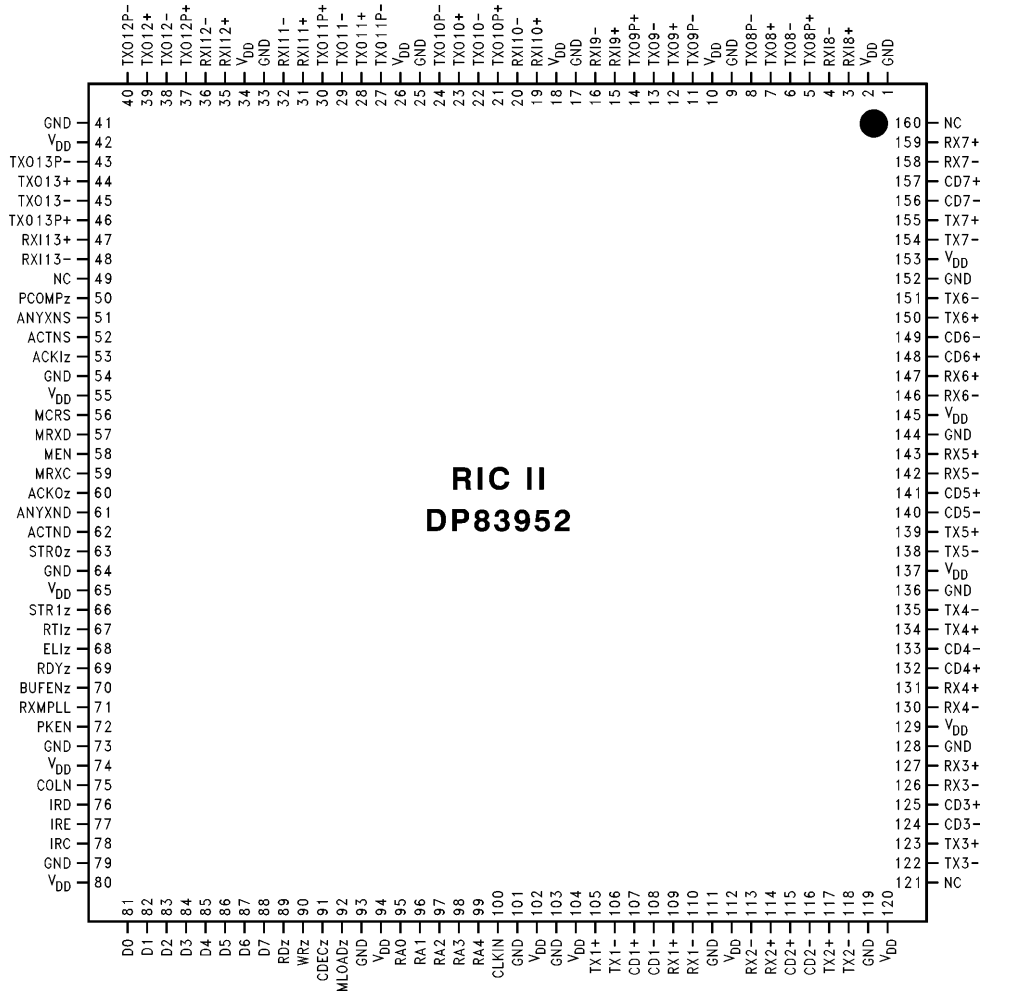
2.0 Connection Diagrams (Continued)

Pin Table (1–7 AUI + 8–13 T.P. Ports)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TXO12P−	40	V_{CC}	80	V_{CC}	120	NC	160
TXO12+	39	GND	79	GND	119	RX7+	159
TXO12−	38	IRC	78	TX2−	118	RX7−	158
TXO12P+	37	IRE	77	TX2+	117	CD7+	157
RXI12−	36	IRD	76	CD2−	116	CD7−	156
RXI12+	35	COLN	75	CD2+	115	TX7+	155
V_{CC}	34	V_{CC}	74	RX2+	114	TX7−	154
GND	33	GND	73	RX2−	113	V_{CC}	153
RXI11−	32	PKEN	72	V_{CC}	112	GND	152
RXI11+	31	RXMPLL	71	GND	111	TX6−	151
TXO11P+	30	$\overline{BUFEN}$	70	RX1−	110	TX6+	150
TXO11−	29	$\overline{RDY}$	69	RX1+	109	CD6−	149
TXO11+	28	$\overline{ELI}$	68	CD1−	108	CD6+	148
TXO11P−	27	$\overline{RTI}$	67	CD1+	107	RX6+	147
V_{CC}	26	$\overline{STR1}$	66	TX1−	106	RX6−	146
GND	25	V_{CC}	65	TX1+	105	V_{CC}	145
TXO10P−	24	GND	64	V_{CC}	104	GND	144
TXO10+	23	$\overline{STR0}$	63	GND	103	RX5+	143
TXO10−	22	ACTND	62	V_{CC}	102	RX5−	142
TXO10P+	21	ANYXND	61	GND	101	CD5+	141
RXI10−	20	$\overline{ACKO}$	60	CLKIN	100	CD5−	140
RXI10+	19	MRXC	59	PA4	99	TX5+	139
V_{CC}	18	MEN	58	PA3	98	TX5−	138
GND	17	MRXD	57	PA2	97	V_{CC}	137
RXI9−	16	MCRS	56	PA1	96	GND	136
RXI9+	15	V_{CC}	55	PA0	95	TX4−	135
TXO9P+	14	GND	54	V_{CC}PLL	94	TX4+	134
TXO9−	13	$\overline{ACKI}$	53	GNDPLL	93	CD4−	133
TXO9+	12	ACTNS	52	$\overline{MLOAD}$	92	CD4+	132
TXO9P−	11	ANYXNS	51	$\overline{CDEC}$	91	RX4+	131
V_{CC}	10	$\overline{PCOMP}$	50	$\overline{WR}$	90	RX4−	130
GND	9	NC	49	$\overline{RD}$	89	V_{CC}	129
TXO8P−	8	RXI13−	48	D7	88	GND	128
TXO8+	7	RXI13+	47	D6	87	RX3+	127
TXO8−	6	TXO13P+	46	D5	86	RX3−	126
TXO8P+	5	TXO13−	45	D4	85	CD3+	125
RXI8−	4	TXO13+	44	D3	84	CD3−	124
RXI8+	3	TXO13P−	43	D2	83	TX3+	123
V_{CC}	2	V_{CC}	42	D1	82	TX3−	122
GND	1	GND	41	D0	81	NC	121

Note: NC = No Connect

2.0 Connection Diagrams (Continued)



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Ports 8–13 TP
Ports 1–7 AUI

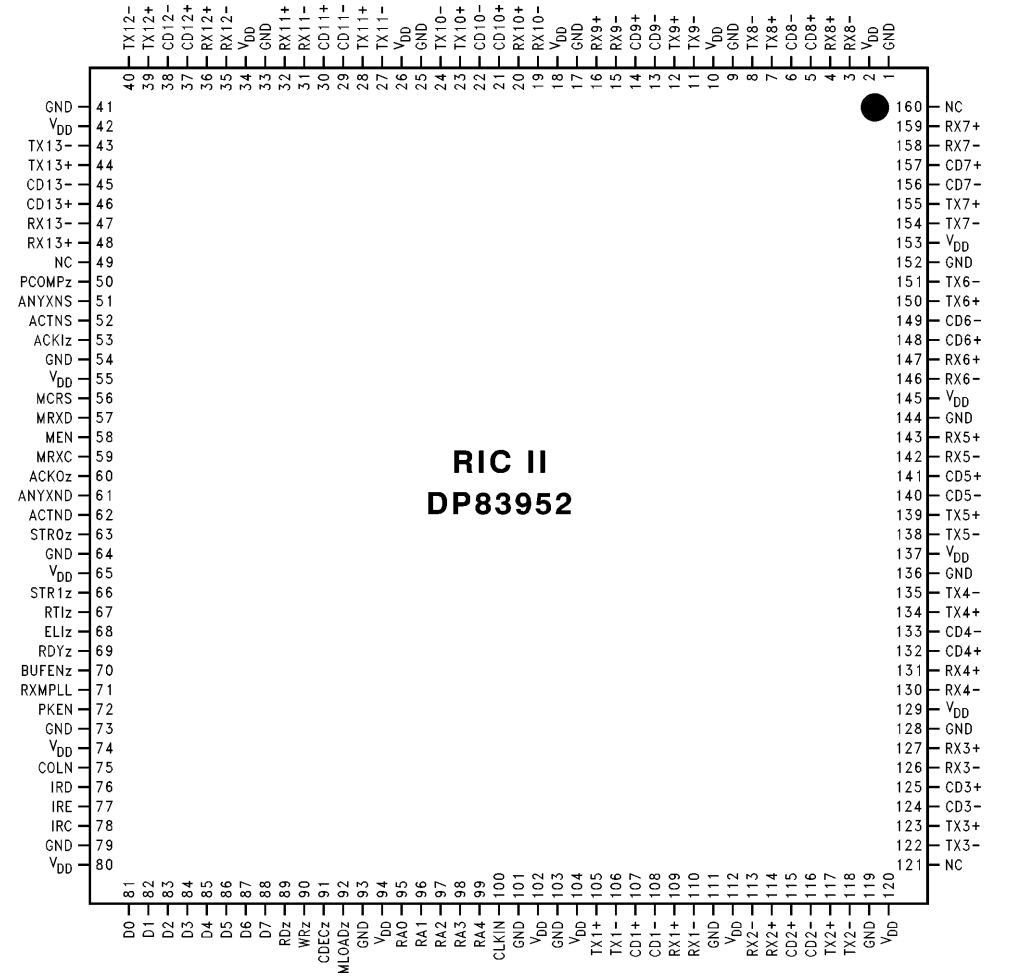
2.0 Connection Diagrams (Continued)

Pin Table (All AUI Ports)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TX12−	40	V_{CC}	80	V_{CC}	120	NC	160
TX12+	39	GND	79	GND	119	RX7+	159
CD12−	38	IRC	78	TX2−	118	RX7−	158
CD12+	37	IRE	77	TX2+	117	CD7+	157
RX12+	36	IRD	76	CD2−	116	CD7−	156
RX12−	35	COLN	75	CD2+	115	TX7+	155
V_{CC}	34	V_{CC}	74	RX2+	114	TX7−	154
GND	33	GND	73	RX2−	113	V_{CC}	153
RX11+	32	PKEN	72	V_{CC}	112	GND	152
RX11−	31	RXMPLL	71	GND	111	TX6−	151
CD11+	30	$\overline{BUFEN}$	70	RX1−	110	TX6+	150
CD11−	29	$\overline{RDY}$	69	RX1+	109	CD6−	149
TX11+	28	$\overline{ELI}$	68	CD1−	108	CD6+	148
TX11−	27	$\overline{RTI}$	67	CD1+	107	RX6+	147
V_{CC}	26	$\overline{STR1}$	66	TX1−	106	RX6−	146
GND	25	V_{CC}	65	TX1+	105	V_{CC}	145
TX10−	24	GND	64	V_{CC}	104	GND	144
TX10+	23	$\overline{STR0}$	63	GND	103	RX5+	143
CD10−	22	ACTND	62	V_{CC}	102	RX5−	142
CD10+	21	ANYXND	61	GND	101	CD5+	141
RX10+	20	$\overline{ACKO}$	60	CLKIN	100	CD5−	140
RX10−	19	MRXC	59	PA4	99	TX5+	139
V_{CC}	18	MEN	58	PA3	98	TX5−	138
GND	17	MRXD	57	PA2	97	V_{CC}	137
RX9+	16	MCRS	56	PA1	96	GND	136
RX9−	15	V_{CC}	55	PA0	95	TX4−	135
CD9+	14	GND	54	V_{CC}PLL	94	TX4+	134
CD9−	13	$\overline{ACKI}$	53	GNDPLL	93	CD4−	133
TX9+	12	ACTNS	52	$\overline{MLOAD}$	92	CD4+	132
TX9−	11	ANYXNS	51	$\overline{CDEC}$	91	RX4+	131
V_{CC}	10	$\overline{PCOMP}$	50	$\overline{WR}$	90	RX4−	130
GND	9	NC	49	$\overline{RD}$	89	V_{CC}	129
TX8−	8	RX13+	48	D7	88	GND	128
TX8+	7	RX13−	47	D6	87	RX3+	127
CD8−	6	CD13+	46	D5	86	RX3−	126
CD8+	5	CD13−	45	D4	85	CD3+	125
RX8+	4	TX13+	44	D3	84	CD3−	124
RX8−	3	TX13−	43	D2	83	TX3+	123
V_{CC}	2	V_{CC}	42	D1	82	TX3−	122
GND	1	GND	41	D0	81	NC	121

Note: NC = No Connect

2.0 Connection Diagrams (Continued)



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All AUI Ports

3.0 Pin Description

Pin Name	Driver Type	I/O	Description
NETWORK INTERFACE PINS (**On-Chip** Transceiver Mode)			
RXI2− to RXI13−	TP	I	Twisted Pair **R**eceive **I**nput Negative
RXI2+ to RXI13+	TP	I	Twisted Pair **R**eceive **I**nput Positive
TXOP2− to TXOP13−	TT	O	Twisted Pair **P**re-Emphasis **T**ransmit **O**utput Negative
TXO2− to TXO13−	TT	O	Twisted Pair **T**ransmit **O**utput Negative
TXO2+ to TXO13+	TT	O	Twisted Pair **T**ransmit **O**utput Positive
TXOP2+ to TXOP13+	TT	O	Twisted Pair **P**re-Emphasis **T**ransmit **O**utput Positive
CD1+	AL	I	AUI **C**ollision **D**etect Input Positive
CD1−	AL	I	AUI **C**ollision **D**etect Input Negative
RX1+	AL	I	AUI **R**eceive Input Positive
RX1−	AL	I	AUI **R**eceive Input Negative
TX1+	AD	O	AUI **T**ransmit Output Positive
TX1−	AD	O	AUI **T**ransmit Output Negative
NETWORK INTERFACE PINS (**External** Transceiver Mode **AUI Signal Level Compatibility Selected**)			
TX2+ to TX13+	AL	O	**T**ransmit Output Positive
TX2− to TX13−	AL	O	**T**ransmit Output Negative
CD2+ to CD13+	AL	I	**C**ollision Input Positive
CD2− to CD13−	AL	I	**C**ollision Input Negative
RX2+ to RX13+	AL	I	**R**eceive Input Positive
RX2− to RX13−	AL	I	**R**eceive Input Negative
CD1+	AL	I	AUI **C**ollision **D**etect Input Positive
CD1−	AL	I	AUI **C**ollision **D**etect Input Negative
RX1+	AL	I	AUI **R**eceive Input Positive
RX1−	AL	I	AUI **R**eceive Input Negative
TX1+	AD	O	AUI **T**ransmit Output Positive
TX1−	AD	O	AUI **T**ransmit Output Negative

Note: AD = **A**UI level and **D**rive compatible, **TP** = **T**wisted **P**air interface compatible, **AL** = **A**UI **L**evel compatible, **TT** = **TT**L compatible, **I** = **I**nput, **O** = **O**utput, **B** = **B**i-directional, **Z** = TRI-STATE®, **C** = **C**MOS compatible.

3.0 Pin Description (Continued)

Pin Name	Driver Type	I/O	Description
PROCESSOR BUS PINS			
RA0–RA4	TT	I	**R**EGISTER **A**DDRESS INPUTS: These five pins are used to select a register to be read or written. The state of these inputs are ignored when the read, write and mode load input strobes are high. (Even under these conditions these inputs must not be allowed to float to an undefined logic state).
$\overline{\text{STR0}}$	C	O	DISPLAY UPDATE **STR**OBE 0 **Maximum Display Mode:** This signal controls the latching of display data for network ports 1 to 7 into the off chip display latches. **Minimum Display Mode:** This signal controls the latching of display data for the RIC II into the off chip display latch. During processor access cycles (read or write is asserted) this signal is inactive (high).
$\overline{\text{STR1}}$	C	O	DISPLAY UPDATE **STR**OBE 1 **Maximum Display Mode:** This signal controls the latching of display data for network ports 8 to 13 into the off-chip display latches. **Minimum Display Mode:** No operation During processor access cycles (read or write is asserted) this signal is inactive (high).
D0–D7	TT	B, Z	**D**ATA BUS: (Note 1) **Display Update Cycles:** These pins become outputs providing display data and port address information. Address information only available in Maximum Display mode. **Processor Access Cycles:** Data input or output is performed via these pins. The read, write and mode load inputs control the direction of the signals.
$\overline{\text{BUFEN}}$	C	O	**BUF**FER **EN**ABLE: This output controls the TRI-STATE operation of the bus transceiver which provides the interface between the RIC II's data pins and the processor's data bus. (Note 2)
$\overline{\text{RDY}}$	C	O	DATA **R**EA**DY** STROBE: The falling edge of this signal during a read cycle indicates that data is stable and valid for sampling. In write cycles the falling edge of $\overline{\text{RDY}}$ denotes that the write data has been latched by the RIC II. Therefore data must have been available and stable for this operation to be successful.
$\overline{\text{ELI}}$	C	O	**E**VENT **L**OGGING **I**NTERRUPT: A low level on the $\overline{\text{ELI}}$ output indicates the RIC II's hub management logic requires CPU attention. The interrupt is cleared by accessing the Port Event Recording register or Event Counter that produced it. All interrupt sources may be masked.
$\overline{\text{RTI}}$	C	O	**R**EAL **T**IME **I**NTERRUPT: A low level on the $\overline{\text{RTI}}$ output indicates the RIC II's real time (packet specific) interrupt logic requires CPU attention. The interrupt is cleared by reading the Real Time Interrupt Status register. All interrupt sources may be masked.
$\overline{\text{CDEC}}$	TT	I	**C**OUNTER **DEC**REMENT: A rising edge on the $\overline{\text{CDEC}}$ input strobe decrements all of the RIC II's Port Event Counters by one. This input is internally synchronized and if necessary the operation of the signal is delayed if there is a simultaneous internally generated counting operation.
$\overline{\text{WR}}$	TT	I	**WR**ITE STROBE: Strobe from the CPU used to write an internal register defined by the RA0–RA4 inputs.
$\overline{\text{RD}}$	TT	I	**R**EA**D** STROBE: Strobe from the CPU used to read an internal register defined by the RA0–RA4 inputs.
$\overline{\text{MLOAD}}$	TT	I	DEVICE RESET AND **M**ODE **LOAD:** When this input is low all of the RIC II's state machines, counters and network ports are reset and held inactive. On the rising edge of $\overline{\text{MLOAD}}$ the logic levels present on the D0–7 pins and RA0–RA4 inputs are latched into the RIC II's configuration registers. The rising edge of $\overline{\text{MLOAD}}$ also signals the beginning of the display test operation.

Note 1: The data pins remain in their display update function, i.e., asserted as outputs unless either the read or write strobe is asserted.

Note 2: The buffer enable output indicates the function of the data pins. When it is high they are performing display update cycles, when it is low a processor access or mode load cycle is occurring.

3.0 Pin Description (Continued)

Pin Name	Driver Type	I/O	Description
INTER-RIC BUS PINS			
$\overline{\text{ACKI}}$	TT	I	**ACK**NOWLEDGE **I**NPUT: Input to the network ports' arbitration chain.
$\overline{\text{ACKO}}$	TT	O	**ACK**NOWLEDGE **O**UTPUT: Output from the network ports' arbitration chain.
IRD	TT	B, Z	**I**NTER-**R**IC **D**ATA: When asserted as an output this signal provides a serial data stream in NRZ format. The signal is asserted by a RIC II when it is receiving data from one of its network segments. The default condition of this signal is to be an input. In this state it may be driven by other devices on the Inter-RIC bus.
IRE	TT	B, Z	**I**NTER-**R**IC **E**NABLE: When asserted as an output this signal provides an activity framing enable for the serial data stream. The signal is asserted by a RIC II when it is receiving data from one of its network segments. The default condition of this signal is to be an input. In this state it may be driven by other devices on the Inter-RIC bus.
IRC	TT	B, Z	**I**NTER-**R**IC **C**LOCK: When asserted as an output this signal provides a clock signal for the serial data stream. Data (IRD) is changed on the falling edge of the clock. The signal is asserted by a RIC II when it is receiving data from one of its network segments. The default condition of this signal is to be an input. When an input IRD is sampled on the rising edge of the clock. In this state it may be driven by other devices on the Inter-RIC bus.
COLN	TT	B, Z	**COL**LISION ON PORT **N**: This denotes that a collision is occurring on the port receiving the data packet. The default condition of this signal is to be an input. In this state it may be driven by other devices on the Inter-RIC bus.
PKEN	C	O	**P**AC**K**ET **EN**ABLE: This output acts as an active high enable for an external bus transceiver (if required) for the IRE, IRC, IRD and COLN signals. When high the bus transceiver should be transmitting on to the bus, i.e. this RIC II is driving the IRD, IRE, IRC, and COLN bus lines. When low the bus transceiver should receive from the bus.
CLKIN	TT	I	40 MHz **CL**OC**K IN**PUT: This input is used to generate the RIC II's timing reference for the state machines, and phase lock loop decoder.
ACTND	OD	O	**ACT**IVITY ON PORT **N D**RIVE: This output is active when the RIC II is receiving data or collision information from one of its network segments.
ACTNS	TT	I	**ACT**IVITY ON PORT **N S**ENSE: This input senses when this or another RIC II in a multi-RIC II system is receiving data or collision information.
ANYXND	OD	O	**A**CTIVITY ON A**NY** PORT E**X**CLUDING PORT **N D**RIVE: This output is active when a RIC II is experiencing a transmit collision or multiple ports have active collisions on their network segments.
ANYXNS	TT	I	**A**CTIVITY ON A**NY** PORT E**X**CLUDING PORT **N S**ENSE: This input senses when this RIC II or other RIC IIs in a multi-RIC II system are experiencing transmit collisions or multiple ports have active collisions on their network segments.

TT = **TT**L compatible, **B** = **B**i-directional, **C** = CMOS compatible, **OD** = **O**pen **D**rain, **I** = **I**nput, **O** = **O**utput

3.0 Pin Description (Continued)

Pin Name	Driver Type	I/O	Description
MANAGEMENT BUS PINS			
MRXC	TT	O, Z	**M**ANAGEMENT **R**ECEIVE **C**LOCK: When asserted this signal provides a clock signal for the MRXD serial data stream. The MRXD signal is changed on the falling edge of this clock. The signal is asserted when a RIC II is receiving data from one of its network segments. Otherwise the signal is inactive.
MCRS	TT	B, Z	**M**ANAGEMENT **C**ARRIER **S**ENSE: When asserted this signal provides an activity framing enable for the serial data stream. The signal is asserted when a RIC II is receiving data from one of its network segments. Otherwise the signal is an input.
MRXD	TT	O, Z	**M**ANAGEMENT **R**ECEIVE **D**ATA: When asserted this signal provides a serial data stream in NRZ format. The data stream is made up of the data packet and RIC II status information. The signal is asserted when a RIC II is receiving data from one of its network segments. Otherwise the signal is inactive.
MEN	C	O	**M**ANAGEMENT BUS OUTPUT **EN**ABLE: This output acts as an active high enable for an external bus transceiver (if required) for the MRXC, $\overline{\text{MCRS}}$ and MRXD signals. When high the bus transceiver should be transmitting on to the bus.
$\overline{\text{PCOMP}}$	TT	I	**P**ACKET **COMP**RESS: This input is used to activate the RIC II's packet compress logic. A low level on this signal when $\overline{\text{MCRS}}$ is active will cause that packet to be compressed. If $\overline{\text{PCOMP}}$ is tied low all packets are compressed, if $\overline{\text{PCOMP}}$ is tied high packet compression is inhibited.
POWER AND GROUND PINS			
V_{CC}			Positive Supply
GND			Negative Supply
EXTERNAL DECODER PINS			
RXM	TT	O	**R**ECEIVE DATA MANCHESTER FORMAT: This output makes the data, in Manchester format, received by port N available for test purposes. If not used for testing this pin should be left open.

TT = **TT**L compatible, **B** = **B**i-directional, **C** = CMOS compatible, **OD** = **O**pen **D**rain, **I** = **I**nput, **O** = **O**utput

4.0 Block Diagram

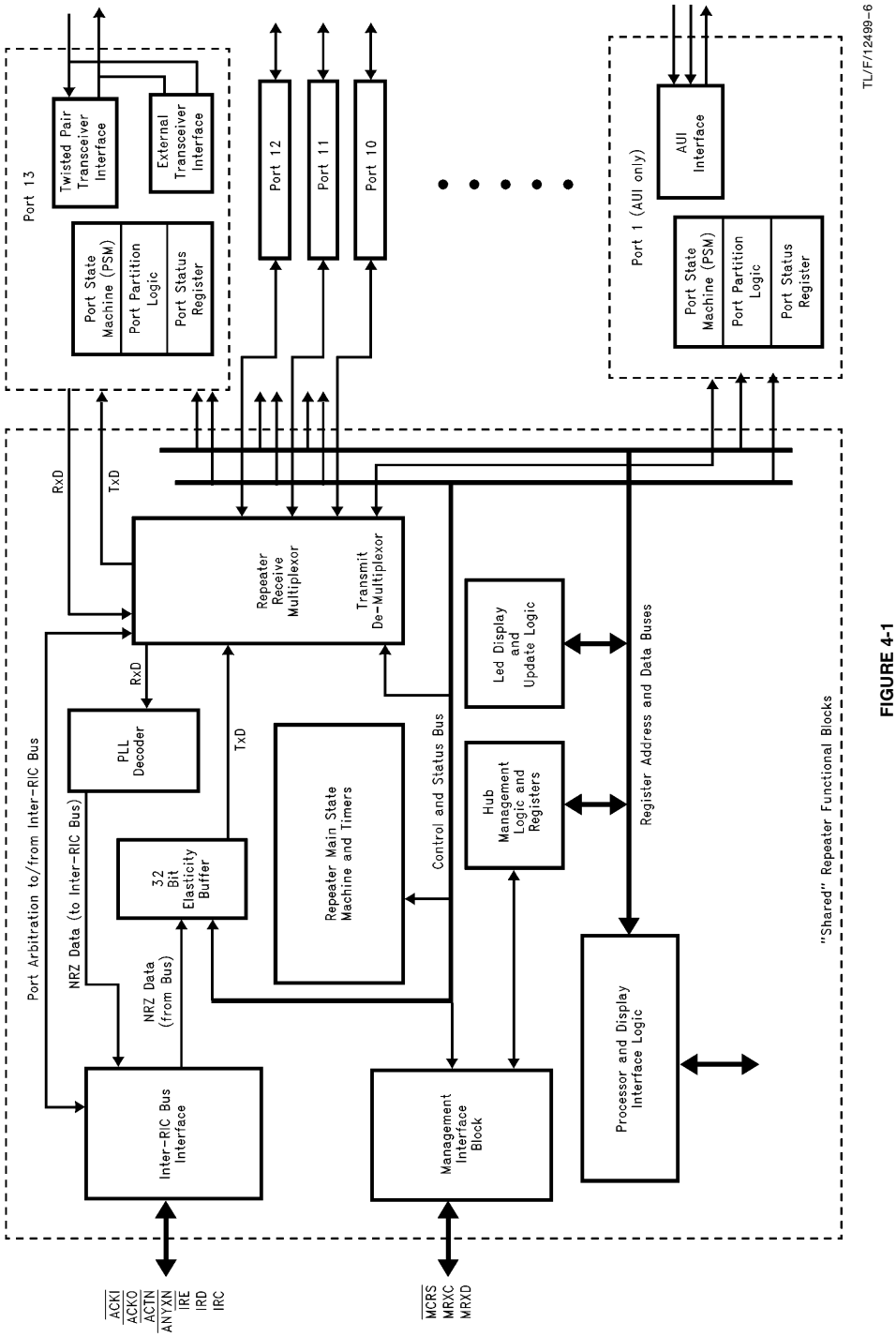
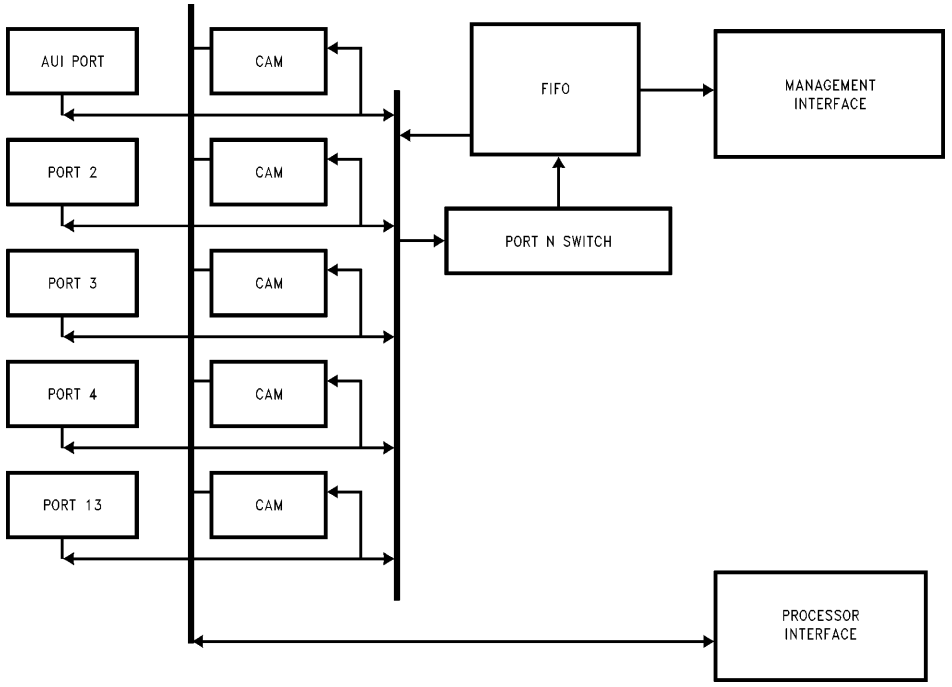


FIGURE 4-1

4.0 Block Diagram (Continued)

RIC II Port Architecture Block Diagram



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Note: The block diagram for the RIC II, when used in the non-secure mode, is identical to the block diagram for the RIC device (*Figure 4-1*). When RIC II is used in the secure mode, the added functional blocks for the security logic are used in the operation of the device (*Figure 4-1a*).

FIGURE 4-1a

5.0 Functional Description

The IEEE 802.3 repeater specification details a number of functions a repeater system must perform. These requirements allied with a need for the implementation to be multiport strongly favors the choice of a modular design style. In such a design, functionality is split between those tasks common to all data channels and those exclusive to each individual channel. The RIC II follows this approach, certain functional blocks are replicated for each network attachment, (also known as a repeater port), and others are shared.

The following sections provide an overview of the RIC II architecture. First, RIC II feature enhancements from the RIC is discussed. Then, the RIC II functional blocks are described.

5.1 SUMMARY OF DP83952 RIC II FEATURE ENHANCEMENTS FROM DP83950B RIC

1. Pin Compatibility. The DP83952VUL RIC II is fully pin compatible with the DP83950BVQB RIC device in the 160-pin Plastic Quad Flat Pack (PQFP) package.
2. Addition of network security. The DP83952 RIC II features significant per port security capability. As a single chip repeater, RIC II provides security using 58 internal CAM (Content Addressable Memory) locations for all 13 ports.

   Unauthorized nodes can be restricted from intruding and/or eavesdropping into the network by preventing them from having access to valid packet data. The RIC II utilizes internal CAMs to store/compare addresses of valid nodes. Complete security operation of RIC II is explained later in this datasheet.
3. Two dedicated CAM locations per port and 32 shareable CAM entries are provided to store Ethernet addresses. Both the port and the shareable CAM locations (48 bits wide) are on-chip.
4. Faster processor access for efficient data gathering.
5. Addition of thirteen 8-bit wide counters for collecting more statistics.

5.2 OVERVIEW OF RIC II FUNCTIONS

SEGMENT SPECIFIC BLOCK: NETWORK PORT

As shown in the Block Diagram, the segment specific blocks consist of:

1. One or more physical layer interfaces.
2. A logic block required for performing repeater operations upon that particular segment. This is known as the ''port'' logic since it is the access ''port'' the segment has to the rest of the network.

This function is repeated 13 times in the RIC II (one for each port) and is shown on the right side of the Block Diagram, *Figure 4-1*.

The physical layer interface depends upon the port. Port 1 has an AUI compliant interface for use with AUI compatible transceiver boxes and cable. Ports 2 to 13 may be configured for use with one of two interfaces: twisted pair or an external transceiver. The former utilizes the RIC II's on-chip 10BASE-T transceivers, the latter allows connection to external transceivers. When using the external transceiver mode the interface is AUI compatible. Although AUI compatible transceivers are supported, when an interface cable is used, external transceivers should always be used for the repeater system.

Inside the port logic there are 4 distinct functions:

1. The port state machine ''PSM'' is required to perform data and collision repetition as described by the repeater specification, for example, it determines whether this port should be receiving from or transmitting to its network segment.
2. The port partition logic implements the segment partitioning algorithm. This algorithm is defined by the IEEE specification and is used to protect the network from malfunctioning segments.
3. The port status register reflects the current status of the port. It may be accessed by a system processor to obtain this status or to perform certain port configuration operations, such as port disable.
4. The Port Security Configuration Logic determines if the packet data will be transmitted/received intact, or as pseudo random data. Two dedicated CAM locations per port are available for learning/storing/comparing port source addresses.

SHARED FUNCTIONAL BLOCKS: REPEATER CORE LOGIC

The shared functional blocks consists of the Repeater Main State Machine (MSM), Timers, a 32-bit Elasticity Buffer, PLL Decoder, Receive and Transmit Multiplexors, and Security Logic with 32 shareable CAM locations. These blocks perform the majority of the operations needed to fulfill the requirements of the IEEE repeater specification.

When a packet is received by a port it is sent via the Receive Multiplexor to the PLL Decoder. Notification of the data and collision status is sent to the main state machine via the receive multiplexor and collision activity status signals. This enables the main state machine to determine the source of the data to be repeated and the type of data to be transmitted, either data or jam pattern.

When a collision occurs, in accordance with IEEE repeater specifications, the transmit data will be a preamble/jam pattern consisting of a 1010 . . . bit pattern. Whenever a collision occurs, (during the preamble, the address field, the ''type field'', or the data field) the RIC II switches to the jam pattern immediately.

When RIC II is configured in the ''non-secure'' mode, the valid received data field is transmitted to all other ports (excluding the port with the received packet).

When RIC II is configured in the ''secure'' mode, the source and destination addresses within each packet are first checked. Based on this comparison, and the port configuration either:

1. a pseudo random bit pattern during the data field (of the packet) is transmitted to the particular port. Or,
2. the received data is transmitted intact.

The data remains intact on the Inter-RIC bus so other cascaded repeaters could compare the destination address with their local CAMs. On a valid source address mismatch, RIC II shall switch to random pattern both on the local transmitting ports and the Inter-RIC bus.

5.0 Functional Description (Continued)

The main state machine is associated with a series of timers. These ensure various IEEE specification times (referred to as the TW1 to TW6 times) are fulfilled.

A repeater unit is required to meet the same signal jitter performance as any receiving node attached to a network segment. Consequently, a phase locked loop Manchester decoder is required so that the packet may be decoded, and the jitter accumulated over the receiving segment recovered. The decode logic outputs data in non-return to zero (NRZ) format with an associated clock and enable. In this form, the packet is in a convenient format for transfer to other devices, such as network controllers and other RIC IIs, via the Inter-RIC bus (described later). The data may then be re-encoded into Manchester data and transmitted.

Reception and transmission via physical layer transceiver units causes a loss of bits in the preamble field of a data packet. The repeater specification requires this loss to be regenerated. To accomplish this, an elasticity buffer is employed to temporarily store bits in the data field of the packet.

The sequence of operation is as follows. Soon after the network segment receiving the data packet has been identified, the RIC II begins to transmit the packet preamble pattern (1010...) onto the other network segments. While the preamble is being transmitted, the Elasticity Buffer monitors the decoded received clock and data signals (this is done via the Inter-RIC bus as described later). When the start of frame delimiter ''SFD'' is detected, the received data stream is written into the elasticity buffer. Removal of data from the buffer for retransmission is not allowed until a valid length preamble pattern has been transmitted.

Internal CAMs

For security purposes, RIC II employs two sets of CAMs (Content Addressable Memory) for address comparison: port CAMs, and shared CAMs.

PORT CAMs

RIC II provides two CAM locations (48 bits wide) per port for comparison. The two CAM locations hold the source address(es) for the incoming packets on that port. The addresses can be stored (CPU access), or learned (Learn mode). External processor/logic access to these two CAM locations is not advised or allowed while in learning mode, LME = 1, since the contents of the register may not be valid. Once the addresses are learned, then they are used to make source address and destination address comparisons. An address is learned when the packet is received with a valid CRC. External processor/logic access to these registers is fine while learning is not in progress, LME = 0 in the port security configuration register.

SHARED CAMs

RIC II provides thirty-two shareable CAM locations (48 bits wide) to store the Ethernet addresses associated with the ports. The Ethernet addresses are stored by writing to these CAM locations where the addresses could be shared among the thirteen ports. By using shared CAMs, multiple Ethernet addresses can be associated with a single port, or multiple ports can be allocated to a single Ethernet address. After the destination address of the received packet is completely buffered, RIC II will compare this address with the stored addresses in the CAM locations. The source address is compared in a similar fashion. These shared CAM locations are only user definable, and will not be filled during the learning mode.

A CAM entry could be shared among the thirteen local ports. This is done through a 16-bit CAM Location Mask Register (CLMR). Each CAM entry has one of these CLMRs, therefore there are 32 registers for the 32 CAM entries. These registers could be accessed by a processor.

Since register access is performed on a byte basis, six write cycles must be done to program/enter the Ethernet address into the CAM. The upper 3 bits of the CAM Location Mask Register act as a pointer indicating which byte of the 6-byte address will be accessed next. This pointer will increment every time a read or write cycle is done to the CAM entry. The pointer starts at 1, indicating the least significant byte of the address.

Four additional registers are provided to validate the shared 32 CAM entries and are referred to as Shared CAM Validation Register 1–4 (SCVR 1–4, Page 9H, Address 16–19H). Each bit of these registers is mapped to one CAM location. An address in the CAM location will only be valid when a corresponding bit Address Valid (ADV bit) has been set in this register. RIC II will include only valid CAM locations for address comparison.

The contents of all CAM locations are unknown at power up. This will pose no problem since the ADV (Address Valid) bit is not set for the CAM. Therefore the comparison will not take place with the CAM contents.

INTER-RIC BUS INTERFACE

Using the RIC II in a repeater system allows the design to be constructed with many network attachments than can be supported by a single chip. The split of functions already described allows data packets, and collision status to be transferred between multiple RIC IIs, and at the same time the multiple RIC IIs still behave as a single logical repeater. Since all RIC IIs in a repeater system are identical and capable of performing any of the repetition operations, the failure of one RIC II will not cause the failure of the entire system. This is an important issue in large multiport repeaters.

RIC IIs communicate via a specialized interface known as the Inter-RIC bus. This allows the data packet to be transferred from the receiving RIC II to the other RIC IIs in the system. These RIC IIs then transmit the data stream to their segments. The notification of collisions occurring across the network is just as important as data transfers. The Inter-RIC bus has a set of status lines capable of conveying collision information between RIC IIs to ensure their main state machines operate in the appropriate manner.

LED INTERFACE AND HUB MANAGEMENT FUNCTION

Repeater systems usually possess optical displays indicating network activity and the status of specific repeater operations. The RIC II's display update block provides the system designer with a wide variety of indicators. The display updates are completely autonomous and merely require SSI logic devices to drive the display devices, usually made up of light emitting diodes, LEDs. The status display is very flexible allowing the user to choose those indicators appropriate for the specification of the equipment.

5.0 Functional Description (Continued)

RIC II has been designed with special awareness for system designers implementing large repeaters possessing hub management capabilities. Hub management uses the unique position of repeaters in a network to gather statistics about the network segments they are attached to. The RIC II provides hub management statistical data in 3 steps. Important events are gathered by the management block from logic blocks throughout the chip. These events may then be stored in on-chip latches, or counted in on-chip counters according to user supplied latching and counting masks.

The fundamental task of a hub management system implementation is to associate the current packet and any management status information with the network segment, such as the repeater port where the packet was received. The ideal system would place this combined data packet and status field in system memory for examination by hub management software. The ultimate function of the RIC II's hub management support logic is to provide this function.

To accomplish this, the RIC II utilizes a dedicated hub management interface. This is similar to the Inter-RIC bus since it allows the data packet to be recovered from the receiving RIC II. Unlike the Inter-RIC bus, the intended recipient is not another RIC II, but National Semiconductor's DP83932 ''SONIC™'' Network controller or the DP83957 RIB. The use of a dedicated bus allows a management status field to be appended at the end of the data packet. This can be done without affecting the operation of the repeater system.

The RIC II adds 13 more (8-bit wide) counters in addition to counters provided on the RIC DP83950B. These counters will count events specified in the Event Count and Interrupt Mask Register2 (ECIMR2) such as Frame Check Sequence, Frame Alignment Error, Partition, and Out of Window Collision. This register also includes ''Reset On Read'' and ''Freeze When Full'' control bits.

It should be noted that Counter Decrement (CDEC) will not be used with the ECMR2. Also no real time or event logging interrupt, RTI or ELI, will be generated for this register.

PROCESSOR INTERFACE

The RIC II's processor interface allows connection to a system processor. Data transfer occurs via an octal bi-directional data bus. The RIC II has a number of on-chip registers indicating the status of the hub management functions, chip configuration and port status. These may be accessed by providing the chosen address at the Register Address (RA4–RA0) input pins.

Display update cycles and processor accesses occur utilizing the same data bus. An on-chip arbiter in the processor/display block schedules and controls the accesses and ensures the correct information is written into the display latches. During the display update cycles the RIC II behaves as a master of its data bus. This is the default state of the data bus. Consequently, a TRI-STATE buffer must be placed between the RIC II and the system processor's data bus. This ensures bus contention is avoided during simultaneous display update cycles and processor accesses of other devices on the system bus. When the processor accesses a RIC II register, the RIC II enables the data buffer and selects the operation, either input or output, of the data pins.

For faster register accesses, RIC II provides the added feature of disabling the display update cycles. In the Lower Event Information register (Page 1H, Address 1FH) setting the Disable LED Update bit, DLU, stops the RIC LED updates. This causes the data bus to be no longer shared, therefore, RIC II is always in a slave access mode. In this mode, the maximum read/write cycle time is reduced to approximately 400 ns.

5.3 DESCRIPTION OF REPEATER OPERATIONS

In order to implement a multi-chip repeater system which behaves as though it were a single logical repeater, special consideration must be paid to the data path used in packet repetition. For example, where in the data path are specific operations such as Manchester decoding and elasticity buffering performed. Also the system's state machines which utilize available network activity signals, must be able to accommodate the various packet repetition and collision scenarios detailed in the repeater specification.

The RIC II contains two types of inter-acting state machines. These are:

1. Port State Machines (PSMs). Every network attachment has its own PSM.
2. Main State Machine (MSM). This state machine controls the shared functional blocks as shown in the block diagram *Figure 4-1*.

REPEATER PORT AND MAIN STATE MACHINES

These two state machines are described in the following sections. Reference is made to expressions used in the IEEE Repeater specification. For the precise definition of these terms please refer to the specification. To avoid confusion with the RIC II's implementation, where references are made to repeater states or terms as described in the IEEE specification, these items are written in *italics*. The IEEE state diagram is shown in *Figure 5-2*, the Inter-RIC bus state diagram is shown in *Figure 5-1*.

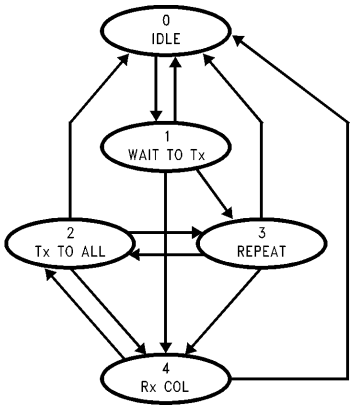

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FIGURE 5-1. Inter-RIC Bus State Diagram

5.0 Functional Description (Continued)

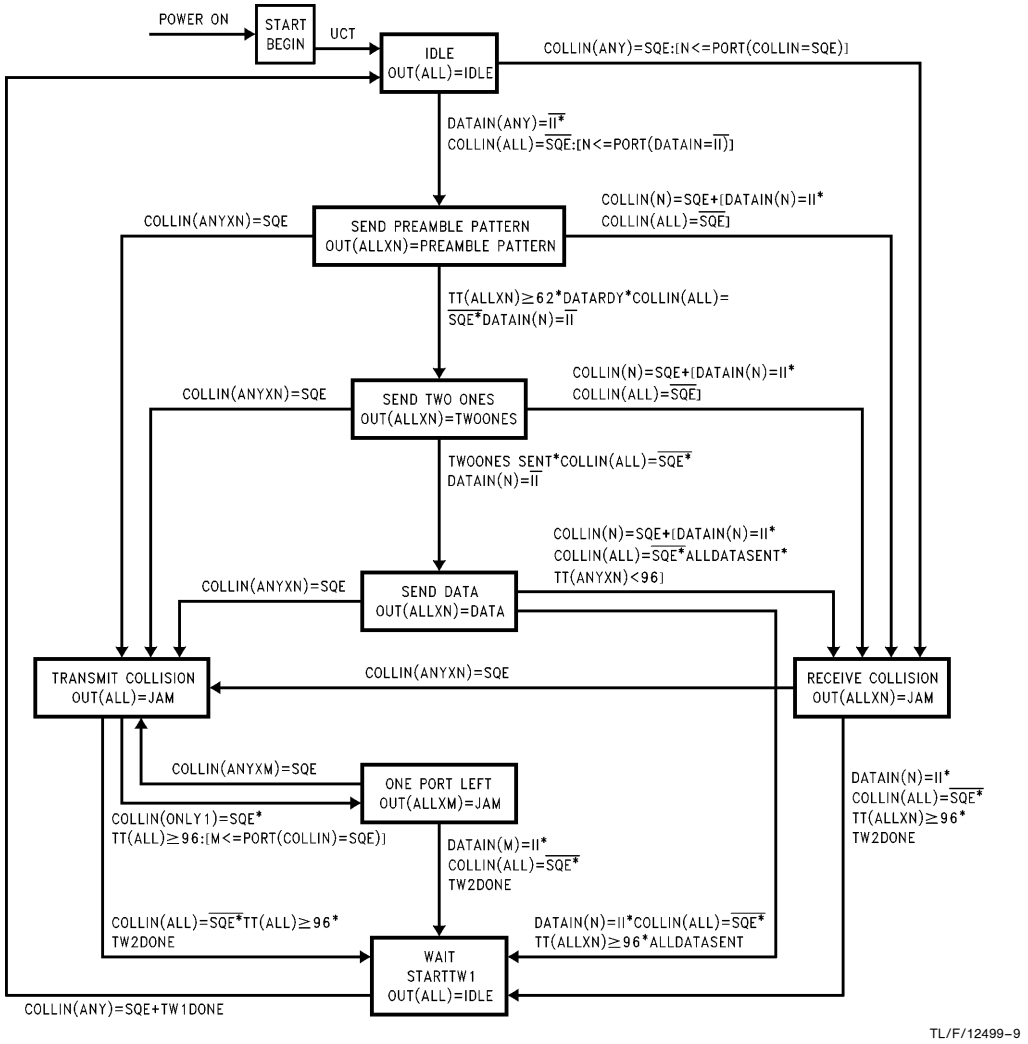

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FIGURE 5-2. IEEE Repeater Main State Diagram

5.0 Functional Description (Continued)

PORT STATE MACHINE (PSM)

There are two primary functions for the PSM as follows:

1. Control the transmission of repeated data, pseudo random data, and jam signals over the attached segment.
2. Decide whether a port will be the source of data or collision information which will be repeated over the network. This repeater port is known as *PORT N*. An arbitration process is required to enable the repeater to transition from the *IDLE* state to the *SEND PREAMBLE PATTERN* or *RECEIVE COLLISION* states, see *Figure 5-2*. This process is used to locate the port which will be *PORT N* for that particular packet. The data received from this port is directed to the PLL decoder and transmitted over the Inter-RIC bus. If the repeater enters the *TRANSMIT COLLISION* state a further arbitration operation is performed to determine which port is *PORT M*. *PORT M* is differentiated from the repeater's other ports if the repeater enters the *ONE PORT LEFT* state. In this state *PORT M* does not transmit to its segment; where as all other ports are still required to transmit to their segments.

MAIN STATE MACHINE (MSM)

The MSM controls the operation of the shared functional blocks in each RIC II as shown in the block diagram, *Figure 4-1*, and it performs the majority of the data and collision propagation operations as defined by the IEEE specification.

The interaction of the main and port state machines is visible, in part, by observing the Inter-RIC bus.

INTER-RIC BUS OPERATION

OVERVIEW

The Inter-RIC Bus consists of eight signals. These signals implement a protocol which may be used to connect multiple RIC IIs together. In this configuration, the logical function of a single repeater is maintained. The resulting multi-RIC II system is compliant to the IEEE 802.3 repeater specification and may connect several hundred network segments. An example of a multi-RIC II system is shown in *Figure 5-3*.

The Inter-RIC Bus connects multiple RIC IIs to realize the following operations:

Port N Identification (which port the repeater receives data from)
Port M Identification (which port is the last one experiencing a collision)
Data Transfer
RECEIVE COLLISION identification
TRANSMIT COLLISION identification
DISABLE OUTPUT (jabber protection)

Repeater Functions

Function	Action
Preamble Regeneration	Restore the length of the preamble pattern to the defined size.
Fragment Extension	Extend received data or collision fragments to meet the minimum fragment length of 96 bits.
Elasticity Buffer Control	A portion of the received packet may require storage in an Elasticity Buffer to accommodate preamble regeneration.
Jam/ Preamble Pattern Generation	In cases of receive or transmit collisions, a RIC II is required to transmit a jam pattern (1010 . . .). (Note)
Transmit Collision Enforcement	Once the *TRANSMIT COLLISION* state is entered a repeater is required to stay in this state for at least 96 network bit times.
Data Encoding Control	NRZ format data from the elasticity buffer must be encoded into Manchester format data prior to retransmission.
Tw1 Enforcement	Enforce the Transmit Recovery Time specification.
Tw2 Enforcement	Enforce Carrier Recovery Time specification on all ports with active collisions.

Note: This pattern is the same as that used for preamble regeneration.

5.0 Functional Description (Continued)

The following table briefly describes the operation of the Inter-RIC bus signals, the conditions required for a RIC II to assert a signal, and which RIC IIs (in a multi-RIC II system) would monitor the signal.

Inter-RIC Bus Signal	Function	Conditions Required for a RIC II to Drive This Signal	RIC II Receiving the Signal
$\overline{\text{ACKI}}$	Input signal to The PSM arbitration chain. This chain is employed to identify *PORT N* and *PORT M*. (Note 1)	Not applicable	This is dependent upon the method used to cascade RIC IIs, described in a following section.
$\overline{\text{ACKO}}$	Output signal from the PSM arbitration chain.	Not applicable	This is dependent upon the method used to cascade RIC IIs, described in a following section.
ACTN	This signal denotes there is activity on *PORT N* or *PORT M*.	A RIC II must contain *PORT N* or *PORT M*. (Note 2)	The signal is monitored by all RIC IIs in the repeater system.
ANYXN	This signal denotes that a repeater port that is not *PORT N* or *PORT M* is experiencing a collision.	Any RIC II which satisfies the above condition. (Note 3)	The signal is monitored by all RIC IIs in the repeater system.
COLN	Denotes *PORT N* or *PORT M* is experiencing a collision.	A RIC II must contain *PORT N* or *PORT M*. (Note 4)	The signal is monitored by all other RIC IIs in the repeater system.
IRE	This signal acts as an activity framing signal for the IRC and IRD signals.	A RIC II must contain *PORT N*.	The signal is monitored by all other RIC IIs in the repeater system.
IRD	Decoded serial data, in NRZ format, received from the network segment attached to *PORT N*.	A RIC II must contain *PORT N*.	The signal is monitored by all other RIC IIs in the repeater system.
IRC	Clock signal associated with IRD and IRE.	A RIC II must contain *PORT N*.	The signal is monitored by all other RIC IIs in the repeater system.

Note 1: A RIC II which contains *PORT N* or *PORT M* may be identified by its $\overline{\text{ACKO}}$ signal being low when its $\overline{\text{ACKI}}$ input is high.

Note 2: Although this signal normally has only one source asserting the signal active it is used in a wired-or configuration.

Note 3: This bus line is used in a wired-or configuration.

Note 4: Refer to the note for the transmit collision case.

5.0 Functional Description (Continued)

METHODS OF RIC II CASCADING

In order to build multi-RIC II repeaters, *PORT N* and *PORT M* identification must be performed across all the RIC IIs in the system. Inside each RIC II, the PSMs are arranged in a logical arbitration chain where port 1 is the highest and port 13 the lowest. The top of the chain, the input to port 1 is accessible to the user via the RIC II's $\overline{\text{ACKI}}$ input pin. The output from the bottom of the chain becomes the $\overline{\text{ACKO}}$ output pin. In a single RIC II system *PORT N* is defined as the highest port in the arbitration chain with receive or collision activity. *Port N* identification is performed when the repeater is in the *IDLE* state. *PORT M* is defined as the highest port in the chain with a collision when the repeater leaves the *TRANSMIT COLLISION* state. In order for the arbitration chain to function, all that needs to be done is to tie the $\overline{\text{ACKI}}$ signal to a logic high state. In multi-RIC II systems there are two methods to propagate the arbitration chain between RIC IIs:

The first and most straightforward is to extend the arbitration chain by daisy chaining the $\overline{\text{ACKI}}$-$\overline{\text{ACKO}}$ signals between RIC IIs. In this approach one RIC II is placed at the top of the chain (its $\overline{\text{ACKI}}$ input is tied high), then the $\overline{\text{ACKO}}$ signal from this RIC II is sent to the $\overline{\text{ACKI}}$ input of the next RIC II and so on. This arrangement is simple to implement but it places some topological restrictions upon the repeater system. In particular, if the repeater is constructed using a backplane with removable printed circuit boards. (These boards contain the RIC IIs and their associated components.) If one of the boards is removed then the $\overline{\text{ACKI}}$-$\overline{\text{ACKO}}$ chain will be broken and the repeater will not operate correctly.

The second method of *PORT N* or *M* identification avoids this problem. This second technique relies on an external parallel arbiter which monitors all of the RIC IIs' $\overline{\text{ACKO}}$ signals and responds to the RIC II with the highest priority. In this scheme each RIC II is assigned with a priority level. One method of doing this is to assign a priority number which reflects the position of a RIC II board on the repeater backplane, i.e., its slot number. When a RIC II experiences receive activity and the repeater system is in the *IDLE* state, the RIC II board will assert $\overline{\text{ACKO}}$. External arbitration logic drives the identification number onto an arbitration bus and the RIC II containing *PORT N* will be identified. An identical procedure is used in the *TRANSMIT COLLISION* state to identify *PORT M*. Parallel arbitration is not subject to the problems caused by missing boards, i.e., empty slots in the backplane. The logic associated with asserting this arbitration vector in the various packet repetition scenarios could be implemented in PAL® or GAL® type devices.

Both of the above methods employ the same signals: $\overline{\text{ACKI}}$, $\overline{\text{ACKO}}$ and $\overline{\text{ACTN}}$ to perform *PORT N* or *M* arbitration.

The Inter-RIC bus allows multi-RIC II operations to be performed in exactly the same manner as if there is only a single RIC II in the system. The simplest way to describe the operation of Inter-RIC bus is to see how it is used in a number of common packet repetition scenarios. Throughout this description the RIC IIs are presumed to be operating in external transceiver mode. This is advantageous for the explanation since the receive, transmit and collision signals from each network segment are observable. In internal transceiver mode this is not the case, since the collision signal for the non-AUI ports is derived by the transceivers inside the RIC II.

5.4 EXAMPLES OF PACKET REPETITION SCENARIOS

The operation of RIC II is described by the following examples of packet repetition scenarios.

DATA REPETITION OVERVIEW

When a packet is received at one port, RIC II checks the source, and destination addresses of the packet. The port configuration causes either a pseudo random bit sequence, or the received packet to be transmitted to different ports.

If there is a destination address mismatch (secure mode), then the RIC II will generate a random pattern on the first bit of the data field on the corresponding transmitting port. The data remains intact on the Inter-RIC bus so other cascaded repeaters could compare the destination address with their local CAMs.

On a valid source address mismatch (secure mode), RIC II shall switch to random pattern both on the local transmitting ports and the Inter-RIC bus.

COLLISION SCENARIOS OVERVIEW

The RIC II will adhere to all collision scenarios. When a collision occurs, RIC II will switch from a random pattern to a jam pattern to comply with IEEE repeater specifications.

If collision occurs during the preamble, then jam pattern is transmitted out by the repeater's ports.

In the case of a collision during the address field, the ''type field'', or the ''data field'', RIC II switches to the jam pattern immediately.

FIFO CONDITION OVERVIEW

Elasticity buffer error (ELBER) or FIFO overflow burst is another condition that could take place anytime during the packet transmission. The sequence of events for FIFO burst is the same as those for collision.

DATA REPETITION PROCESS

The first task to be performed is *PORT N* identification. This is an arbitration process performed by the Port State Machines in the system. In situations where two or more ports simultaneously receive packets, the Inter-RIC bus operates by choosing one of the active ports, and forcing the others to transmit data (real data or pseudo random data). This is done in accordance with the IEEE specification's allowed exit paths from the *IDLE* state, i.e., to the *SEND PREAMBLE PATTERN* or *RECEIVE COLLISION* states.

The packet begins with a preamble pattern derived from the RIC II's on-chip jam/preamble generator. The data received at *PORT N* is directed through the receive multiplexor to the PLL decoder. Once phase lock has been achieved, the decoded data (in NRZ format) with its associated clock and enable signals, is asserted onto the IRD, IRE, and IRC Inter-RIC bus lines respectively. This serial data stream is received from the bus by all RIC IIs in the repeater and directed to their Elasticity Buffers. Logic circuits monitor the data stream and look for the Start of Frame Delimiter (SFD). When this has been detected, data is loaded into the elasticity buffer for later transmission. This will occur when sufficient preamble has been transmitted and certain internal state machine operations have been fulfilled.

Figure 5-3 shows two RIC IIs A and B, daisy chained together with RIC II A positioned at the top of the chain. A packet is received at port B1 of RIC II B, and is then repeated by the other ports in the system (non-secure mode). *Figure 5-4*

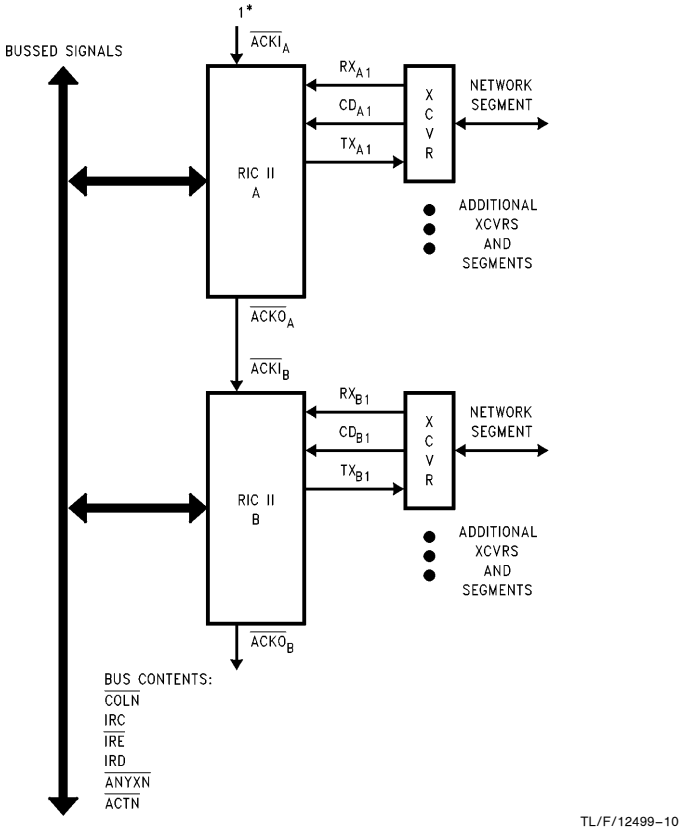
5.0 Functional Description (Continued)

shows the functional timing diagram for this packet repetition represented by the signals shown in *Figure 5-3*. In this example only two ports in the system are shown. In non-secure mode, the other ports also repeat the packet. It also indicates the operation of the RIC IIs' state machines in so far as can be seen by observing the Inter-RIC bus. For reference, the repeater's state transitions are shown in terms of the states defined by the IEEE specification. The location of *PORT N* is also shown. The following section describes the repeater and Inter-RIC bus transitions shown in *Figure 5-4*.

The repeater is stimulated into activity by the data signal received by port B1. The RIC IIs in the system are alerted to forthcoming repeater operation by the falling edges on the $\overline{\text{ACKI}}$ and $\overline{\text{ACKO}}$ daisy chain and the $\overline{\text{ACTN}}$ bus signal. Following a defined start up delay the repeater moves to the *SEND PREAMBLE* state. The RIC II system utilizes the start up delay to perform port arbitration. When packet transmission begins the RIC II system enters the REPEAT state. The expected, for normal packet repetition, sequence of repeater states, *SEND PREAMBLE, SEND SFD and SEND DATA* is followed, but is not visible upon the Inter-RIC bus. They are merged together into a single REPEAT state. This is also true for the *WAIT* and *IDLE* states, they appear as a combined Inter-RIC bus IDLE state.

Once a repeat operation has begun, i.e., the repeater leaves the *IDLE* state. It is required to transmit at least 96 bits of data or jam/preamble onto its network segments. If the duration of the received signal from *PORT N* is smaller than 96 bits, the repeater transitions to the *RECEIVE COLLISION* state (described later). This behavior is known as fragment extension.

After the packet data has been repeated, including the emptying of the RIC IIs' elasticity buffers, the RIC II performs the *Tw1* transmit recovery operation. This is performed during the *WAIT* state shown in the repeater state diagram.

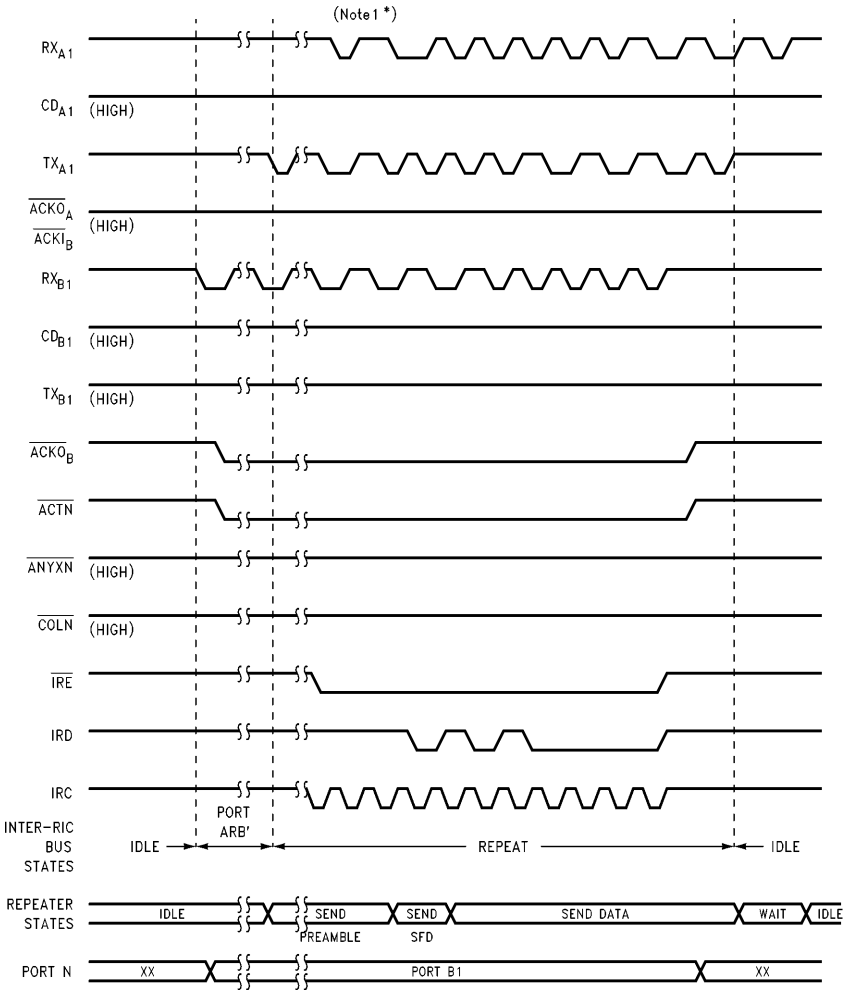


TL/F/12499–10

Note 1*: This input is tied at a logic high state.

FIGURE 5-3. RIC II System Topology

5.0 Functional Description (Continued)

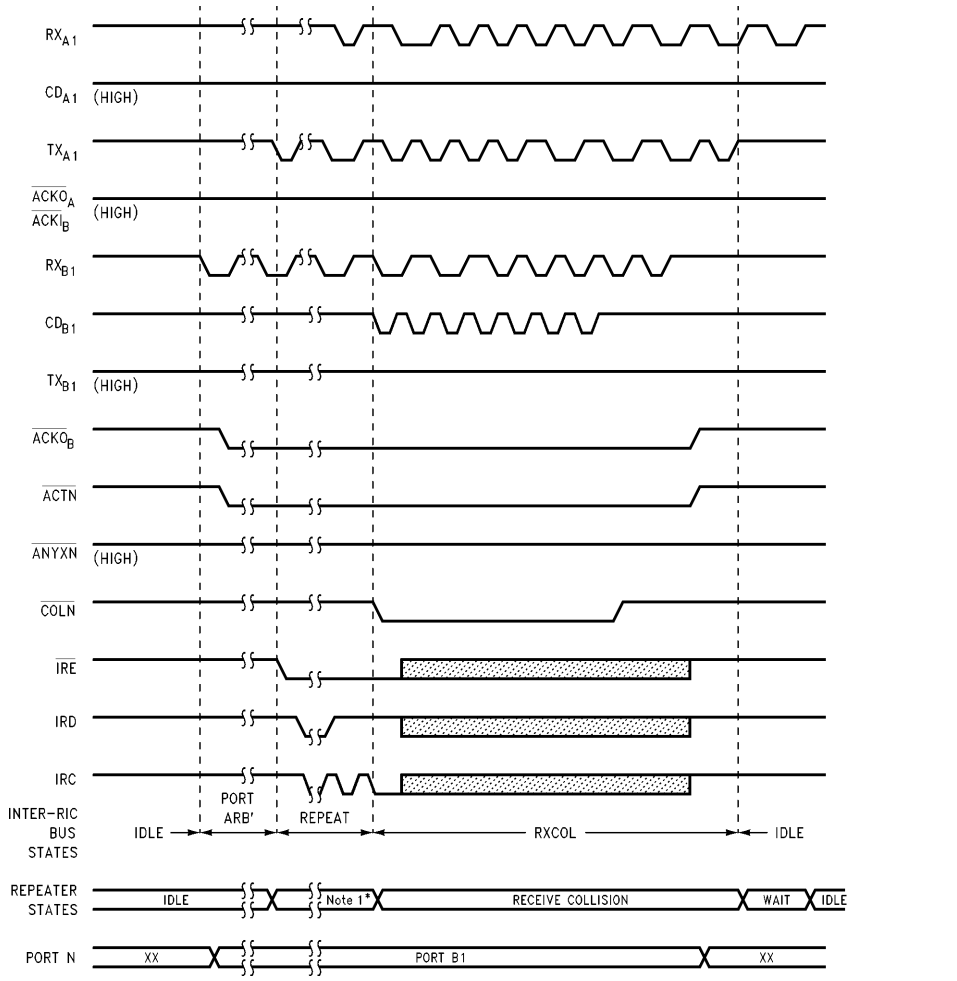


TL/F/12499–11

Note 1*: The activity shown on RX_{A1} represents the transmitted signal on TX_{A1} after being looped back by the attached transceiver.

FIGURE 5-4. Data Repetition

5.0 Functional Description (Continued)



TL/F/12499–12

Note 1*: *SEND PREAMBLE, SEND SFD, SEND DATA*

FIGURE 5-5. Receive Collision

5.0 Functional Description (Continued)

RECEIVE COLLISIONS

A receive collision is a collision which occurs on the network segment attached to *PORT N*, i.e., the collision is ''received'' in a similar manner as a data packet is received, and then repeated to the other network segments. Not surprisingly, the receive collision propagation follows a similar sequence of operations as data repetition.

An arbitration process is performed to find *PORT N* and a preamble/jam pattern is transmitted by the repeater's other ports. When *PORT N* detects a collision on its segment the $\overline{\text{COLN}}$ Inter-RIC bus signal is asserted. This forces all the RIC IIs in the system to transmit a preamble/jam pattern to their segments. This is important since they may be already transmitting data from their elasticity buffers. The repeater moves to the *RECEIVE COLLISION* state and begins to transmit the jam pattern. The repeater remains in this state until both the following conditions have been fulfilled:

1. at least 96 bits have been transmitted onto the network,
2. the activity has ended.

Under close examination, the repeater specification reveals that the actual end of activity has its own permutations of conditions:

1. collision and receive data signals may end simultaneously,
2. receive data may appear to end before collision signals,
3. receive data may continue for some time after the end of the collision signal.

Network segments using coaxial media may experience spurious gaps in segment activity when the collision signal goes inactive. This arises from the interaction between the receive and collision signal squelch circuits, implemented in coaxial transceivers, and the properties of the coaxial cable itself. The repeater specification avoids propagation of these activity gaps by extending collision activity by the *Tw2* wait time. Jam pattern transmission must be sustained throughout this period. After this, the repeater will move to the *WAIT* state unless there is a data signal being received by *PORT N*.

The functional timing diagram, *Figure 5-5*, shows the operation of a repeater system during a receive collision. The system configuration is the same as earlier described and is shown in *Figure 5-3*.

The RIC IIs perform the same *PORT N* arbitration and data repetition operations as previously described. The system is notified of the receive collision on port B1 by the $\overline{\text{COLN}}$ bus signal going active. This is the signal which informs the main state machines to output the jam pattern rather than the data held in the elasticity buffers. Once a collision has occurred the IRC, IRD and $\overline{\text{IRE}}$ bus signals may become undefined. When the collision has ended and the *Tw2* operation performed, the repeater moves to the *WAIT* state.

TRANSMIT COLLISIONS

A transmit collision is a collision that is detected upon a segment to which the repeater system is transmitting. The port state machine monitoring the colliding segment asserts the $\overline{\text{ANYXN}}$ bus signal. The assertion of $\overline{\text{ANYXN}}$ causes *PORT M* arbitration to begin. The repeater moves to the *TRANSMIT COLLISION* state when the port which had been *PORT N* starts to transmit a Manchester encoded 1 on to its network segment. While in the *TRANSMIT COLLISION* state, all ports of the repeater must transmit the 1010 . . . jam pattern, and *PORT M* arbitration is performed. Each RIC II is obliged, by the IEEE specification, to ensure all of its ports transmit for at least 96 bits once the *TRANSMIT COLLISION* state has been entered. This transmit activity is enforced by the $\overline{\text{ANYXN}}$ bus signal. While $\overline{\text{ANYXN}}$ is active, all RIC II ports will transmit jam. To ensure this situation lasts for at least 96 bits, the MSM inside the RIC IIs assert the $\overline{\text{ANYXN}}$ signal throughout this period. After this period has elapsed, $\overline{\text{ANYXN}}$ will only be asserted if there are multiple ports with active collisions on their network segments.

There are two possible ways for a repeater to leave the *TRANSMIT COLLISION* state. The most straightforward is when network activity, i.e., collisions and their *Tw2* extensions, end before the 96-bit enforced period expires. Under these conditions the repeater system may move directly to the *WAIT* state when 96 bits have been transmitted to all ports. If the MSM enforced period ends and there is still one port experiencing a collision, the *ONE PORT LEFT* state is entered. This may be seen on the Inter-RIC bus when $\overline{\text{ANYXN}}$ is de-asserted and PORT M stops transmitting to its network segment. In this circumstance the Inter-RIC bus transitions to the *RECEIVE COLLISION* state. The repeater will remain in this state while *PORT M*'s collision, *Tw2* collision extension and any receive signals are present. When these conditions are not true, packet repetition finishes and the repeater enters the *WAIT* state.

Figure 5-6 shows a multi-RIC II system operating under transmit collision conditions. There are many different scenarios which may occur during a transmit collision, this figure illustrates one of these. The diagram begins with packet reception by port A1. Port B1 experiences a collision, since it is not *PORT N* it asserts $\overline{\text{ANYXN}}$. This alerts the main state machines in the system to switch from data to jam pattern transmission.

Port A1 is also monitoring the $\overline{\text{ANYXN}}$ bus line. Its assertion forces A1 to relinquish its *PORT N* status, start transmitting, stop asserting $\overline{\text{ACTN}}$ and release its hold on the PSM arbitration signals ($\overline{\text{ACKO}}$ A and $\overline{\text{ACKI}}$ B). The first bit it transmits will be a Manchester encoded ''1'' in the jam pattern. Since port B1 is the only port with a collision, it attains *PORT M* status and stops asserting $\overline{\text{ANYXN}}$. It does however assert $\overline{\text{ACTN}}$, and exert its presence upon the PSM arbitration chain (forces $\overline{\text{ACKO}}$ B low). The MSMs ensure that $\overline{\text{ANYXN}}$ stays active and thus force all of the ports, including *PORT M*, to transmit to their segments.

After some time port A1 experiences a collision. This arises from the presence of the packet being received from port A1's segment and the jam signal the repeater is now transmitting onto this segment. Two packets on one segment results in a collision. *PORT M* now moves from B1 to A1. Port A1 fulfills the same criteria as B1, i.e., it has an active collision on its segment, but in addition it is higher in the arbitration chain. This priority yields no benefits for port A1 since the $\overline{\text{ANYXN}}$ signal is still active. There are now two sources driving $\overline{\text{ANYXN}}$, the MSMs and the collision on port B1.

5.0 Functional Description (Continued)

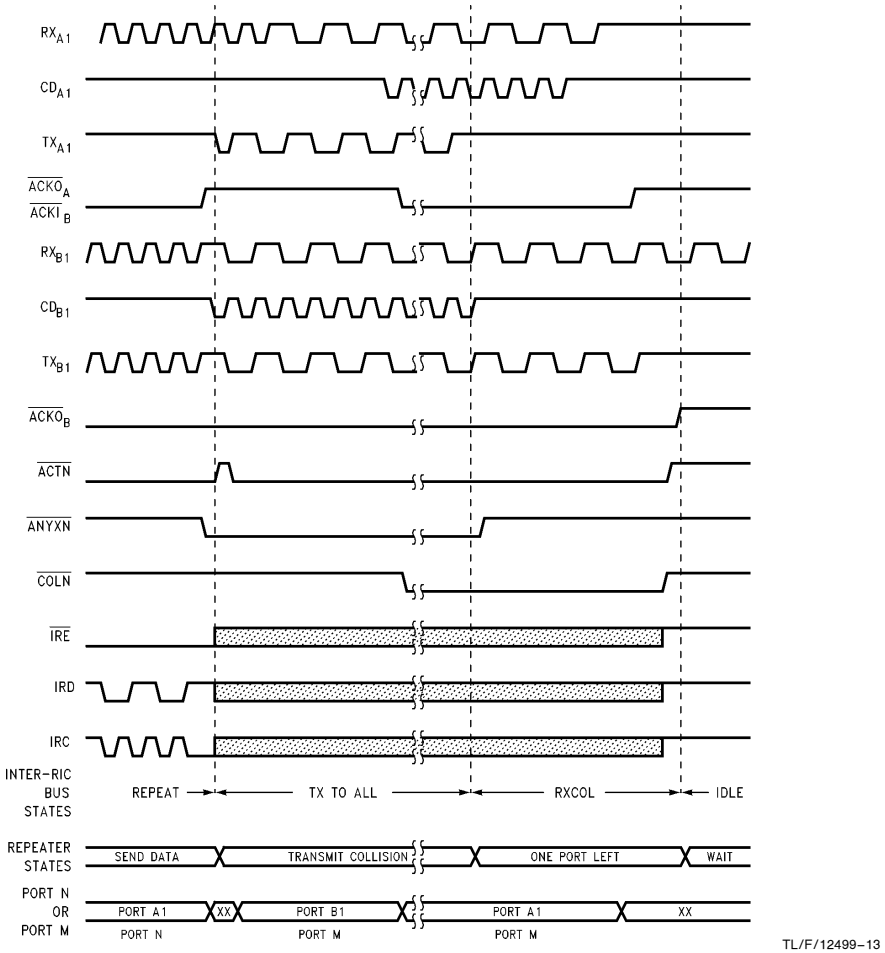
Eventually the collision on port B1 ends and the $\overline{\text{ANYXN}}$ extension by the MSMs expires. There is only one collision on the network (this may be deduced since $\overline{\text{ANYXN}}$ is inactive) so the repeater will move to the *ONE PORT LEFT* state. The RIC II system treats this state in a similar manner to a receive collision with *PORT M* fulfilling the role of the receiving port. The difference from a true receive collision is that the switch from packet data to the jam pattern has already been made (controlled by $\overline{\text{ANYXN}}$). Thus the state of $\overline{\text{COLN}}$ has no effect upon repeater operations. In common with the operation of the *RECEIVE COLLISION* state, the repeater remains in this condition until the collision and receive activity on *PORT M* subside. The packet repetition operation completes when the *Tw1* recovery time in the *WAIT* state has been performed.

Note: In transmit collision conditions $\overline{\text{COLN}}$ will only go active if the RIC II which contained *PORT N* at the start of packet repetition contains *PORT M* during the *TRANSMIT COLLISION* and *ONE PORT LEFT* states.

JABBER PROTECTION

A repeater is required to disable transmit activity if the length of its current transmission reaches the jabber protect limit. This is defined by the specification's *Tw3* time. The repeater disables output for a time period defined by the *Tw4* specification, after this period normal operation may resume.

Figure 5-7 shows the effect of a jabber length packet upon a RIC II based repeater system. The **JABBER PROTECT** state is entered from the *SEND DATA* state. While the *Tw4* period is observed the Inter-RIC bus displays the IDLE state. This is misleading since new packet activity or continuous activity (as shown in the diagram) does not result in packet repetition. This may only occur when the *Tw4* requirement has been satisfied.



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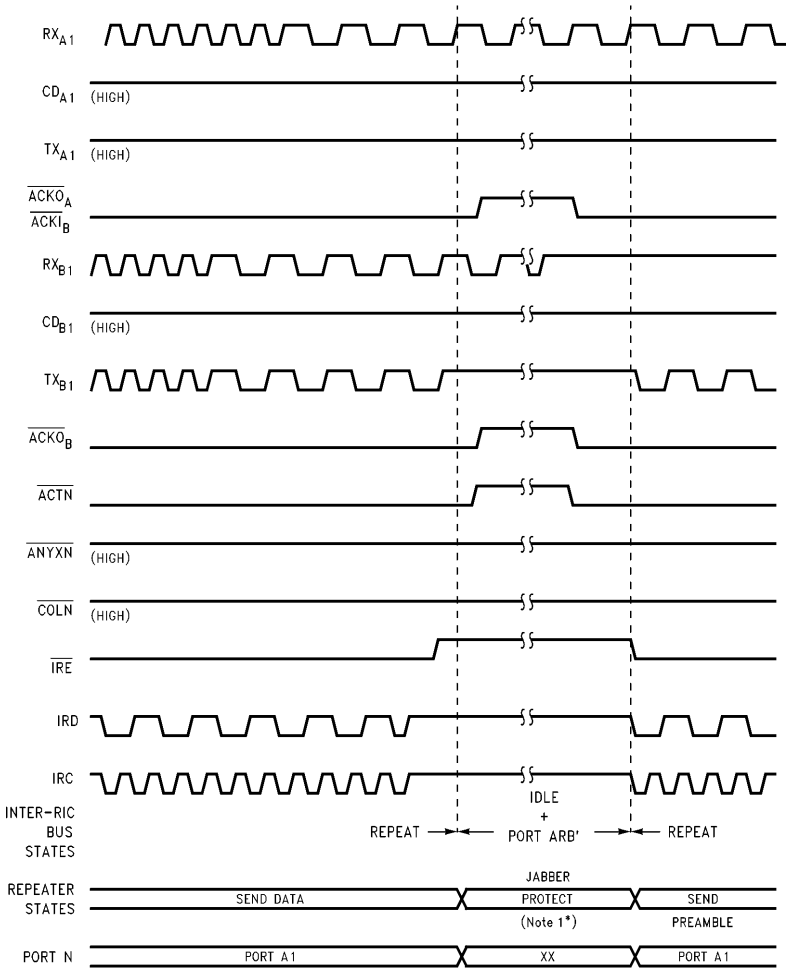
Note: The Inter-RIC bus is configured to use active low signals.

FIGURE 5-6. Transmit Collision

5.0 Functional Description (Continued)



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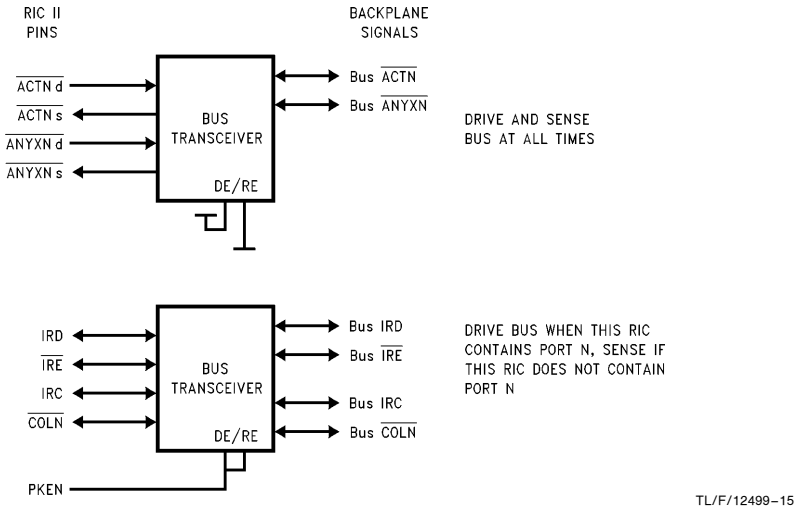
Note 1*: The IEEE Specification does not have a jabber protect state defined in its main state diagram, this behavior is defined in an additional MAU Jabber Lockup Protection state diagram.

Note: The Inter-RIC bus is configured to use active low signals.

FIGURE 5-7. Jabber Protect

5.0 Functional Description (Continued)



Note: DE = Bus Drive Enable active high, $\overline{RE}$ = Bus Receive Enable active low

Note: The Inter-RIC bus is configured to use active low signals.

FIGURE 5-8. External Bus Transceiver Connection Diagram

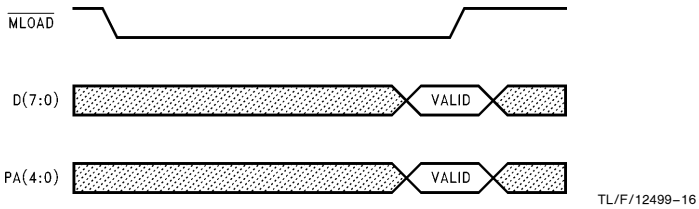


FIGURE 5-9. Mode Load Operation

5.0 Functional Description (Continued)

5.5 DESCRIPTION OF HARDWARE CONNECTION FOR INTER-RIC BUS

When considering the hardware interface, the Inter-RIC bus may be viewed as consisting of three groups of signals:

1. Port Arbitration chain, namely: $\overline{ACKI}$ and $\overline{ACKO}$.
2. Simultaneous drive and sense signals, i.e., $\overline{ACTN}$ and $\overline{ANYXN}$. (Potentially these signals may be driven by multiple devices.)
3. Drive or sense signals, i.e., $\overline{IRE}$, IRD, IRC and $\overline{COLN}$. (Only one device asserts these signals at any instance in time.)

The first set of signals are either used as point to point links, or with external arbitration logic. In both cases the load on these signals will not be large, so the on-chip drivers are adequate. This may not be true for signal classes (2) and (3).

The Inter-RIC bus has been designed to connect RIC IIs together directly, or via external bus transceivers. The latter is advantageous in large repeaters. In the second application the backplane is often heavily loaded and is beyond the drive capabilities of the on-chip bus drivers. The need for simultaneous sense and drive capabilities on the $\overline{ACTN}$ and $\overline{ANYXN}$ signals, and the desire to allow operation with external bus transceivers, makes it necessary for these bus signals to each have a pair of pins on the RIC II. One driving the bus, the other sensing the bus signal. When external bus transceivers are used, they must be open collector/open drain to allow wire-ORing of the signals. Additionally, the drive and sense enables of the bus transceiver should be tied in the active state.

The uni-directional nature of information transfer on the $\overline{IRE}$, IRD, IRC and $\overline{COLN}$ signals, means a RIC II is either driving these signals or receiving them from the bus, but not both at the same time. Thus a single bi-directional input/output pin is adequate for each of these signals. If an external bus transceiver is used with these signals the Packet Enable ''PKEN'' RIC II output pin performs the function of a drive enable and sense disable.

Figure 5-8 shows the RIC II connected to the Inter-RIC bus via external bus transceivers, such as National's DS3893A bus transceivers.

Some bus transceivers are of the inverting type. To allow the Inter-RIC bus to utilize these transceivers, the RIC II may be configured to invert the active states of the $\overline{ACTN}$, $\overline{ANYXN}$, $\overline{COLN}$ and $\overline{IRE}$ signals. Instead of being active low they are active high. Thus they become active low once more when passed through an inverting bus driver. This is particularly important for the $\overline{ACTN}$ and $\overline{ANYXN}$ bus lines, since these signals must be used in a wired-or configuration. Incorrect signal polarity would make the bus unusable.

5.6 PROCESSOR AND DISPLAY INTERFACE

The processor interface pins, which include the data bus, address bus and control signals, actually perform three operations which are multiplexed on these pins. These operations are:

1. The Mode Load Operation, which performs a power up initialization cycle upon the RIC II.
2. Display Update Cycles, which are refresh operations for updating the display LEDs.
3. Processor Access Cycles, which allows μP's to communicate with the RIC II's registers.

These three operations are described below.

MODE LOAD OPERATION

The Mode Load Operation is a hardware initialization procedure performed at power on. It loads vital device configuration information into on-chip configuration registers. In addition to its configuration function, the $\overline{MLOAD}$ pin is the RIC II's reset input. When $\overline{MLOAD}$ is low all of the RIC II's repeater timers, state machines, segment partition logic and hub management logic are reset.

The Mode Load Operation may be accomplished by attaching the appropriate set of pull up and pull down resistors to the data and register address pins to assert logic high or low signals onto these pins, and then providing a rising edge on the $\overline{MLOAD}$ pin as is shown in *Figure 5-9*. The mapping of chip functions to the configuration inputs is shown in Table 5-1. Such an arrangement may be performed using a simple resistor, capacitor, diode network. Performing the Mode Load Operation in this way enables the configuration of a RIC II that is in a simple repeater system (one without a processor).

Alternatively in a complex repeater system, the Mode Load Operation may be performed using a processor write cycle. This would require the $\overline{MLOAD}$ pin be connected to the CPU's write strobe via some decoding logic, and included in the processor's memory map.

To support the security options, pin D0 of MLOAD is assigned to configure RIC II during mode load operation. A pull up (non-security mode) or a pull down (security mode) on this pin defines the desired security level. By using this bit, the user could also take advantage of the learning mode, as described below.

LEARNING OF PORT SOURCE ADDRESS(ES)

Learning mode could be invoked in two ways according to bit D0 of MLOAD configuration. Only the port CAMs are capable of learning the addresses:

1. When D0 = 0, upon power up and by default, LME, SME, ESA and EDA bits in the Port Security Configuration Register (PSCR) are set globally. This means that each port will learn the address of the node connected to it by the reception of the first good packet. The second address is learned only if it is different than the first one. Only the address of a packet with correct CRC can be learned. As soon as the address is learned by any of the two CAM locations, RIC II will set the corresponding ADV (Address Valid) bit in Port CAM Pointer Register.

   To start the address comparison, the SAC (Start Comparison) bit must be set (SAC = 1) by the user. RIC II will only use this CAM location for comparison when the ADV bit is set (ADV = 1), whether LME is 1 or 0. These four bits in PSCR could be disabled later on a per port basis, which allow all the packets regardless of their address to pass through the repeater.
2. When D0 = 1 for MLOAD, security could still be done, but this time it means that the user should set the LME, SME, ESA and/or EDA bits in the Port Security Configuration Register. The rest of the operation is same as when D0 is equal to zero.

5.0 Functional Description (Continued)

It is important to note that RIC II will learn the address of the packet if LME is set regardless of the D0 setting of MLOAD, i.e. secure or non-secure mode.

It is also very important to note that for proper address learning, LME and SAC should not be set together.

When the repeater is in non-secure mode, then the comparison will not take place between the incoming address and the learned address.

When the repeater is in secure mode, and the LME bit is set, then the processor read/write access will be ignored for the port CAM entries. That is read/write cycles are completed, however unknown values are read during the learning process. Data will not be written into the CAM entries until the end of the learning process.

It may be desired not to randomize the outgoing data and transmit the data intact when there is a valid source address mismatch. The Generate Random Pattern bit, GRP in the Global Security Register, will provide the option.

If GRP is set (GRP = 1) and there is a source address mismatch, then RIC II will not generate random pattern; the packet will be transmitted out and the Hub Manager will be informed about the source address mismatch.

For this option to work properly, GRP = ESA = 1 and EDA = 0. If EDA is also set to 1, then the packet will be randomized on ports with valid DA mismatches, and this functionality will not work.

TABLE 5-1. Pin Definitions for Options in the Mode Load Operation

Pin Name	Programming Function	Effect When Bit is 0	Effect When Bit is 1	Function
D0	$\overline{\text{SCRTY}}$	Security Mode	Non-Security Mode	This bit configures RIC II security feature options. When D0 = 0 LME, SME, ESA, EDA bits in the Port Security Configuration Register (PSCR) are set globally. When D0 = 1 security can still be done, but now the user needs to set the above bits in the PSCR register.
D1	TW2	5 Bits	3 Bits	This allows the user to select one of two values for the repeater specification TW2 time. The lower limit (3 bits) meets the IEEE. specification. The upper limit (5 bits) is not specification compliant but may provide users with higher network throughput by avoiding spurious network activity gaps when using coaxial (10BASE2, 10BASE5) network segments.
D2	$\overline{\text{CCLIM}}$	63	31	The partition specification requires a port to be partitioned after a certain number of consecutive collisions. The RIC II has two values available to allow users to customize the partitioning algorithm to their environment. Please refer to the Partition State Machine, in data sheet Section 7.3.
D3	$\overline{\text{LPPART}}$	Selected	Not Selected	The RIC II may be configured to partition a port if the segment transceiver does not loopback data to the port when the port is transmitting to it, as described in the Partition State Machine.
D4	$\overline{\text{OWCE}}$	Selected	Not Selected	This configuration bit allows the on-chip partition algorithm to include out of window collisions into the collisions it monitors, as described in the Partition State Machine.
D5	$\overline{\text{TXONLY}}$	Selected	Not Selected	This configuration bit allows the on-chip partition algorithm to restrict segment reconnection, as described in the Partition State Machine.
D6	$\overline{\text{DPART}}$	Selected	Not Selected	The Partition state machines for all ports may be disabled by writing a logic zero to this bit during the mode load operation.
D7	MIN/MAX	Minimum Mode	Maximum Mode	The operation of the display update block is controlled by the value of this configuration bit, as described in the Display Update Cycles section.

TABLE 5-1. Pin Definitions for Options in the Mode Load Operation (Continued)

<table>
<tr><th>Pin Name</th><th>Programming Function</th><th>Effect When Bit is 0</th><th>Effect When Bit is 1</th><th>Function</th></tr>
<tr><td>RA0
RA1</td><td>BYPAS1
BYPAS2</td><td></td><td></td><td>These configuration bits select which of the repeater ports (numbers 2 to 13) are configured to use the on-chip internal 10BASE-T transceivers or the external transceiver interface. The external transceiver interface operates using AUI compatible signal levels.

<table><tr><th>BYPAS2</th><th>BYPAS1</th><th>Information</th></tr><tr><td>0</td><td>0</td><td>All ports (2 to 13) use the external Transceiver Interface.</td></tr><tr><td>0</td><td>1</td><td>Ports 2 to 5 use the external interface, 6 to 13 use the internal 10BASE-T transceivers.</td></tr><tr><td>1</td><td>0</td><td>Ports 2 to 7 use the external interface, 8 to 13 use the internal 10BASE-T transceivers.</td></tr><tr><td>1</td><td>1</td><td>All ports (2 to 13) use the internal 10BASE-T transceivers.</td></tr></table></td></tr>
<tr><td>RA2</td><td>BINV</td><td>Active High Signals</td><td>Active Low Signals</td><td>This selection determines whether the Inter-RIC signals: IRE, ACTN, ANYXN, COLN and Management bus signal MCRS are active high or low.</td></tr>
<tr><td>RA3</td><td>EXPLL</td><td>External PLL</td><td>Internal PLL</td><td>If desired, the RIC II may be used with an external decoder, this configuration bit performs the selection.</td></tr>
<tr><td>RA4</td><td>resv</td><td>Not Permitted</td><td>Required</td><td>To ensure correct device operation, this bit must be written with a logic one during the mode load operation.</td></tr>
</table>

5.0 Functional Description (Continued)

5.7 DESCRIPTION OF HARDWARE CONNECTION FOR PROCESSOR AND DISPLAY INTERFACE

DISPLAY UPDATE CYCLES

The RIC II possesses control logic and interface pins which may be used to provide status information concerning activity on the attached network segments and the current status of repeater functions. These status cycles are completely autonomous and require only simple support circuitry to produce the data in a form suitable for a light emitting diode ''LED'' display. The display may be used in one of two modes:

1. Minimum mode—General Repeater Status LEDs,

2. Maximum mode—Individual Port Status LEDs.

Minimum mode, intended for simple LED displays, makes available four status indicators. The first LED denotes whether the RIC II has been forced to activate its jabber protect functions. The remaining 3 LEDs indicate if any of the RIC II's network segments are: (1) experiencing a collision, (2) receiving data, (3) currently partitioned. When minimum display mode is selected the only external components required are a 74LS374 type latch, the LEDs and their current limiting resistors.

Maximum mode differs from minimum mode by providing display information specific to individual network segments. This information denotes the collision activity, packet reception and partition status of each segment. In the case of 10BASE-T segments the link integrity status and polarity of the received data are also made available. The wide variety of information available in maximum mode may be used in its entirety or in part. Thus allowing the system designer to choose the appropriate complexity of status display commensurate with the specification of the end equipment.

The signals provided and their timing relationships have been designed to interface directly with 74LS259 type addressable latches. The number of latches used being dependent upon the complexity of the display. Since the latches are octal, a pair of latches is needed to display each type of segment specific data (13 ports means 13 latch bits). The accompanying tables (5-2 and 5-3) show the function of the interface pins in minimum and maximum modes. *Figure 5-11* shows the location of each port's status information when maximum mode is selected. This may be compared with the connection diagram *Figure 5-10*.

Immediately following the Mode Load Operation (when the $\overline{\text{MLOAD}}$ pin transitions to a high logic state), the display logic performs an LED test operation. This operation lasts one second. While it is in effect, all of the utilized LEDs will blink on. Thus, an installation engineer is able to test the operation of the display by forcing the RIC II into a reset cycle ($\overline{\text{MLOAD}}$ forced low). The rising edge on the $\overline{\text{MLOAD}}$ pin starts the LED test cycle. **During the LED test cycle the RIC II does not perform packet repetition operations**.

The status display possesses a capability to lengthen the time an LED is active. At the end of the repetition of a packet, the display is frozen showing the current activity. This freezing lasts for 30 ms or until a subsequent packet is repeated. Thus at low levels of packet activity, the display stretches activity information to make it discernible to the human eye. At high traffic rates the relative brightness of the LEDs indicates those segments with high or low activity.

It should be mentioned that when the Real Time Interrupt (RTI) occurs, the display update cycle will stop and after RTI is serviced, the display update cycle will resume activity.

5.0 Functional Description (Continued)

TABLE 5-2. Status Display Pin Functions in Minimum Mode

Signal Pin Name	Function in Minimum Mode
D0	No operation
D1	Provides status information indicating if there is a collision occurring on one of the segments attached to this RIC II.
D2	Provides status information indicating if one of this RIC II's ports is receiving a data or collision packet from a segment attached to this RIC II.
D3	Provides status information indicating that the RIC II has experienced a jabber protect condition.
D4	Provides Status information indicating if one of the RIC II's segments is partitioned.
D(7:5)	No operation.
$\overline{STR0}$	This signal is the latch enable for the 374 type latch.
$\overline{STR1}$	This signal is held at a logic one.

TABLE 5-3. Status Display Pin Functions in Maximum Mode

Signal Pin Name	Function in Maximum Mode
D0	Provides status information concerning the Link Integrity status of 10BASE-T segments. This signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D1	Provides status information indicating if there is a collision occurring on one of the segments attached to this RIC II. This signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D2	Provides status information indicating if one of this RIC II's ports is receiving a data or a collision packet from its segment . This signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D3	Provides Status information indicating that the RIC II has experienced a jabber protect condition. Additionally it denotes which of its ports are partitioned. This signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D4	Provides status information indicating if one of this RIC II's ports is receiving data of inverse polarity. This status output is only valid if the port is configured to use its internal 10BASE-T transceiver. The signal should be connected to the data inputs of the chosen pair of 74LS259 latches.
D(7:5)	These signals provide the repeater port address corresponding to the data available on D(4:0).
$\overline{STR0}$	This signal is the latch enable for the lower byte latches, that is the 74LS259s which display information concerning ports 1 to 7.
$\overline{STR1}$	This signal is the latch enable for the upper byte latches, that is the 74LS259s which display information concerning ports 8 to 13.

5.0 Functional Description (Continued)

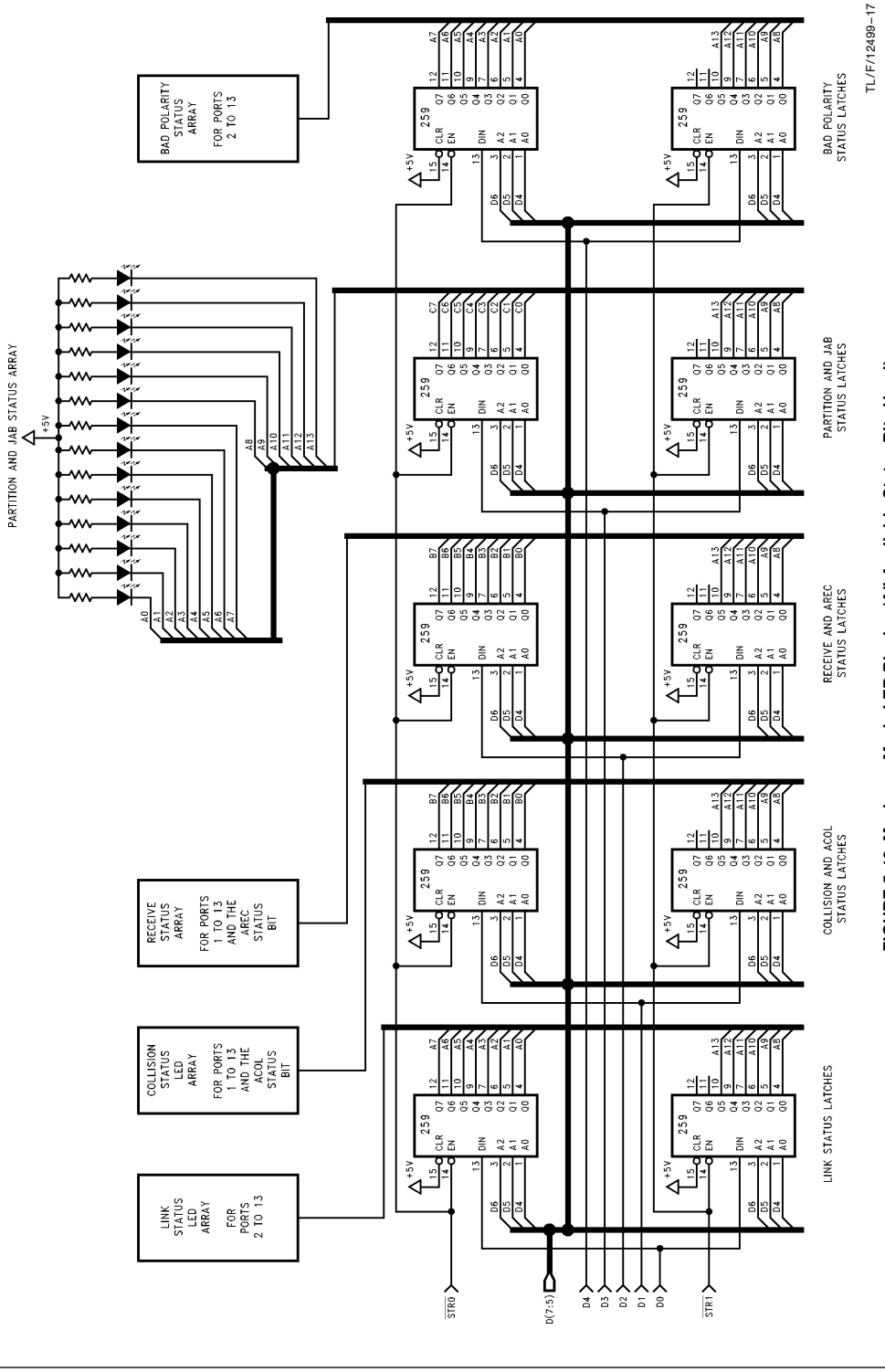


FIGURE 5-10. Maximum Mode LED Display (All Available Status Bits Used)

5.0 Functional Description (Continued)

74LS259 Latch Inputs = $\overline{\text{STR0}}$

259 Output	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
259 Addr S2–0	000	001	010	011	100	101	110	111
RIC II Port Number		1 (AUI)	2	3	4	5	6	7
RIC II D0 259 # 1			LINK	LINK	LINK	LINK	LINK	LINK
RIC II D1 259 # 2	ACOL	COL	COL	COL	COL	COL	COL	COL
RIC II D2 259 # 3	AREC	REC	REC	REC	REC	REC	REC	REC
RIC II D3 259 # 4	JAB	PART	PART	PART	PART	PART	PART	PART
RIC II D4 259 # 5			BDPOL	BDPOL	BDPOL	BDPOL	BDPOL	BDPOL

74LS259 (or Equiv.) Latch Inputs = $\overline{\text{STR1}}$

259 Outputs	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
259 Addr S2–0	000	001	010	011	100	101	110	111
RIC II Port Number	8	9	10	11	12	13		
RIC II D0 259 # 6	LINK	LINK	LINK	LINK	LINK	LINK		
RIC II D1 259 # 7	COL	COL	COL	COL	COL	COL		
RIC II D2 259 # 8	REC	REC	REC	REC	REC	REC		
RIC II D3 259 # 9	PART	PART	PART	PART	PART	PART		
RIC II D4 259 # 10	BDPOL	BDPOL	BDPOL	BDPOL	BDPOL	BDPOL		

This shows the LED Output Functions for the LED Drivers when 74LS259s are used. The top table refers to the bank of 4 74LS259s latched with $\overline{\text{STR0}}$, and the lower table refers to the bank of 4 74LS259s latched with $\overline{\text{STR1}}$. (For example the RIC II's D0 data signal goes to 259 #1 and #5. These two 74LS259s then drive the LINK LEDs.)

Note: ACOL = Any Port Collision, AREC = Any Port Reception, JAB = Any Port Jabbering, LINK = Port Link, COL = Port Collision, REC = Port Reception, PART = Port Partitioned, BDPOL = Bad (inverse) Polarity of received data.

FIGURE 5-11. Maximum Mode LED Definitions

5.0 Functional Description (Continued)

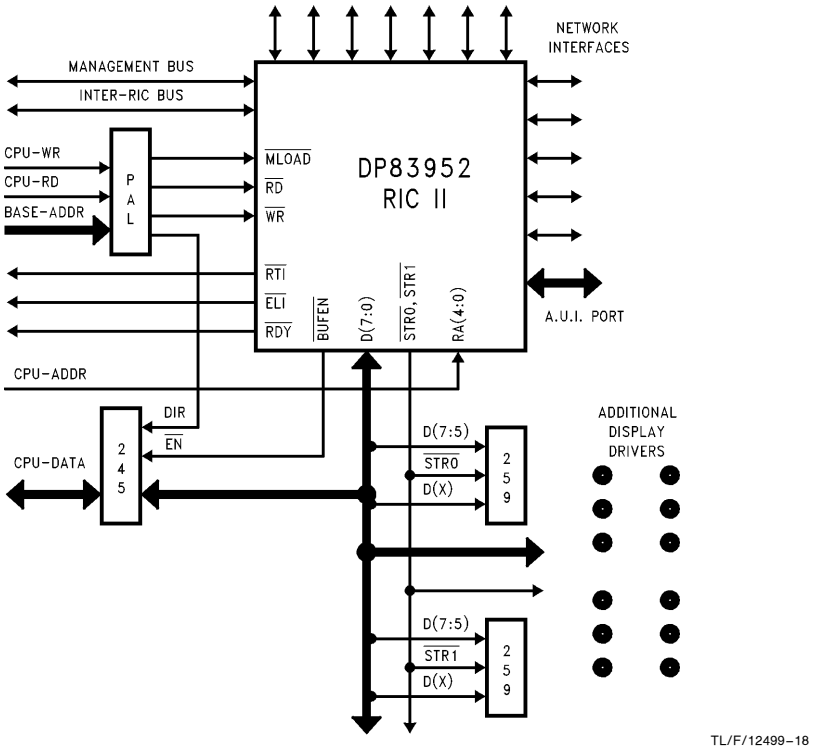


FIGURE 5-12. Processor Connection Diagram

5.0 Functional Description (Continued)

PROCESSOR ACCESS CYCLES

Access to the RIC II's on-chip registers is made via its processor interface. This utilizes conventional non-multiplexed address (5-bit) and data (8-bit) busses. The data bus is also used to provide data and address information to off-chip display latches during display update cycles. While performing these cycles, the RIC II behaves as a master of its data bus. Consequently a TRI-STATE bi-directional bus transceiver, e.g., 74LS245 must be placed between the RIC II and any processor bus.

RIC II provides the following scheme to facilitate faster register accesses. Lower Event Information Register (Page 1H, Address 1FH) has Disable LED Update bit, DLU, which when it is set, then RIC II stops the LED updates. This causes the data bus to be no longer shared, and therefore RIC II is always in a slave access mode. In this mode, the maximum read/write cycle time is reduced to approximately 400 ns.

The processor requests a register access by asserting the read "$\overline{RD}$" or write "$\overline{WR}$" input strobes. The RIC II responds by finishing any current display update cycle and asserts the TRI-STATE buffer enable signal "$\overline{BUFEN}$". If the processor cycle is a write cycle then the RIC II's data buffers are disabled to prevent contention. In order to interface to the RIC II in a processor controlled system it is likely a PAL device will be used to perform the following operations:

1. locate the RIC II in the processor's memory map (address decode),
2. generate the RIC II's read and write strobes,
3. control the direction signal for the 74LS245.

An example of the processor and display interfaces is shown in *Figure 5-12*.

INTERRUPT HANDLING

The DP83952 RIC II offers an alternate method for a faster access to determine the source of the Event Logging Interrupt (ELI) then the DP83950 RIC.

For an event logging interrupt due to flag found, the **DP83950 RIC** requires the following scheme:

1. Read the Page Select Register (Address 10H) to locate the source of Event Logging Interrupt.
2. Read all the Port Event Recording Registers (Page 1H, Address 11H to 1DH) to find the port and the event responsible for Event Logging Interrupt.

DP83952 RIC II allows the following alternate scheme for a faster access:

1. Read Page Select Register (Address 10H) to locate the source of Event Logging Interrupt.
2. Read the Event Information Registers (Page 1H, addresses 1EH and 1FH) to locate the port responsible for interrupt.
3. Read the Event Recording register of that port to find which specific event caused the Event Logging Interrupt.

6.0 Hub Management Support

The RIC II provides information regarding the status of its ports and the packets it is repeating. This data is available in three forms:

1. Counted Events—Network events accumulated into the RIC II's 16-bit Event Counter Registers.
2. Recorded Events—Network events that set bits in the Event Record Registers.
3. Hub Management Status packets—This is information sent over the Management Bus in a serial function to be decoded by an Ethernet Controller board.

The counted and recorded event information is available through the processor interface. This data is port specific and may be used to generate interrupts via the Event Logging Interrupt "$\overline{ELI}$" pin. Since the information is specific to each port, each repeater port has its own event record register and event counter. The counters and event record registers have user definable masks which enable them to be configured to count and record a variety of events. The counters and record registers are designed to be used together, so that detailed information, i.e., a count value can be held on-chip for a specific network condition. More general information, i.e. the occurrence of certain types of events may be retained in on-chip latches. Thus, the user can configure the counters to increment upon a rapidly occurring event (most likely to be used to count collisions), and the record registers may log the occurrence of less frequent error conditions such as jabber protect packets.

6.1 EVENT COUNTING FUNCTION

The counters may increment upon the occurrence of one of the categories of event as described below.

Potential sources for Counter increment:

Jabber Protection (JAB): The port counter increments if the length of a received packet from its associated port, causes the repeater state machine to enter the jabber protect state.

Elasticity Buffer Error (ELBER): The port counter increments if a Elasticity Buffer underflow or overflow occurs during packet reception. The flag is held inactive if a collision occurs during packet reception or if a phase lock error, described below, has already occurred during the repetition of the packet.

Phase Lock Error (PLER): A phase lock error is caused if the phase lock loop decoder looses lock during packet reception. Phase lock onto the received data stream may or may not be recovered later in the packet, and data errors may have occurred. This flag is held inactive if a collision occurs.

Non-SFD Packet (NSFD): If a packet is received, and the start of frame delimiter is not found, the port counter will increment. Counting is inhibited if the packet suffers a collision.

Out of Window Collision (OWC): The out of window collision flag for a port goes active when a collision is experienced outside of the network slot time.

Transmit Collision (TXCOL): The transmit collision flag for a port is enabled when a transmit collision is experienced by the repeater. Each port experiencing a collision under these conditions is said to have suffered a transmit collision.

6.0 Hub Management Support (Continued)

Receive Collision (RXCOL): The receive collision flag for a port goes active when the port is the receive source of network activity and suffers a collision, provided no other network segments experience collisions then the receive collision flag for the receiving port will be set.

Partition (PART): The port counter increments when a port becomes partitioned.

Bad Link (BDLNK): The port counter increments when a port is configured for 10BASE-T operation has entered the link lost state.

Short Event reception (SE): The port counter increments if the received packet is less than 74 bits long and no collision occurs during reception.

Packet Reception (REC): When a packet is received the port counter increments .

In order to utilize the counters the user must choose, from the above list, the desired statistic for counting. This counter mask information must be written to the appropriate, Event Count Mask Register. There are two of these registers, the Upper and Lower Event Count Mask registers. For the exact bit patterns of these registers please see Section 8 of the data sheet.

For example if the counters are configured to count network collisions and the appropriate masks have been set, then whenever a collision occurs on a segment, this information is latched by the hub management support logic. At the end of repetition of the packet the collision status, respective to each port, is loaded into that port's counter. This operation is completely autonomous and requires no processor intervention.

Each counter is 16 bits long and may be directly read by the processor. Additionally each counter has a number of decodes to indicate the current value of the count. There are three decodes:

low count (a value of 00FF Hex and under),
high count (a value of C000 Hex and above),
full count (a value of FFFF Hex).

The decodes from each counter are logically ''ORed'' together and may be used as interrupt sources for the $\overline{ELI}$ interrupt pin. Additionally the status of these bits may be observed by reading the Page Select Register (PSR), (see Section 8 for register details). In order to enable any of these threshold interrupts, the appropriate interrupt mask bit must be written to the Management and Interrupt Configuration Register; see Section 8 for register details.

In addition to their event masking functions, the Upper Event Counting Mask Register (UECMR) possesses two bits which control the operation of the counters. When written to a logic one, the reset on read bit ''ROR'' resets the counter after a processor read cycle is performed. If this operation is not selected, then in order to zero the counters, they must either be written with zeros by the processor, or allowed to roll over to all zeros. The freeze when full bit ''FWF'' prevents counter roll over by inhibiting count up cycles (these happen when chosen events occur), thus freezing the particular counter at FFFF Hex.

The port event counters may also be controlled by the Counter Decrement ($\overline{CDEC}$) pin. As its name suggests, a logic low state on this pin will decrement all the counters by a single value. The pulses on $\overline{CDEC}$ are internally synchronized and scheduled so as not to conflict with any ''up counting'' activity. If an up count and a down count occur simultaneously, then the down count is delayed until the up count has completed. This combination of up and down counting capability enables the RIC II's on-chip counters to provide a simple rolling average, or be used as extensions of larger off-chip counters.

Note: If the FWF option is enabled then the count down operation is disabled from those registers which have reached FFFF Hex and consequently have been frozen. Thus, if FWF is set and $\overline{CDEC}$ has been employed to provide a rate indication. A frozen counter indicates that a rate has been detected which has gone out of bounds, i.e., too fast increment or too slow increment. If the low count and high count decodes are employed as either interrupt sources or in a polling cycle, the direction of the rate excursion may be determined.

NEW HUB MANAGEMENT COUNTERS

The RIC II adds 13 more 8-bit counters then provided on the DP83950 RIC. These counters will count events specified in the Event Count and Interrupt Mask Register 2 (ECIMR2), such as Frame Check Sequence, Frame Alignment Error, Partition, Out of Window Collision. This register also includes ''Reset On Read'' and ''Freeze When Full'' control bits.

It should be noted that Counter Decrement (CDEC) will not be used with the ECMR2. Also no real time or event logging interrupt, RTI or ELI, will be generated for this register.

READING THE EVENT COUNTERS

The RIC II's external data bus is eight bits wide, since the event counters are 16 bits long, two processor read cycles are required to yield the counter value. In order to ensure that the read value is correct, and to allow simultaneous event counts with processor accesses, a temporary holding register is employed. A read cycle to either the lower or upper byte of a counter, causes both bytes to be latched into the holding register. Thus, when the other byte of the counter is obtained, the holding register is accessed, and, not the actual counter register. This ensures that the upper and lower bytes contain the value sampled at the same instance in time, i.e., when the first read cycle to that counter occurred.

There is no restriction concerning whether the upper or lower byte is read first. However to ensure the ''same instance value'' is obtained, the reads of the upper then lower byte (or vice versa) should be performed as consecutive reads of the counter array. Other NON-COUNTER registers may be read in between these read cycles and also write cycles may be performed. If another counter is read, or the same byte of the original counter is read again, then the holding register is updated from the counter array, and the unread byte is lost.

If the reset on read option is employed, then the counter is reset after the transfer to the holding register is performed. Processor read and write cycles are scheduled in such a manner that they do not conflict with count up or count down operations. That is to say, in the case of a processor read, the count value is stable when it is loaded into the holding register. In the case of a processor write, the newly written value is stable so it may be incremented or decremented by any subsequent count operation. During the period the $\overline{MLOAD}$ pin is low, (power on reset) all counters are

6.0 Hub Management Support (Continued)

reset to zero and all count masks are forced into the disabled state. Section 8 of the data sheet details the address location of the port event counters.

6.2 EVENT RECORD FUNCTION

As previously stated each repeater port has its own Event Recording Register. This is an 8-bit status register. Each bit is dedicated to logging the occurrence of a particular event (see Section 8 for detailed description). The logging of these events is controlled by the Event Recording Mask Register, for an event to be recorded the particular mask bit must be set, (see Section 8 description of this register). Similar to the scheme employed for the event counters, the recorded events are latched during the repetition of a packet, and then automatically loaded into the recording registers at the end of transmission of a packet. When one of the unmasked events occurs, the particular port register bit is set. This status is visible to the user. All of the register bits for all of the ports are logically ''ORed'' together to produce a Flag Found ''FF'' signal. This indicator may be found by reading the Page Select Register. Additionally, an interrupt may be generated if the appropriate mask bit is enabled in the Management and Interrupt Configuration Register.

A processor read cycle to an Event Record Register resets any of the bits set in that register. Read operations are scheduled to guarantee non-changing data during a read cycle. Any internal bit setting event which immediately follows a processor read will be successful. The events which may be recorded are described below:

Jabber Protection (JAB): This flag goes active if the length of a received packet from the relevant port, causes the repeater state machine to enter the Jabber Protect state.

Elasticity Buffer Error (ELBER): This condition occurs if an Elasticity Buffer full or overflow occurs during packet reception. The flag is held inactive if a collision occurs during packet reception or if a phase lock error has already occurred during the repetition of the packet.

Phase Lock Error (PLER): A phase lock error is caused if the phase lock loop decoder loses lock during packet reception. Phase lock onto the received data stream may or may not be recovered later in the packet and data errors may have occurred. This flag is held inactive if a collision occurs.

Non-SFD Packet (NSFD): If a packet is received and the start of frame delimiter is not found, the flag will go active. The flag is held inactive if a collision occurs during packet repetition.

Out of Window Collision (OWC): The out of window collision flag for a port goes active when a collision is experienced outside of the network slot time.

Partition (PART): This flag goes active when a port becomes partitioned.

Bad Link (BDLNK): The flag goes active when a port is configured for 10BASE-T operation has entered the link lost state.

Short Event reception (SE): This flag goes active if the received packet is less than 74 bits long and no collision occurs during reception.

6.3 MANAGEMENT INTERFACE OPERATION

The Hub Management interface provides a mechanism to combine repeater status information with packet information to form a hub management status packet. The interface, a serial bus consisting of carrier sense, received clock and received data, is designed to connect one or multiple RIC II's over a backplane bus to a DP83932 ''SONIC'' network controller or DP83957 RIB. The SONIC/RIB and the RIC IIs form a powerful entity for network statistics gathering.

The interface consists of four pins:

MRXC	Management Receive Clock—10 MHz NRZ Clock output.
$\overline{\text{MCRS}}$	Management Carrier Sense—Input/Output indicating of valid data stream.
MRXD	Management Receive Data—NRZ Data output synchronous to MRXC.
$\overline{\text{PCOMP}}$	Packet Compress—Input to truncate the packet's data field.

The first three signals mimic the interface between an Ethernet controller and a phase locked loop decoder (specifically the DP83932 SONIC and DP83910 SNI), these signals are driven by the RIC II receiving the packet. MRXC and MRXD compose an NRZ serial data stream compatible with the DP83932. The $\overline{\text{PCOMP}}$ signal is driven by logic on the processor board. The actual data stream transferred over MRXD is derived from data transferred over the IRD Inter-RIC bus line. These two data streams differ in two important characteristics:

1. At the end of packet repetition a hub management status field is appended to the data stream. This status field, consisting of 7 bytes, is shown in *Figures 6-1* and *6-2*. The information field is obtained from a number of packet status registers described below. In common with the 802.3 protocol the least significant bit of a byte is transmitted first.
2. While the data field of the repeated packet is being transferred over the management bus, received clock signals on the MRXC pin may be inhibited. This operation is under the control of the Packet Compress pin $\overline{\text{PCOMP}}$. If $\overline{\text{PCOMP}}$ is asserted during repetition of the packet then MRXC signals are inhibited when the number of bytes (after SFD) transferred over the management bus equals the number indicated in the Packet Compress Decode Register. This register provides a means to delay the effect of the $\overline{\text{PCOMP}}$ signal, which may be generated early in the packet's repetition, until the desired moment. Packet compression may be used to reduce the amount of memory required to buffer packets when they are received and are waiting to be processed by hub management software. In this kind of application an address decoder, which forms part of the packet compress logic, would monitor the address fields as they are received over the management bus. If the destination address is not the address of the management node inside the hub, then packet compression could be employed. In this manner only the portion of the packet meaningful for hub management interrogation, i.e., the address fields, is transferred to the SONIC and is buffered in memory.

6.0 Hub Management Support (Continued)

If the repeated packet ends before $\overline{PCOMP}$ is asserted or before the required number of bytes have been transferred, then the hub management status field is directly appended to the received data at a byte boundary. If the repeated packet is significantly longer than the value in the Decode Register requires, and $\overline{PCOMP}$ is asserted, the status fields will be delayed until the end of packet repetition. During this delay period MRXC clocks are inhibited, but the MCRS signal remains asserted.

Note: If $\overline{PCOMP}$ is asserted late in the packet, i.e., after the number of bytes defined by the packet compression register, then packet compression will not occur.

The Management Interface may be fine tuned to meet the timing considerations of the SONIC and the access time of its associated packet memory. This refinement may be performed in two ways:

1. The default mode of operation of the Management interface is to only transfer packets over the bus which have a start of frame delimiter. Thus ''packets'' that are only preamble/jam and do not convey any source or destination address information are inhibited. This filtering may be disabled by writing a logic zero to the Management Interface Configuration or ''MIFCON'' bit in the Management and Interrupt Configuration Register. See Section 8 for details.
2. The Management bus has been designed to accommodate situations of maximum network utilization, for example when collision generated fragments occur (these collision fragments may violate the IEEE802.3 IFG specification). The IFG required by the SONIC is a function of the time taken to release space in the receive FIFO and to perform end of packet processing (write status information into memory). These functions are primarily memory operations and consequently depend upon the bus latency and the memory access time of the system. In order to allow the system designer some discretion in choosing the speed of this memory, the RIC II may be configured to protect the SONIC from a potential FIFO overflow. This is performed by utilizing the Inter Frame Gap Threshold Select Register.

   The value held in this register, plus one, defines, in network bit times, the minimum allowed gap between frames on the management bus. If the gap is smaller than this number then $\overline{MCRS}$ is asserted but MRXC clocks are inhibited. Consequently no data transfer is performed.

   Thus the system designer may make the decision whether to gather statistics on all packets even if they occur with very small IFGs or to monitor a subset.

The status field, shown in *Figure 6-1*, contains information of six different types. They are contained in seven Packet Status Registers ''PSRs'':

1. The RIC II and port address fields [PSR(0) and (1)] can uniquely identify the repeater port receiving the packet out of a potential maximum of 832 ports sharing the same management bus (64 RIC IIs each with 13 ports). Thus all of the other status fields can be correctly attributed to the relevant port.
2. The status flags the RIC II produces for the event counters or recording latches are supplied with each packet [PSR(2)]. Additionally the clean receive CLN status is supplied to allow the user to determine the reliability of the address fields in the packet. The CLN status bit [PSR(1)] is set if no collisions are experienced during the repetition of the address fields.
3. The RIC II has an on-chip timer to indicate when, relative to the start of packet repetition, a collision, if any, occurred [PSR(3)]. There is also a timer which indicates how many bit times of IFG was seen on the network between repetition of this packet and the preceding one. This is provided by [PSR(6)].
4. If packet compression is employed, the receive byte count contained in the SONIC's packet descriptor will indicate the number of bytes transferred over the management bus rather than the number of bytes in the packet. For this reason the RIC II which receives the packet, counts the number of received bytes and transfers this over the management bus [PSR(4),(5)].
5. Appending a status field to a data packet will obviously result in a CRC error being flagged by the SONIC. For this reason the RIC II monitors the repeated data stream to check for CRC and FAE errors. In the case of FAE errors the RIC II provides additional dummy data bits, so that the status fields are always byte aligned.
6. As a final check upon the effectiveness of the management interface, the RIC II transfers a bus specific status bit to the SONIC. This flag Packet Compress Done PCOMPD [PSR(0)], may be monitored by hub management software to check if the packet compression operation is enabled.

Figure 6-3 shows an example of a packet being transmitted over the management bus. The first section of the diagram (moving from left to right) shows a short preamble and SFD pattern. The second region contains the packet's address and the start of the data fields. During this time logic on the processor/SONIC card would determine if packet compression should be used on this packet. The $\overline{PCOMP}$ signal is asserted and packet transfer stops when the number of bytes transmitted equals the value defined in the decode register. Hence the MRXC signal is idle for the remainder of the packet's data and CRC fields. The final region shows the transfer of the RIC II's seven bytes of packet status.

The following pages describe these Hub Management registers which constitute the management status field.

Note that Packet Status Register 5 (PSR5) can be configured to remain identical in the RIC II as in the RIC, or PSR5 can be modified to include the RUNT and SAM (source address mismatch) information. PSR5 register bit allocation is determined by the value of bit D2, MPS (Modify Packet Status), in the Global Security Register. When the MPS bit is set, PSR5 register is modified.

6.0 Hub Management Support (Continued)

Packet Status Register (PSR) (Note 1)		D7	D6	D5	D4	D3	D2	D1	D0
PSR(0)		A5	A4	A3	A2	A1	A0	PCOMPD	resv
PSR(1)		CRCER	FAE	COL	CLN	PA3	PA2	PA1	PA0
PSR(2)		SE	OWC	NSFD	PLER	ELBER	JAB	CBT9	CBT8
PSR(3) Collision Bit Timer		CBT7	CBT6	CBT5	CBT4	CBT3	CBT2	CBT1	CBT0
PSR(4) Lower Repeat Byte Count		RBY7	RBY6	RBY5	RBY4	RBY3	RBY2	RBY1	RBY0
PSR(5) Upper Repeat Byte Count	MPS = 0 (Note 2)	RBY15	RBY14	RBY13	RBY12	RBY11	RBY10	RBY9	RBY8
	MPS = 1	res	res	res	SAM	RUNT	RBY10	RBY9	RBY9
PSR(6) Inter Frame Gap Bit Timer		IBT7	IBT6	IBT5	IBT4	IBT3	IBT2	IBT1	IBT0

Note 1: These registers may only be reliably accessed via the management interface. Due to the nature of these registers they may not be accessed (read or write cycles) via the processor interface.

Note 2: When MPS (Modify Packet Status) bit in the Global Security Register is:

MPS = 0, Do not modify Packet Status Register 5. The RIC II PSR5 is the same as the RIC PSR5.

MPS = 1, The PSR5 register is modified in the RIC II.

FIGURE 6-1. Hub Management Status Field

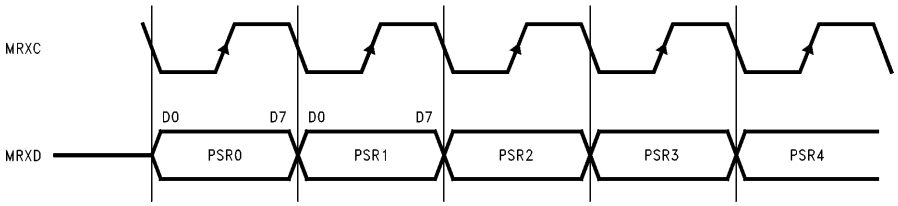


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FIGURE 6-2. Management Bus Packet Status Register Timing

6.0 Hub Management Support (Continued)

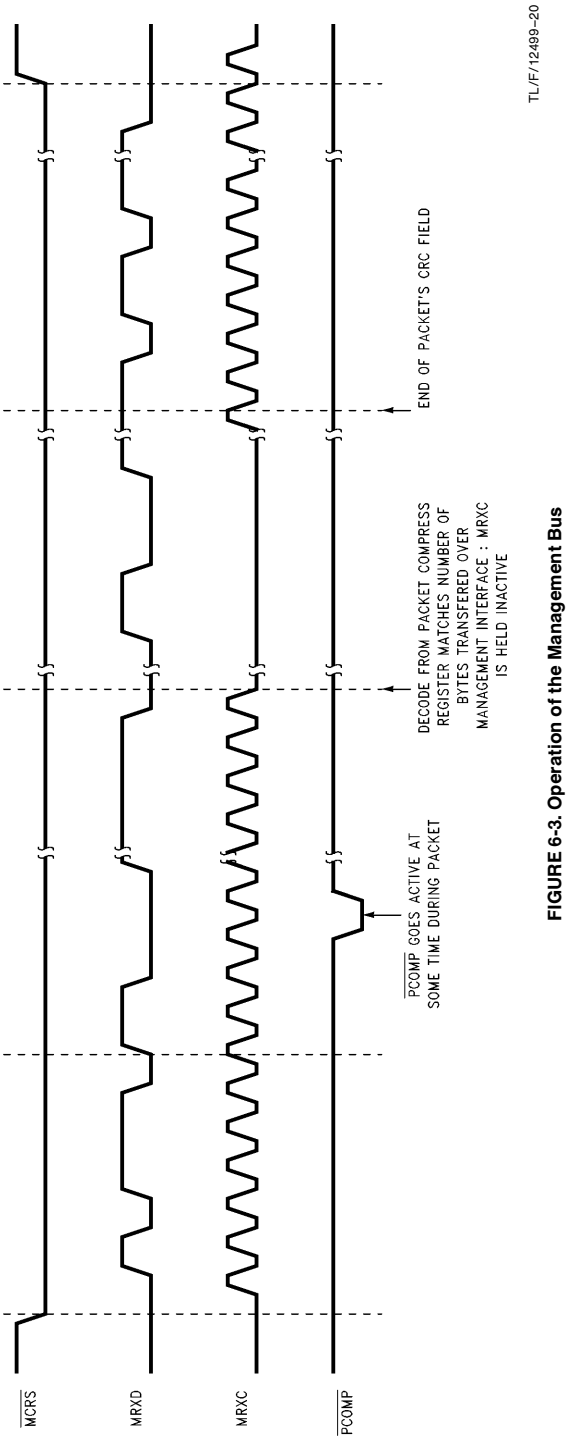


FIGURE 6-3. Operation of the Management Bus

6.0 Hub Management Support (Continued)

PACKET STATUS REGISTER 0

D7	D6	D5	D4	D3	D2	D1	D0
A5	A4	A3	A2	A1	A0	PCOMPD	resv

Bit	Symbol	Description
D0	resv	**RESERVED FOR FUTURE USE:** This bit is currently undefined management software should not examine the state of this bit.
D1	PCOMPD	**PACKET COMPRESSION DONE:** If packet compression is utilized, this bit informs the user that compression was performed, i.e., the packet was long enough to require compression.
D(7:2)	A(5:0)	**RIC II ADDRESS (5:0):** This address is defined by the user and is supplied when writing to the RIC II Address Register. It is used by hub management software to distinguish between RIC IIs in a multi-RIC II system.

PACKET STATUS REGISTER 1

D7	D6	D5	D4	D3	D2	D1	D0
CRCER	FAE	COL	CLN	PA3	PA2	PA1	PA0

Bit	Symbol	Description
D(3:0)	PA(3:0)	**PORT ADDRESS:** This field defines the port which is receiving the packet.
D4	CLN	**CLEAN RECEIVE:** This bit is asserted provided no collision activity occurs during repetition of the source and destination address fields, and the packet is of sufficient size to contain these fields.
D5	COL	**COLLISION:** If a receive or transmit collision occurs during packet repetition the collision bit is asserted.
D6	FAE	**FRAME ALIGNMENT ERROR:** This bit is asserted if a Frame Alignment Error occurred in the repeated packet.
D7	CRER	**CRC ERROR:** This bit is asserted if a CRC Error occurred in the repeated packet. This status flag should not be tested if the COL bit is asserted since the error may be simply due to the collision.

PACKET STATUS REGISTER 2

D7	D6	D5	D4	D3	D2	D1	D0
SE	OWC	NSFD	PLER	ELBER	JAB	CBT9	CBT8

Bit	Symbol	Description
D(1:0)	CT(9:8)	**COLLISION TIMER BITS 9 AND 8:** These two bits are the upper bits of the collision bit timer.
D2	JAB	**JABBER EVENT:** This bit indicates that the receive packet was so long the repeater was forced to go into a jabber protect condition.
D3	ELBER	**ELASTICITY BUFFER ERROR:** During the packet an Elasticity Buffer under/overflow occurred.
D4	CRER	**CARRIER ERROR EVENT:** The packet suffered sufficient jitter/noise corruption to cause the phase lock loop decoder to loose lock.
D5	NSFD	**NON-SFD:** The repeated packet did not contain a Start of Frame Delimiter. When this bit is set the Repeat Byte Counter counts the length of the entire packet. When this bit is not set the byte counter only counts post SFD bytes. (Note)
D6	OWC	**OUT OF WINDOW COLLISION:** The packet suffered an out of window collision.
D7	SE	**SHORT EVENT:** The received activity was so small it met the criteria to be classed as a short event.

Note: The operation of this bit is not inhibited by the occurrence of a collision during packet repetition (see description of the Repeat Byte Counter below).

6.0 Hub Management Support (Continued)

MODIFIED PACKET STATUS REGISTER 5 (MPS = 1 IN GSR REGISTER)

RIC II provides an option for a new Packet Status Register 5 (PSR5) field. On the seven bytes of management status field, PSR5 has been modified to indicate the source address mismatch information (SAM bit) for security purposes.

By using this option, the maximum received byte count changes to 2048 (2^{11}). As soon as the counter reaches this number, it will freeze, instead of rolling over and starting again on the reception of the next packet.

A RUNT bit has also been added to this register indicating whether the last packet received by a port was RUNT. (A packet is RUNT when its length is greater than or equal to Short Event and less than or equal to 64 bytes from SFD.)

The other registers comprise the remainder of the collision timer register [PSR(3)], the Repeat Byte Count registers [PSR(4) and PSR(5)], and the Inter Frame Gap Counter ''IFG'' register [PSR(6)].

COLLISION BIT TIMER

The Collision Timer counts in bit times the time between the start of repetition of the packet and the detection of the packet's first collision. The Collision counter increments as the packet is repeated and freezes when a collision occurs. The value in the counter is only valid when the collision bit ''COL'' in [PSR(1)] is set.

REPEAT BYTE COUNTER

The Repeat Byte Counter is a 16-bit counter which can perform two functions. In cases where the transmitted packet possesses an SFD, the byte counter counts the number of received bytes after the SFD field. Alternatively, if no SFD is repeated, the counter reflects the length of the packet (counted in bytes) starting at the beginning of the preamble field. When performing the latter function, the counter is shortened to 7 bits when MPS = 0 in the GSR register. Thus, the maximum count value is 127 bytes. The counter is shortened to 11 bits when MPS = 1 in the GSR register. In this configuration, the maximum received byte count changes to 2048 bytes. The mode of counting is indicated by the ''NSFD'' bit in [PSR(2)]. In order to check if the received packet was genuinely a Non-SFD packet, the status of the COL bit should be checked. During collisions SFD fields may be lost or created, Management software should be robust to this kind of behavior.

INTER FRAME GAP (IFG) BIT TIMER

The IFG counter counts in bit times the period in between repeater transmissions. The IFG counter increments whenever the RIC II is not transmitting a packet. If the IFG is long, i.e., greater than 255 bits the counter sticks at this value. Thus an apparent count value of 255 should be interpreted as 255 or more bit times.

6.4 DESCRIPTION OF HARDWARE CONNECTION FOR MANAGEMENT INTERFACE

The RIC II has been designed so it may be connected to the Management bus directly or via external bus transceivers. The latter is advantageous in large repeaters. In this application the system backplane is often heavily loaded beyond the drive capabilities of the on-chip bus drivers.

The uni-directional nature of information transfer on the $\overline{\text{MCRS}}$, MRXD and MRXC signals, means a single open drain output pin is adequate for each of these signals. The Management Enable (MEN) RIC II output pin performs the function of a drive enable for an external bus transceiver if one is required.

In common with the Inter-RIC bus signals $\overline{\text{ACTN}}$, $\overline{\text{ANYXN}}$, $\overline{\text{COLN}}$ and $\overline{\text{IRE}}$ the $\overline{\text{MCRS}}$ active level asserted by the $\overline{\text{MCRS}}$ output is determined by the state of the BINV Mode Load configuration bit.

MODIFIED PACKET STATUS REGISTER 5 (MPS = 1 IN GSR REGISTER)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	SAM	RUNT	RBY10	RBY9	RBY8

Bit	R/W	Symbol	Description
D0	NA	RBY8	Eighth bit of receive byte count.
D1	NA	RBY9	Ninth bit of receive byte count.
D2	NA	RBY10	Tenth bit of receive byte count.
D3	NA	RUNT	**RUNT:** A packet whose length is less than or equal to 64 bytes from SFD and greater than or equal to SE length. 0: Last packet received was not a runt. 1: Last packet received was a runt.
D4	NA	SAM	**SOURCE ADDRESS MISMATCH:** 0: Source address match occurred for the last packet. 1: Source address mismatch occurred for the last packet.
D[7:5]	NA	res	**RESERVED FOR FUTURE USE:** Reads as a logic 0.

7.0 Port Block Functions

The RIC II has 13 port logic blocks (one for each network connection). In addition to the packet repetition operations already described, the port block performs two other functions:

1. the physical connection to the network segment (transceiver function).
2. it provides a means to protect the network from malfunctioning segments (segment partition).

Each port has its own status register. This register allows the user to determine the current status of the port and configure a number of port specific functions.

7.1 TRANSCEIVER FUNCTIONS

The RIC II may connect to network segments in three ways:

1. over AUI cable to transceiver boxes,
2. directly to board mounted transceivers,
3. to twisted pair cable via a simple interface.

The first method is only supported by RIC II port 1 (the AUI port). Options (2) and (3) are available on ports 2 to 13. The selection of the desired option is made at device initialization during the Mode Load operation. The Transceiver Bypass XBYPAS configuration bits are used to determine whether the ports will utilize the on-chip 10BASE-T transceivers, or bypass these in favor of external transceivers. Four possible combinations of port utilization are supported:

All ports (2 to 13) use the external Transceiver Interface.

Ports 2 to 5 use the external interface, 6 to 13 use the internal 10BASE-T transceivers.

Ports 2 to 7 use the external interface, 8 to 13 use the internal 10BASE-T transceivers.

All ports (2 to 13) use the internal 10BASE-T transceivers.

10BASE-T TRANSCEIVER OPERATION

The RIC II contains virtually all the digital and analog circuits required for connection to 10BASE-T network segments. The only additional active component is an external driver package. The connection for a RIC II port to a 10BASE-T segment is shown in *Figure 7-1*. The diagram shows the components required to connect one of the RIC II's ports to a 10BASE-T segment. The major components are the driver package, a member of the 74ACT family, and an integrated filter/choke network.

The operation of the 10BASE-T transceiver's logical functions may be modified by software control. The default mode of operation is for the transceivers to transmit and expect reception of link pulses. This may be modified if a logic one is written to the $\overline{\text{GDLNK}}$ bit of a port's status register. The port's transceiver will operate normally but will not transmit link pulses nor monitor their reception. Thus the entry to a link fail state and the associated modification of transceiver operation will not occur.

The on-chip 10BASE-T transceivers automatically detect and correct the polarity of the received data stream. This polarity detection scheme relies upon the polarity of the received link pulses and the end of packet waveform. Polarity detection and correction may be disabled under software control.

EXTERNAL TRANSCEIVER OPERATION

RIC II ports 2 to 13 may be connected to media other than twisted-pair by opting to bypass the on-chip transceivers. When using external transceivers the user must have the external transceivers perform collision detection and the other functions associated with an IEEE 802.2 Media Access Unit. *Figure 7-2* shows the connection between a repeater port and a coaxial transceiver using the AUI type interface.

7.2 SEGMENT PARTITION

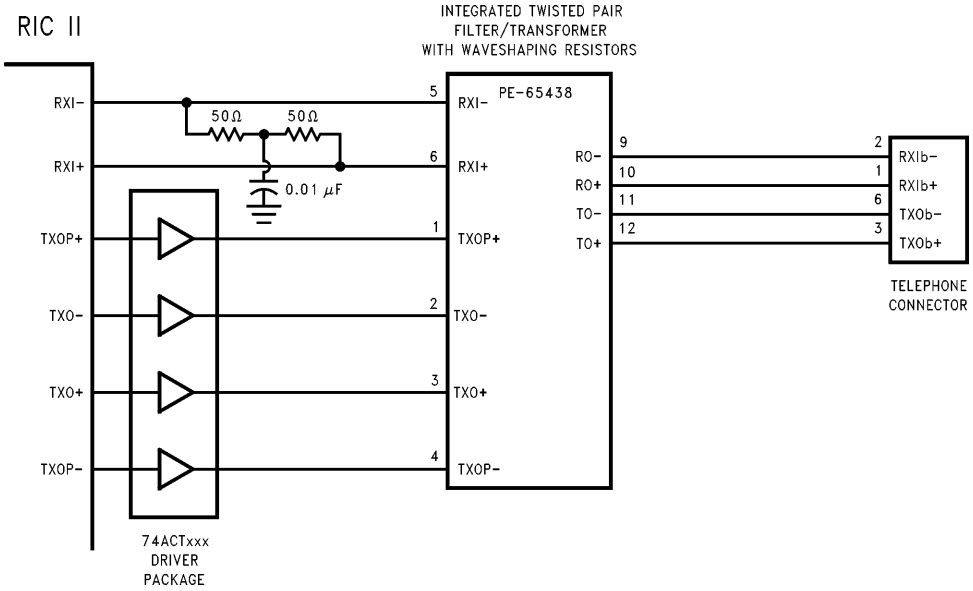
Each of the RIC II's ports has a dedicated state machine to perform the functions defined by the IEEE partition algorithm as shown in *Figure 7-3*. To allow users to customize this algorithm for different applications, a number of user selected options are available during device configuration at power up (the Mode Load cycle).

Five different options are provided:

1. Operation of the 13 partition state machines may be disabled via the disable partition $\overline{\text{DPART}}$ configuration bit (pin D6).
2. The value of consecutive counts required to partition a segment (the CCLimit specification) may be set at either 31 or 63 consecutive collisions.
3. The use of the TW5 specification in the partition algorithm differentiates between collisions which occur early in a packet (before TW5 has elapsed) and those which occur late in the packet (after TW5 has elapsed). These late or ''out of window'' collisions can be regarded in the same manner as early collisions if the Out of Window Collision Enable $\overline{\text{OWCE}}$ option is selected. This configuration bit is applied to the D4 pin during the Mode Load operation. The use of $\overline{\text{OWCE}}$ delays until the end of the packet the operation of the state diagram branch marked (1) and enables the branch marked (2) in *Figure 7-3*.
4. The operation of the ports' state machines when reconnecting a segment may also be modified by the user. The Transmit Only $\overline{\text{TXONLY}}$ configuration bit allows the user to prevent segment reconnection unless the reconnecting packet is being sourced by the repeater. In this case the repeater is transmitting on to the segment, rather than the segment transmitting when the repeater is idle. The normal mode of reconnection does not differentiate between such packets. The $\overline{\text{TXONLY}}$ configuration bit is input on pin D5 during the Mode Load cycle. If this option is selected the operation of the state machine branch marked (3) in *Figure 7-3* is affected.
5. The RIC II may be configured to use an additional criterion for segment partition. This is referred to as loop back partition. If this operation is selected the partition state machine monitors the receive and collision inputs from a network segment to discover if they are active when the port is transmitting. Thus determining if the network transceiver is looping back the data pattern from the cable. A port may be partitioned if no data or collision signals are seen by the partition logic in the following window: 61 to 96 network bit times after the start of transmission; see data sheet Section 8 for details. A segment partitioned by this operation may be reconnected in the normal manner.

In addition to the autonomous operation of the partition state machines, the user may reset these state machines. This may be done individually to each port by writing a logic one to the $\overline{\text{PART}}$ bit in its status register. The port's partition state machine and associated counters are reset and the port is reconnected to the network. The reason why a port became partitioned may be discovered by the user by reading the port's status register.

7.0 Port Block Functions (Continued)



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Note: For recommended modules, see ''Ethernet Magnetics Vendors for 10BASE-T, 10BASE2, and BASE5''. In this example, Pulse Engineering's PE-65438 device is used.

FIGURE 7-1. Port Connection to a 10-BASE-T Segment

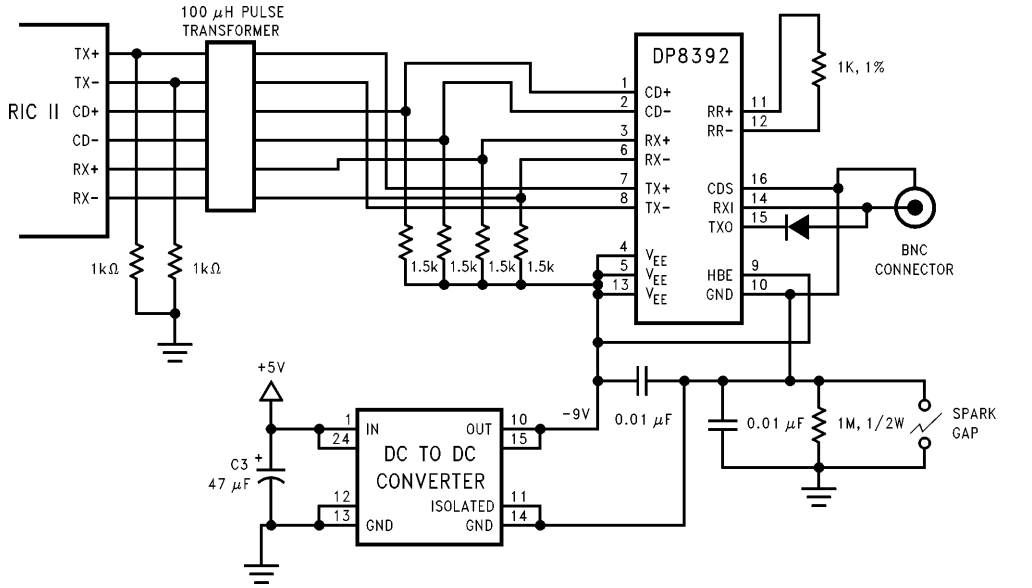

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FIGURE 7-2. Port Connection to a 10-BASE2 Segment (AUI Interface Selected)

The above diagrams show a RIC II port (numbers 2 to 13) connected to a 10BASE-T and a 10BASE2 segment. The values of any components not indicated above are to be determined.

7.0 Port Block Functions (Continued)

7.3 PORT STATUS REGISTER FUNCTIONS

Each RIC II port has its own status register. In addition to providing status concerning the port and its network segment, the register allows the following operations to be performed upon the port:

1. Port Disable
2. Link Disable
3. Partition Reconnection
4. Selection between normal and reduced squelch levels

Note that the link disable and port disable functions are mutually exclusive functions, i.e. disabling link does not affect receiving and transmitting from/to that port and disabling a port does not disable link.

When a port is disabled packet transmission and reception between the port's segment and the rest of the network is prevented.

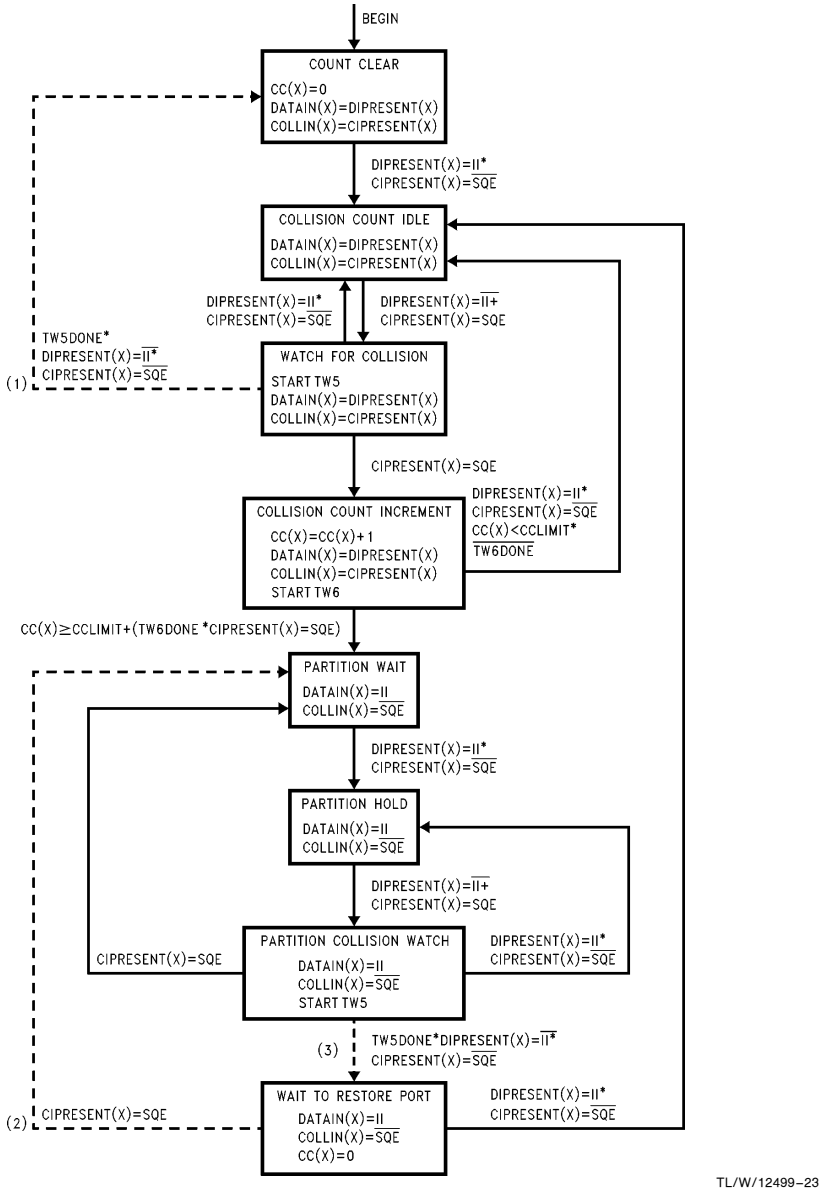

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FIGURE 7-3. IEEE Segment Partition Algorithm

7.0 Port Block Functions (Continued)

7.4 LOCAL PORTS AND INTER-RIC BUS EXPECTED ACTIVITY

The RIC II incorporates security options into the repeater. The configuration of the security features can be performed globally, or on a per port basis. Upon packet reception by the RIC II, depending on port configuration, the repeater will either: transmit the actual data intact to the port, or transmit pseudo random data to the port during the data field of the packet.

RIC II security features can be globally enabled/disabled during the MLOAD process, or via the RIC II Configuration Register bit GSE (global security enable). When GSE is set, the device will, for all ports, set the port SME (Security Mode), ESA (Source Address Security), EDA (Destination Address Security), LME (Learn Mode Enable) bits in the Port Security Configuration Register (PSCR).

Learning Mode for all the port CAMs can be globally enabled during the MLOAD process, or via the GLME (Global Learn Mode Enable) bit in the Global Security Register (GSR). When GLME is set, the device will, for all ports, set the LME (Learn Mode Enable) bit in the PSCR register.

In a multi RIC II repeater environment, each RIC II will get the packet intact over the Inter-RIC bus (except on source address mismatch occurrence when configured in the security mode). Each RIC II will transmit either the real data or pseudo random data to the port depending on the port configuration.

Rule of Thumb (See table on next page)

1. Security Mode Disabled

   RIC II performs the same repeater operations as the RIC. The received data is transmitted to all ports, and on the Inter-RIC bus.

2. Security Mode Enabled

   a. When a port's ESA = 0,

      1) and the port's EDA = 0, then the repeater will repeat the data on the port, and the Inter-RIC bus.

      2) and the port's EDA = 1, then the repeater will repeat the data on destination address match. On a destination address mismatch, the repeater will transmit random data on that port. In both cases, the repeater will transmit data on the Inter-RIC bus.

   b. When a port's ESA = 1,

      1) and the port's EDA = 0, then on a valid source address match, the repeater will repeat the data on that port, and on the Inter-RIC bus. If source address mismatch occurs, then the repeater will transmit random data to the port, and on the Inter-RIC bus.

      2) and the port's EDA = 1, then on a valid source and destination address match, the repeater will repeat the data on the port. If source address matches, but the destination address does not match, then the repeater will transmit random data to that port. In both of these cases, the repeater will repeat the data on the Inter-RIC bus. When source address mismatch occurs, then the repeater will transmit random data to the port and on the Inter-RIC bus.

The following table describes the type of data in the packet (actual data or pseudo random data) is transmitted out of the ports, and over the Inter-RIC bus. It is assumed that the repeater is powered up in security mode (GLME = 0).

For example, suppose the repeater is in security mode (SME = 1), and configured to perform address comparison only on destination address (ESA = 0 and EDA = 1). If a packet is received whose destination address does not match with that stored address in a designated CAM, then all the transmitting ports switch to random packet, while the data is transmitted intact over the Inter-RIC bus. The other cascaded repeaters will compare the packet's destination address with their own internal CAMs for proper decision making.

7.0 Port Block Functions (Continued)

7.5 LOCAL PORTS AND INTER-RIC BUS DATA FIELD CONTENTS

SME	ESA	EDA	Source Address of Packet	Destination Address of Packet	Transmitting Ports	Inter-RIC Bus
0	X	X	X	X	Repeat	Repeat
1	0	0	X	X	Repeat	Repeat
		1	Match	Match	Repeat	Repeat
			Match	Mismatch	Random	Repeat
			Mismatch	Match	Repeat	Repeat
			Mismatch	Mismatch	Random	Repeat
	1	0	Match	Match	Repeat	Repeat
			Match	Mismatch	Repeat	Repeat
			Mismatch	X	Random	Random
		1	Match	Match	Repeat	Repeat
			Match	Mismatch	Random	Repeat
			Mismatch	X	Random	Random

Note: SME: Security Mode bit in the Port Security Configuration Register (PSCR).
ESA: Source Address Security bit in the PSCR register.
EDA: Destination Address Security bit in the PSCR register.

8.0 RIC II Registers

RIC II REGISTER ADDRESS MAP

The RIC II's registers may be accessed by applying the required address to the five Register Address (RA(4:0)) input pins. Pin RA4 makes the selection between the upper and lower halves of the register array. The lower half of the register map consists of 16 registers:

1 RIC II Real Time Status and Configuration register,
13 Port Real Time Status registers,
1 RIC II Configuration register,
1 Real Time Interrupt Status register.

These registers may be directly accessed at any time via the RA(4:0) pins, (RA4 = 0).

The upper half of the register map, (RA4 = 1), is organized as 15 pages of registers. These pages include registers for port security configuration (global and on a per port basis), event count registers, port CAM and shared CAM locations, CAM location mask registers, etc. See Memory Map and Register Description sections for details.

Register access within these pages is performed using the RA(4:0) pins, (RA4 = 1). Page switching is performed by writing to the Page Selection bits (PSEL3,2,1, and 0). These bits are found in the Page Select Register, located at address 10 hex on each page of the upper half of the register array. At power on these bits default to 0 Hex, i.e., page zero.

On the RIC II the following registers have been added/modified from the RIC registers:

1. Page Select Register
2. ECIMR-2 register added to page (0)
3. GSR register added to page (0)
4. Upper and Lower EIR registers added to page (1)
5. Added all registers on pages (4)–(15)
6. Modification Option for Management Packet Status Register 5 (PSR5) on the Management Bus.

8.0 RIC II Registers (Continued)

Register Address Map

	Name			
Address	**PAGE (0)**	**PAGE (1)**	**PAGE (2)**	**PAGE (3)**
00H	RIC II Status and Configuration Register			
01H	Port 1 Status Register			
02H	Port 2 Status Register			
03H	Port 3 Status Register			
04H	Port 4 Status Register			
05H	Port 5 Status Register			
06H	Port 6 Status Register			
07H	Port 7 Status Register			
08H	Port 8 Status Register			
09H	Port 9 Status Register			
0AH	Port 10 Status Register			
0BH	Port 11 Status Register			
0CH	Port 12 Status Register			
0DH	Port 13 Status Register			
0EH	RIC II Configuration Register			
0FH	Real Time Interrupt Register			
10H	Page Select Register			
11H	Device Type Register	Port 1 Event Record Register (ERR)	res	res
12H	Lower Event Count Mask Register (ECMR)	Port 2 ERR	Port 1 Lower Event Count Register (ECR)	Port 8 Lower ECR
13H	Upper ECMR	Port 3 ERR	Port 1 Upper ECR	Port 8 Upper ECR
14H	Event Record Mask Register	Port 4 ERR	Port 2 Lower ECR	Port 9 Lower ECR
15H	***ECIMR - 2***	Port 5 ERR	Port 2 Upper ECR	Port 9 Upper ECR
16H	Management/Interrupt Configuration Register	Port 6 ERR	Port 3 Lower ECR	Port 10 Lower ECR
17H	RIC II Address Register	Port 7 ERR	Port 3 Upper ECR	Port 10 Upper ECR
18H	Packet Compress Decode Register	Port 8 ERR	Port 4 Lower ECR	Port 11 Lower ECR
19H	res	Port 9 ERR	Port 4 Upper ECR	Port 11 Upper ECR
1AH	res	Port 10 ERR	Port 5 Lower ECR	Port 12 Lower ECR
1BH	res	Port 11 ERR	Port 5 Upper ECR	Port 12 Upper ECR
1CH	res	Port 12 ERR	Port 6 Lower ECR	Port 13 Lower ECR
1DH	***GSR***	Port 13 ERR	Port 6 Upper ECR	Port 13 Upper ECR
1EH	res	***Upper EIR***	Port 7 Lower ECR	res
1FH	IFG Threshold Select	***Lower EIR***	Port 7 Upper ECR	res

Note: Registers written in ***bold*** are the new RIC II specific registers which are not present in the RIC.

8.0 RIC II Registers (Continued)

Register Address Map (Continued)

	Name			
Address	**PAGE (4)**	**PAGE (5)**	**PAGE (6)**	**PAGE (8)**
11H	Port 1 ECR-2	Port 1 CAM 1	Port 5 PCPR	Port 9 PSCR
12H	Port 2 ECR-2	Port 1 CAM 2	Port 5 CAM 1	Port 9 PCPR
13H	Port 3 ECR-2	Port 2 PSCR	Port 5 CAM 2	Port 9 CAM 1
14H	Port 4 ECR-2	Port 2 PCPR	Port 6 PSCR	Port 9 CAM 2
15H	Port 5 ECR-2	Port 2 CAM 1	Port 6 PCPR	Port 10 PSCR
16H	Port 6 ECR-2	Port 2 CAM 2	Port 6 CAM 1	Port 10 PCPR
17H	Port 7 ECR-2	Port 3 PSCR	Port 6 CAM 2	Port 10 CAM 1
18H	Port 8 ECR-2	Port 3 PCPR	Port 7 PSCR	Port 10 CAM 2
19H	Port 9 ECR-2	Port 3 CAM 1	Port 7 PCPR	Port 11 PSCR
1AH	Port 10 ECR-2	Port 3 CAM 2	Port 7 CAM 1	Port 11 PCPR
1BH	Port 11 ECR-2	Port 4 PSCR	Port 7 CAM 2	Port 11 CAM 1
1CH	Port 12 ECR-2	Port 4 PCPR	Port 8 PSCR	Port 11 CAM 2
1DH	Port 13 ECR-2	Port 4 CAM 1	Port 8 PCPR	Port 12 PSCR
1EH	Port 1 PSCR	Port 4 CAM 2	Port 8 CAM 1	Port 12 PCPR
1FH	Port 1 PCPR	Port 5 PSCR	Port 8 CAM 2	Port 12 CAM 1

	Name			
Address	**PAGE (9)**	**PAGE (10)**	**PAGE (11)**	**PAGE (12)**
11H	Port 12 CAM 2	SCAM Lo 3	SCAM Lo 8	SCAM Lo 13
12H	Port 13 PSCR	CLMR Lo Loc 3	CLMR Lo Loc 8	CLMR Lo Loc 13
13H	Port 13 PCPR	CLMR Hi Loc 3	CLMR Hi Loc 8	CLMR Hi Loc 13
14H	Port 13 CAM 1	SCAM Lo 4	SCAM Lo 9	SCAM Lo 14
15H	Port 13 CAM 2	CLMR Lo Loc 4	CLMR Lo Loc 9	CLMR Lo Loc 14
16H	SCVR 1	CLMR Hi Loc 4	CLMR Hi Loc 9	CLMR Hi Loc 14
17H	SCVR 2	SCAM Lo 5	SCAM Lo 10	SCAM Lo 15
18H	SCVR 3	CLMR Lo Loc 5	CLMR Lo Loc 10	CLMR Lo Loc 15
19H	SCVR 4	CLMR Hi Loc 5	CLMR Hi Loc 10	CLMR Hi Loc 15
1AH	SCAM Lo 1	SCAM Lo 6	SCAM Lo 11	SCAM Lo 16
1BH	CLMR Lo Loc 1	CLMR Lo Loc 6	CLMR Lo Loc 11	CLMR Lo Loc 16
1CH	CLMR Hi Loc 1	CLMR Hi Loc 6	CLMR Hi Loc 11	CLMR Hi Loc 16
1DH	SCAM Lo 2	SCAM Lo 7	SCAM Lo 12	SCAM Lo 17
1EH	CLMR Lo Loc 2	CLMR Lo Loc 7	CLMR Lo Loc 12	CLMR Lo Loc 17
1FH	CLMR Hi Loc 2	CLMR Hi Loc 7	CLMR Hi Loc 12	CLMR Hi Loc 17

8.0 RIC II Registers (Continued)

Register Address Map (Continued)

	Name		
Address	**PAGE (13)**	**PAGE (14)**	**PAGE (15)**
11H	SCAM Lo 18	SCAM Lo 23	SCAM Lo 28
12H	CLMR Lo Loc 18	CLMR Lo Loc 23	CLMR Lo Loc 28
13H	CLMR Hi Loc 18	CLMR Hi Loc 23	CLMR Hi Loc 28
14H	SCAM Lo 19	SCAM Lo 24	SCAM Lo 29
15H	CLMR Lo Loc 19	CLMR Lo Loc 24	CLMR Lo Loc 29
16H	CLMR Hi Loc 19	CLMR Hi Loc 24	CLMR Hi Loc 20
17H	SCAM Lo 20	SCAM Lo 25	SCAM Lo 30
18H	CLMR Lo Loc 20	CLMR Lo Loc 25	CLMR Lo Loc 30
19H	CLMR Hi Loc 20	CLMR Hi Loc 25	CLMR Hi Loc 30
1AH	SCAM Lo 21	SCAM Lo 26	SCAM Lo 31
1BH	CLMR Lo Loc 21	CLMR Lo Loc 26	CLMR Lo Loc 31
1CH	CLMR Hi Loc 21	CLMR Hi Loc 26	CLMR Hi Loc 31
1DH	SCAM Lo 22	SCAM Lo 27	SCAM Lo 32
1EH	CLMR Lo Loc 22	CLMR Lo Loc 27	CLMR Lo Loc 32
1FH	CLMR Hi Loc 22	CLMR Hi Loc 27	CLMR Hi Loc 32

8.0 RIC II Registers (Continued)

Register Array Bit Map Addresses 00H to 10H

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	BINV	BYPAS2	BYPAS1	$\overline{\text{APART}}$	$\overline{\text{JAB}}$	$\overline{\text{AREC}}$	$\overline{\text{ACOL}}$	resv
01 to 0D	DISPT	SQL	PTYPE1	PTYPE0	$\overline{\text{PART}}$	$\overline{\text{REC}}$	$\overline{\text{COL}}$	$\overline{\text{GDLNK}}$
0E	MINMAX	$\overline{\text{DPART}}$	$\overline{\text{TXONLY}}$	$\overline{\text{OWCE}}$	$\overline{\text{LPPART}}$	$\overline{\text{CCLIM}}$	TW2	GSE
0F	IVCTR3	IVCTR2	IVCTR1	IVCTR0	ISRC3	ISRC2	ISRC1	ISRC0
10	FC	HC	LC	FF	PSEL3	PSEL2	PSEL1	PSEL0

Register Array Bit Map Addresses 11H to 1FH Page (0)

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
11	1	0	0	0	0	0	X	X
12	BDLNKC	PARTC	RECC	SEC	NSFDC	PLERC	ELBERC	JABC
13	resv	resv	OWCC	RXCOLC	TXCOLC	resv	FWF	ROR
14	BDLNKE	PARTE	OWCE	SEE	NSFDE	PLERE	ELBERE	JABE
15	res	ISAM	FWF-2	ROR-2	OWCC-2	PARTC-2	FAEC	FCSC
16	$\overline{\text{IFC}}$	$\overline{\text{IHC}}$	$\overline{\text{ILC}}$	$\overline{\text{IFF}}$	$\overline{\text{IREC}}$	$\overline{\text{ICOL}}$	$\overline{\text{IPART}}$	MIFCON
17	A5	A4	A3	A2	A1	A0	resv	resv
18	PCD7	PCD6	PCD5	PCD4	PCD3	PCD2	PCD1	PCD0
1D	res	GLME	res	DSM	res	MPS	GRP	SAC
1F	IFGT7	IFGT6	IFGT5	IFGT4	IFGT3	IFGT2	IFGT1	IFGT0

Register Array Bit Map Addresses 11H to 1FH Page (1)

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
11 to 1D	BDLNK	PART	OWC	SE	NSFD	PLER	ELBER	JAB
1E	ER8	ER7	ER6	ER5	ER4	ER3	ER2	ER1
1F	DLU	res	res	ER13	ER12	ER11	ER10	ER9

Register Array Bit Map Addresses 11H to 1FH Pages (2) and (3)

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
11	—	—	—	—	—	—	—	—
Even Locations	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
Odd Locations	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8

8.0 RIC II Registers (Continued)

Register Array Bit Map Addresses 11H to 1FH Page (4)

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
11 to 1D	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
1E	res	EDA	ESA	SAM	MCE	BCE	SME	LME
1F	ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0

Register Array Bit Map Addresses 11H to 1FH Page (5)

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
11, 12	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0
13	res	EDA	ESA	SAM	MCE	BCE	SME	LME
14	ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0
15, 16	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0
17	res	EDA	ESA	SAM	MCE	BCE	SME	LME
18	ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0
19, 1A	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0
1B	res	EDA	ESA	SAM	MCE	BCE	SME	LME
1C	ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0
1D, 1E	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0
1F	res	EDA	ESA	SAM	MCE	BCE	SME	LME

Register Array Bit Map Addresses 11H to 1FH Page (6)

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
11	ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0
12, 13	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0
14	res	EDA	ESA	SAM	MCE	BCE	SME	LME
15	ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0
16, 17	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0
18	res	EDA	ESA	SAM	MCE	BCE	SME	LME
19	ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0
1A, 1B	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0
1C	res	EDA	ESA	SAM	MCE	BCE	SME	LME
1D	ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0
1E, 1F	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0

8.0 RIC II Registers (Continued)

Register Array Bit Map Addresses 11H to 1FH Page (8)

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
11	res	EDA	ESA	SAM	MCE	BCE	SME	LME
12	ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0
13, 14	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0
15	res	EDA	ESA	SAM	MCE	BCE	SME	LME
16	ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0
17, 18	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0
19	res	EDA	ESA	SAM	MCE	BCE	SME	LME
1A	ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0
1B, 1C	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0
1D	res	EDA	ESA	SAM	MCE	BCE	SME	LME
1E	ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0
1F	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0

Note: For Port CAM register bits (PCAM**x**__D[7:0]) and Shared CAM register bits (SCAM**x**__D[7:0]) **x** represents the port number.

Register Array Bit Map Addresses 11H to 1FH Page (9)

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
11	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0
12	res	EDA	ESA	SAM	MCE	BCE	SME	LME
13	ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0
14, 15	PCAMx __D7	PCAMx __D6	PCAMx __D5	PCAMx __D4	PCAMx __D3	PCAMx __D2	PCAMx __D1	PCAMx __D0
16	ADV8	ADV7	ADV6	ADV5	ADV4	ADV3	ADV2	ADV1
17	ADV16	ADV15	ADV14	ADV13	ADV12	ADV11	ADV10	ADV9
18	ADV24	ADV23	ADV22	ADV21	ADV20	ADV19	ADV18	ADV17
19	ADV32	ADV31	ADV30	ADV29	ADV28	ADV27	ADV26	ADV25
1A	SCAMx __D7	SCAMx __D6	SCAMx __D5	SCAMx __D4	SCAMx __D3	SCAMx __D2	SCAMx __D1	SCAMx __D0
1B	P8	P7	P6	P5	P4	P3	P2	P1
1C	PTR2	PTR1	PTR0	P13	P12	P11	P10	P9
1D	SCAMx __D7	SCAMx __D6	SCAMx __D5	SCAMx __D4	SCAMx __D3	SCAMx __D2	SCAMx __D1	SCAMx __D0
1E	P8	P7	P6	P5	P4	P3	P2	P1
1F	PTR2	PTR1	PTR0	P13	P12	P11	P10	P9

8.0 RIC II Registers (Continued)

Register Array Bit Map Addresses 11H to 1FH Pages (AH, BH, CH, DH, EH, FH)

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
11	SCAMx __D7	SCAMx __D6	SCAMx __D5	SCAMx __D4	SCAMx __D3	SCAMx __D2	SCAMx __D1	SCAMx __D0
12	P8	P7	P6	P5	P4	P3	P2	P1
13	PTR2	PTR1	PTR0	P13	P12	P11	P10	P9
14	SCAMx __D7	SCAMx __D6	SCAMx __D5	SCAMx __D4	SCAMx __D3	SCAMx __D2	SCAMx __D1	SCAMx __D0
15	P8	P7	P6	P5	P4	P3	P2	P1
16	PTR2	PTR1	PTR0	P13	P12	P11	P10	P9
17	SCAMx __D7	SCAMx __D6	SCAMx __D5	SCAMx __D4	SCAMx __D3	SCAMx __D2	SCAMx __D1	SCAMx __D0
18	P8	P7	P6	P5	P4	P3	P2	P1
19	PTR2	PTR1	PTR0	P13	P12	P11	P10	P9
1A	SCAMx __D7	SCAMx __D6	SCAMx __D5	SCAMx __D4	SCAMx __D3	SCAMx __D2	SCAMx __D1	SCAMx __D0
1B	P8	P7	P6	P5	P4	P3	P2	P1
1C	PTR2	PTR1	PTR0	P13	P12	P11	P10	P9
1D	SCAMx __D7	SCAMx __D6	SCAMx __D5	SCAMx __D4	SCAMx __D3	SCAMx __D2	SCAMx __D1	SCAMx __D0
1E	P8	P7	P6	P5	P4	P3	P2	P1
1F	PTR2	PTR1	PTR0	P13	P12	P11	P10	P9

Note: For Port CAM register bits (PCAM**x**__D[7:0]) and Shared CAM register bits (SCAM**x**__D[7:0]) **x** represents the port number.

8.0 RIC II Registers (Continued)

RIC II STATUS AND CONFIGURATION REGISTER (ADDRESS 00H)

The lower portion of this register contains real time information concerning the operation of the RIC II. The upper three bits represent the chosen configuration of the transceiver interface employed.

D7	D6	D5	D4	D3	D2	D1	D0
BINV	BYPAS2	BYPAS1	$\overline{\text{APART}}$	$\overline{\text{JAB}}$	$\overline{\text{AREC}}$	$\overline{\text{ACOL}}$	resv

Bit	R/W	Symbol	Description
D0	R	resv	**RESERVED FOR FUTURE USE:** Reads as a logic 1.
D1	R	$\overline{\text{ACOL}}$	**ANY COLLISIONS:** 0: A collision is occurring at one or more of the RIC II's ports. 1: No collisions.
D2	R	$\overline{\text{AREC}}$	**ANY RECEIVE:** 0: One of the RIC II's ports is the current packet or collision receiver. 1: No packet or collision reception within this RIC II.
D3	R	$\overline{\text{JAB}}$	**JABBER PROTECT:** 0: The RIC II has been forced into jabber protect state by one of its ports or by another port on the Inter-RIC bus (Multi-RIC II operations). 1: No jabber protect conditions exist.
D4	R	$\overline{\text{APART}}$	**ANY PARTITION:** 0: One or more ports are partitioned. 1: No ports are partitioned.
D5 D6	R R	BYPAS1 BYPAS2	These bits define the configuration of ports 2 to 13, i.e., their use if the internal 10BASE-T transceivers or the external (AUI-like) transceiver interface.
D7	R	BINV	**BUS INVERT:** This register bit informs whether the Inter-RIC signals: IRE, ACTN, ANYXN, COLN and Management bus signal MCRS are: 0: Active high. 1: Active low.

8.0 RIC II Registers (Continued)

PORT REAL TIME STATUS REGISTERS (ADDRESS 01H TO 0DH)

D7	D6	D5	D4	D3	D2	D1	D0
DISPT	SQL	PTYPE1	PTYPE0	$\overline{\text{PART}}$	$\overline{\text{REC}}$	$\overline{\text{COL}}$	$\overline{\text{GDLNK}}$

Bit	R/W	Symbol	Description
D0	R$\overline{\text{W}}$	$\overline{\text{GDLNK}}$	**GOOD LINK:** 0: Link pulses are being received by the port. 1: Link pulses are not being received by the port logic. (Note 1)
D1	R	$\overline{\text{COL}}$	**COLLISION:** 0: A collision is happening or has occurred during the current packet. 1: No collisions have occurred as yet during this packet.
D2	R	$\overline{\text{REC}}$	**RECEIVE:** 0: This port is now or has been the receive source of packet or collision information for the current packet. 1: This port has not been the receive source during the current packet.
D3	R/W	$\overline{\text{PART}}$	**PARTITION:** Writing a logic one to this bit forces segment reconnection and partition state machine reset. Writing a zero to this bit has no effect. 0: This port is partitioned. 1: This port is not partitioned.
D(5,4)	R	PTYPE0 PTYPE1	**PARTITION TYPE 0** **PARTITION TYPE 1** The partition type bits provide information specifying why the port is partitioned.

PTYPE1	PTYPE0	Information
0	0	Consecutive collision limit reached.
0	1	Excessive length of collision limit reached.
1	0	Failure to see data loopback from transceiver in monitored window.
1	1	Processor forced reconnection.

D6	R/W	SQL	**SQUELCH LEVELS:** (Notes 2 and 3) 0: Port operates with normal IEEE receive squelch level. 1: Port operates with reduced receive squelch level.
D7	R/W	DISPT	**DISABLE PORT:** 0: Port operates as defined by repeater operations. 1: All port activity is prevented.

Note 1: Writing a 1 to this bit will cause the 10Base-T transceiver not to transmit or monitor the reception of link pulses. If the internal 10BASE-T transceivers are not selected or if port 1 (AUI port) is read, then this bit is undefined.

Note 2: This bit has no effect when external transceiver is selected.

Note 3 (for RIC II only): In addition to hysteresis that DP83950 RIC provides on normal receive squelch, DP83952 RIC II provides a hysteresis when operating in the reduced squelch level mode.

8.0 RIC II Registers (Continued)

RIC II CONFIGURATION REGISTER (ADDRESS 0EH)

This register displays the state of a number of RIC II configuration bits loaded during the Mode Load operation.

D7	D6	D5	D4	D3	D2	D1	D0
MINMAX	$\overline{\text{DPART}}$	$\overline{\text{TXONLY}}$	$\overline{\text{OWCE}}$	$\overline{\text{LPPART}}$	$\overline{\text{CCLIM}}$	TW2	GSE

Bit	R/W	Symbol	Description
D0	R	GSE	**GLOBAL SECURITY ENABLE:** 0: RIC II operates in security mode with Learning Mode enabled by default for all ports. 1: RIC II operates in non-security mode.
D1	R	TW2	**CARRIER RECOVERY TIME:** 0: TW2 set at 5 bits. 1: TW2 set at 3 bits.
D2	R	$\overline{\text{CCLIM}}$	**CONSECUTIVE COLLISION LIMIT:** 0: Consecutive collision limit set at 63 collisions. 1: Consecutive collision limit set at 31 collisions.
D3	R	$\overline{\text{LPPART}}$	**LOOPBACK PARTITION:** 0: Partitioning upon lack of loopback from transceivers is enabled. 1: Partitioning upon lack of loopback from transceivers is disabled.
D4	R	$\overline{\text{OWCE}}$	**OUT OF WINDOW COLLISION ENABLE:** 0: Out of window collisions are treated as in window collisions by the segment partition state machines. 1: Out of window collisions are treated as out of window collisions by the segment partition state machines.
D5	R	$\overline{\text{TXONLY}}$	**ONLY RECONNECT UPON SEGMENT TRANSMISSION:** 0: A segment will only be reconnected to the network if a packet transmitted by the RIC II onto that segment fulfills the requirements of the segment reconnection algorithm. 1: A segment will be reconnected to the network by any packet on the network which fulfills the requirements of the segment reconnection algorithm.
D6	R	$\overline{\text{DPART}}$	**DISABLE PARTITION:** 0: Partitioning of ports by on-chip algorithms is prevented. 1: Partitioning of ports by on-chip algorithms is enabled.
D7	R	MINMAX	**MINIMUM/MAXIMUM DISPLAY MODE:** 0: LED display set in minimum display mode. 1: LED display set in maximum display mode.

8.0 RIC II Registers (Continued)

REAL TIME INTERRUPT REGISTER (ADDRESS 0FH)

The Real Time Interrupt register (RTI) contains information which may change on a packet by packet basis. Any remaining interrupts which have not been serviced before the following packet is transmitted are cleared. Since multiple interrupt sources may be displayed by the RTI a priority scheme is implemented. A read cycle to the RTI gives the interrupt source and an address vector indicating the RIC II port which generated the interrupt.

The order of priority for the display of interrupt information is as follows (in secure mode only):

1. **Source Address Mismatch (added feature to the RIC II which is not present in the RIC)**,
2. The receive source of network activity (Port N),
3. The first RIC II port showing collision,
4. A port partitioned or reconnected.

During the repetition of a single packet it is possible that multiple ports may be partitioned or alternatively reconnected. The ports have equal priority in displaying partition/reconnection information. This data is derived from the ports by the RTI register as it polls consecutively around the ports.

Reading the RTI clears the particular interrupt. If no interrupt sources are active the RTI returns a no valid interrupt status.

D7	D6	D5	D4	D3	D2	D1	D0
IVCTR3	IVCTR2	IVCTR1	IVCTR0	ISRC3	ISRC2	ISRC1	ISRC0

Bit	R/W	Symbol	Description
D(3:0)	R	ISCR(3:0)	**INTERRUPT SOURCE:** These four bits indicate the reason why the interrupt was generated.
D(7:4)	R	IVCTR(3:0)	**INTERRUPT VECTOR:** This field defines the port address responsible for generating the interrupt.

The following table shows the mapping of interrupt sources onto the D3 to D0 pins. Essentially each of the three interrupt sources has a dedicated bit in this field. If a read to the RTI produces a low logic level on one of these bits then the interrupt source may be directly decoded. Associated with the source of the interrupt is the port where the event is occurring. If no unmasked events (receive, collision, etc.), have occurred when the RTI is read then an all ones pattern is driven by the RIC onto the data pins.

D7	D6	D5	D4	D3	D2	D1	D0	Comments
PA3	**PA2**	**PA1**	**PA0**	**1**	**1**	**0**	**1**	**Source Address Mismatch** **PA(3:0) = Port Address for the Mismatch**
PA3	PA2	PA1	PA0	1	1	0	1	First Collision PA(3:0) = Collision Port Address
PA3	PA2	PA1	PA0	1	0	1	1	Receive PA(3:0) = Receive Port Address
PA3	PA2	PA1	PA0	0	1	1	1	Partition Reconnection PA(3:0) = Partition Port Address
1	1	1	1	1	1	1	1	No Valid Interrupt

8.0 RIC II Registers (Continued)

PAGE SELECT REGISTER ((ALL PAGES) ADDRESS 10H)

The Page Select register performs two functions:

1. It enables switches to be made between register pages,
2. It provides status information regarding the Event Logging Interrupts.

D7	D6	D5	D4	D3	D2	D1	D0
FC	HC	LC	FF	PSEL3	PSEL2	PSEL1	PSEL0

Bit	R/W	Symbol	Description
D(3:0)	R/W	PSEL(3:0)	**PAGE SELECT BITS:** When read these bits indicate the currently selected Upper Register Array Page. Write cycles to these locations facilitates page swapping.
D4	R	FF	**FLAG FOUND:** This indicates one of the unmasked event recording latches has been set.
D5	R	LC	**LOW COUNT:** This indicates one of the port event counters has a value less than 00FF Hex.
D6	R	HC	**HIGH COUNT:** This indicates one of the port event counters has a value greater than C000 Hex.
D7	R	FC	**FULL COUNTER:** This indicates one of the port event counters has a value equal to FFFF Hex.

DEVICE TYPE REGISTER (PAGE 0H ADDRESS 11H)

This register may be used to distinguish different revisions of RIC. It will return the value D7 = 1 for the DP83952 RIC II device, or the value D7 = 0 for the DP83950 RIC device. Write operations to this register have no effect upon the contents.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	X	X

8.0 RIC II Registers (Continued)

LOWER EVENT COUNT MASK REGISTER (PAGE 0H ADDRESS 12H)

D7	D6	D5	D4	D3	D2	D1	D0
BDLNKC	PARTC	RECC	SEC	NSFDC	PLERC	ELBERC	JABC

Bit	R/W	Symbol	Description
D0	R/W	JABC	**JABBER COUNT ENABLE:** Enables recording of Jabber Protect events.
D1	R/W	ELBERC	**ELASTICITY BUFFER ERROR COUNT ENABLE:** Enables recording of Elasticity Buffer Error events.
D2	R/W	PLERC	**PHASE LOCK ERROR COUNT ENABLE:** Enables recording of Carrier Error events.
D3	R/W	NSFDC	**NON-SFD COUNT ENABLE:** Enables recording of Non-SFD packet events.
D4	R/W	SEC	**SHORT EVENT COUNT ENABLE:** Enables recording of Short events.
D5	R/W	RECC	**RECEIVE COUNT ENABLE:** Enables recording of Packet Receive (Port N status) events that do not suffer collisions.
D6	R/W	PARTC	**PARTITION COUNT ENABLE:** Enables recording of Partition events.
D7	R/W	BDLNKC	**BAD LINK COUNT ENABLE:** Enables recording of Bad Link events.

UPPER EVENT COUNT MASK REGISTER (PAGE 0H ADDRESS 13H)

The bits in this register effect the Upper and Lower Port Event Count Registers (ECR) on Page (3) addresses 12H to 1FH, and Page (4) addresses 12H to 1DH.

D7	D6	D5	D4	D3	D2	D1	D0
resv	resv	OWCC	RXCOLC	TXCOLC	resv	FWF	ROR

Bit	R/W	Symbol	Description
D0	R/W	ROR	**RESET ON READ:** This bit selects the action a read operation has upon a port's event counter: 0: No effect upon register contents. 1: The counter register is reset.
D1	R/W	FWF	**FREEZE WHEN FULL:** This bit controls the freezing of the Event Count registers when the counter is full (FFFF Hex).
D2	R	resv	**RESERVED FOR FUTURE USE:** This bit should be written with a low logic level.
D3	R/W	TXCOLC	**TRANSMIT COLLISION COUNT ENABLE:** Enables recording of transmit collision events only.
D4	R/W	RXCOLC	**RECEIVE COLLISION COUNT ENABLE:** Enables recording of receive collision events only.
D5	R/W	OWCC	**OUT OF WINDOW COLLISION COUNT ENABLE:** Enables recording of out of window collision events only.
D(7: 6)	R	resv	**RESERVED FOR FUTURE USE:** These bits should be written with a low logic level.

Note: To count all collisions then both the TXCOLC and RXCOLC bits must be set. The OWCC bit should not be set otherwise the port counter will be incremented twice when an out of collision window collision occurs. The OWCC bit alone should be set if only out of window collision are to be counted.

8.0 RIC II Registers (Continued)

EVENT RECORD MASK REGISTER (PAGE 0H ADDRESS 14H)

D7	D6	D5	D4	D3	D2	D1	D0
BDLNKE	PARTE	OWCE	SEE	NSFDE	PLERE	ELBERE	JABE

Bit	R/W	Symbol	Description
D0	R/W	JABE	**JABBER ENABLE:** Enables recording of Jabber Protect events.
D1	R/W	ELBERE	**ELASTICITY BUFFER ERROR ENABLE:** Enables recording of Elasticity Buffer Error events.
D2	R/W	PLERE	**PHASE LOCK ERROR ENABLE:** Enables recording of Carrier Error events.
D3	R/W	NSFDE	**NON-SFD ENABLE:** Enables recording of Non-SFD packet events.
D4	R/W	SEE	**SHORT EVENT ENABLE:** Enables recording of Short Events.
D5	R/W	OWCE	**OUT OF WINDOW COLLISION COUNT ENABLE:** Enables recording of Out of Window Collision events only.
D6	R/W	PARTE	**PARTITION ENABLE:** Enables recording of Partition events.
D7	R/W	BDLNKE	**BAD LINK ENABLE:** Enables recording of Bad Link Events.

Note: Writing a 1 enables the event to be recorded.

EVENT COUNT AND INTERRUPT MASK REGISTER 2 (ECIMR-2) (PAGE 0H ADDRESS 15H)

The bits in this register effect the Port Event Count Register 2, PECR-2 on Page 4, Addresses 11H to 1DH.

D7	D6	D5	D4	D3	D2	D1	D0
res	ISAM	FWF-2	ROR-2	OWCC-2	PARTC-2	FAEC	FCSC

Bit	R/W	Symbol	Description
D0	R/W	FCSC	**FRAME CHECK SEQUENCE COUNT ENABLE:** This bit enables counting the packets with frame check sequence error. 0: Disable the frame check sequence count. 1: Enable the frame check sequence count.
D1	R/W	FAEC	**FRAME ALIGNMENT ERROR COUNT ENABLE:** This bit enables counting the packets with frame alignment error. 0: Disable the frame alignment error count. 1: Enable the frame alignment error count.
D2	R/W	PARTC-2	**PARTITION COUNT ENABLE:** This bit enables recording of partition events. 0: Disable the partition count. 1: Enable the partition count.
D3	R/W	OWCC-2	**OUT OF WINDOW COLLISION COUNT ENABLE:** This bit enables counting of out of window collision events. 0: Disable the out of window collision count. 1: Enable the out of window collision count.
D4	R/W	ROR-2	**RESET ON READ:** This bit enables the counter register to reset upon reading the port event's counter. 0: No effect upon reading the register contents. 1: The counter register is reset by reading the contents of the register.
D5	R/W	FWF-2	**FREEZE WHEN FULL:** This bit controls the freezing of the Event Count registers when the counter is full (FF Hex). 0: No effect on the event count register. 1: Freeze the event count register when the counter is full.
D6	R/W	$\overline{\text{ISAM}}$	**INTERRUPT ON THE SOURCE ADDRESS MISMATCH MASK:** 0: Interrupts will be generated on a source address mismatch mask. ($\overline{\text{RTI}}$ pin becomes active.) 1: No interrupts are generated.
D7	R	res	**RESERVED FOR FUTURE USE:** Reads as a logic 0.

8.0 RIC II Registers (Continued)

INTERRUPT AND MANAGEMENT CONFIGURATION REGISTER (PAGE 0H ADDRESS 16H)

This register powers up with all bits set to one and must be initialized by a processor write cycle before any events will generate interrupts.

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{IFC}$	$\overline{IHC}$	$\overline{ILC}$	$\overline{IFF}$	$\overline{IREC}$	$\overline{ICOL}$	$\overline{IPART}$	MIFCON

Bit	R/W	Symbol	Description
D0	R/W	MIFCON	**MANAGEMENT INTERFACE CONFIGURATION:** 0: All Packets repeated are transmitted over the Management bus. 1: Packets repeated by the RIC II which do not have a Start of Frame Delimiters are not transmitted over the Management bus.
D1	R/W	$\overline{IPART}$	**INTERRUPT ON PARTITION:** 0: Interrupts will be generated ($\overline{RTI}$ pin goes active) if a port becomes Partitioned. 1: No interrupts are generated by this condition.
D2	R/W	$\overline{ICOL}$	**INTERRUPT ON COLLISION:** 0: Interrupts will be generated ($\overline{RTI}$ pin goes active) if this RIC II has a port which experiences a collision, Single RIC II applications, or contains a port which experiences a receive collision or is the first port to suffer a transmit collision in a packet in Multi-RIC II applications. 1: No interrupts are generated by this condition.
D3	R/W	$\overline{IREC}$	**INTERRUPT ON RECEIVE:** 0: Interrupts will be generated ($\overline{RTI}$ pin goes active) if this RIC II contains the receive port for packet or collision activity. 1: No interrupts are generated by this condition.
D4	R/W	$\overline{IFF}$	**INTERRUPT ON FLAG FOUND:** 0: Interrupts will be generated ($\overline{ELI}$ pin goes active) if one or more than one of the flags in the flag array is true. 1: No interrupts are generated by this condition.
D5	R/W	$\overline{ILC}$	**INTERRUPT ON LOW COUNT:** 0: Interrupt generated ($\overline{ELI}$ pin goes active) when one or more of the Event Counters holds a value less than 256 counts. 1: No effect
D6	R/W	$\overline{IHC}$	**INTERRUPT ON HIGH COUNT:** 0: Interrupt generated ($\overline{ELI}$ pin goes active) when one or more of the Event Counters holds a value in excess of 49,152 counts. 1: No effect.
D7	R/W	$\overline{IFC}$	**INTERRUPT ON FULL COUNTER:** 0: Interrupt generated ($\overline{ELI}$ pin goes active) when one or more of the Event Counters is full. 1: No effect.

8.0 RIC II Registers (Continued)

RIC II ADDRESS REGISTER (PAGE 0H ADDRESS 17H)

This register may be used to differentiate between RIC IIs in a multi-RIC II repeater system. The contents of this register form part of the information available through the management bus.

D7	D6	D5	D4	D3	D2	D1	D0
A5	A4	A3	A2	A1	A0	res	res

PACKET COMPRESS DECODE REGISTER (PAGE 0H ADDRESS 18H)

This register is used to determine the number of bytes in the data field of a packet which are transferred over the management bus when the packet compress option is employed. The register bits perform the function of a direct binary decode. Thus up to 255 bytes of data may be transferred over the management bus if packet compression is selected.

D7	D6	D5	D4	D3	D2	D1	D0
PCD7	PCD6	PCD5	PCD4	PCD3	PCD2	PCD1	PCD0

GLOBAL SECURITY REGISTER (GSR) (PAGE 0H ADDRESS 1DH)

This register provides various security configuration options. For instance, enabling learning mode for all the ports; starting address comparison; using the modified packet status register 5 for the management bus; generating random pattern on source address mismatch; disabling port on source address mismatch.

D7	D6	D5	D4	D3	D2	D1	D0
res	GLME	res	DSM	res	MPS	GRP	SAC

Bit	R/W	Symbol	Description
D0	R/W	SAC	**START ADDRESS COMPARISON:** 0: Do not begin comparision. 1: Begin comparison.
D1	R/W	GRP	**GENERATE RANDOM PATTERN:** This bit controls generating the random pattern on a valid source address mismatch. In any event, the Hub Manager will be informed on the SA mismatch. 0: Generate the random pattern. 1: Do not generate the random pattern.
D2	R/W	MPS	**MODIFY PACKET STATUS REGISTER 5:** This bit enables modifying the packet status register 5, PSR5 on the 7 management bytes, over the management bus. 0: Do not modify the PSR5. 1: Modify the PSR5.
D3	R	res	**RESERVED FOR FUTURE USE:** For proper operation, this bit must be 0.
D4	R/W	DSM	**DISABLE THE PORT ON A SOURCE ADDRESS MISMATCH:** 0: Do not disable the port on a valid source address mismatch. 1: Disable the port on a valid source address mismatch.
D5	R	res	**RESERVED FOR FUTURE USE**
D6	R/W	GLME	**GLOBAL LEARN MODE ENABLE:** (Note) 0: Do not enable the learn mode for all ports. 1: Enable the learn mode for all ports.
D7	R	res	**RESERVED FOR FUTURE USE:** Reads as a logic 0.

Note: The GLME is not a status bit. Reading this bit indicates what value was last written to it.

8.0 RIC II Registers (Continued)

INTER FRAME GAP THRESHOLD SELECT REGISTER (PAGE 0H ADDRESS 1FH)

This register is used to configure the hub management interface to provide a certain minimum inter frame gap between packets transmitted over the management bus. The value written to this register, plus one, is the magnitude in bit times of the minimum IFG allowed on the management bus.

D7	D6	D5	D4	D3	D2	D1	D0
IFGT7	IFGT6	IFGT5	IFGT4	IFGT3	IFGT2	IFGT1	IFGT0

PORT EVENT RECORD REGISTERS (PAGE 1H ADDRESS 11H TO 1DH)

These registers hold the recorded events for the specified RIC II port. The flags are cleared when the register is read.

D7	D6	D5	D4	D3	D2	D1	D0
BDLNK	PART	OWC	SE	NSFD	PLER	ELBER	JAB

Bit	R/W	Symbol	Description
D0	R	JAB	**JABBER:** A Jabber Protect event has occurred.
D1	R	ELBER	**ELASTICITY BUFFER ERROR:** A Elasticity Buffer Error has occurred.
D2	R	PLER	**PHASE LOCK ERROR:** A Phase Lock Error event has occurred.
D3	R	NSFD	**NON-SFD:** A Non-SFD packet event has occurred.
D4	R	SE	**SHORT EVENT:** A short event has occurred.
D5	R	OWC	**OUT OF WINDOW COLLISION:** An out of window collision event has occurred.
D6	R	PART	**PARTITION:** A partition event has occurred.
D7	R	BDLNK	**BAD LINK:** A link failure event has occurred.

8.0 RIC II Registers (Continued)

UPPER EVENT INFORMATION REGISTER (UPPER EIR) (PAGE 1H ADDRESS 1EH)

D7	D6	D5	D4	D3	D2	D1	D0
ER8	ER7	ER6	ER5	ER4	ER3	ER2	ER1

Bit	R/W	Symbol	Description
D0	R	ER1	0: Flag found not generated by event on port 1. 1: Flag found generated by event on port 1.
D1	R	ER2	0: Flag found not generated by event on port 2. 1: Flag found generated by event on port 2.
D2	R	ER3	0: Flag found not generated by event on port 3. 1: Flag found generated by event on port 3.
D3	R	ER4	0: Flag found not generated by event on port 4. 1: Flag found generated by event on port 4.
D4	R	ER5	0: Flag found not generated by event on port 5. 1: Flag found generated by event on port 5.
D5	R	ER6	0: Flag found not generated by event on port 6. 1: Flag found generated by event on port 6.
D6	R	ER7	0: Flag found not generated by event on port 7. 1: Flag found generated by event on port 7.
D7	R	ER8	0: Flag found not generated by event on port 8. 1: Flag found generated by event on port 8.

LOWER EVENT INFORMATION REGISTER (LOWER EIR) (PAGE 1H ADDRESS 1FH)

D7	D6	D5	D4	D3	D2	D1	D0
DLU	res	res	ER13	ER12	ER11	ER10	ER9

Bit	R/W	Symbol	Description
D0	R	ER9	0: Flag found not generated by event on port 9. 1: Flag found generated by event on port 9.
D1	R	ER10	0: Flag found not generated by event on port 10. 1: Flag found generated by event on port 10.
D2	R	ER11	0: Flag found not generated by event on port 11. 1: Flag found generated by event on port 11.
D3	R	ER12	0: Flag found not generated by event on port 12. 1: Flag found generated by event on port 12.
D4	R	ER13	0: Flag found not generated by event on port 13. 1: Flag found generated by event on port 13.
D5	R	res	**RESERVED FOR FUTURE USE:** Reads as a logic 0.
D6	R	res	**RESERVED FOR FUTURE USE:** Reads as a logic 0.
D7	R/W	DLU	**DISABLE THE LED UPDATES:** This bit disables the LED display updates for a faster processor register access. 0: Re-enable the LED update cycle (Note). 1: Disable the LED update cycles.

Note: The LED update cycle will be re-enabled only when the network and the RIC II internal state machines are idle.

8.0 RIC II Registers (Continued)

PORT EVENT COUNT REGISTER (PAGES 2H AND 3H)

The Event Count (EC) register shows the instantaneous value of the specified port's 16-bit counter. The counter increments when an enabled event occurs. The counter may be cleared when it is read and prevented from rolling over when the maximum count is reached by setting the appropriate control bits in the Upper Event Count mask register. Since the RIC II's processor port is octal and the counters are 16 bits long a temporary holding register is employed for register reads. When one of the counters is read, either high or low byte first, all 16 bits of the counter are transferred to a holding register. Provided the next read cycle to the counter array accesses the same counter's other byte, then the read cycle accesses the holding register. This avoids the problem of events occurring in between the two processor reads and indicating a false count value. In order to enter a new value to the holding register a different counter must be accessed, or the same counter byte must be re-read.

Lower Byte

D7	D6	D5	D4	D3	D2	D1	D0
EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Upper Byte

D7	D6	D5	D4	D3	D2	D1	D0
EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8

PORT EVENT COUNT REGISTER 2 (PECR-2) (PAGE 4H ADDRESSES 11H TO 1DH)

The Port Event Count Register 2 (PECR-2) shows the instantaneous value of the specified port's 8-bit counter. The counter increments when an enabled event occurs. The counter may be cleared when it is read, and prevented from rolling over when the maximum count is reached, by setting the appropriate control bits in the ECIMR-2 register.

D7	D6	D5	D4	D3	D2	D1	D0
EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

8.0 RIC II Registers (Continued)

PORT SECURITY CONFIGURATION REGISTER (PSCR) (PAGES 4H, 5H, 6H, 8H, 9H)

This register sets up the various security modes for the RIC II. It provides port specific information such as enabling/disabling the security mode, passing broadcast packets, etc. In addition, comparison on destination address, source address, or both can be selected. The system can also qualify learning mode on a per port basis.

Note: Bit D0 is **only** for the port CAMs, and **not** for the shared CAMs.

D7	D6	D5	D4	D3	D2	D1	D0
res	EDA	ESA	SAM	MCE	BCE	SME	LME

Bit	R/W	Symbol	Description
D0	R/W	LME	**LEARNING MODE:** 0: Disable Learn Mode for port CAMs. 1: Enable Learn Mode for port CAMs.
D1	R/W	SME	**SECURITY MODE:** 0: Disable Security Mode. 1: Enable Security Mode.
D2	R/W	BCE	**ACCEPT BROADCAST:** Enables the repeater to pass/repeat a packet with an all 1's destination address (Note 1). 0: Replace the broadcast packets with random packets. 1: Pass broadcast packets.
D3	R/W	MCE	**ACCEPT MULTICAST:** Enables the repeater to pass/repeat a packet with the LSB of ''1'' in the most significant byte of the destination address (Note 2). 0: Replace the multicast packets with random packets. 1: Pass multicast packets.
D4	R	SAM	**SOURCE ADDRESS MATCH/MISMATCH:** 0: Source address match occurred for the packet. 1: Source address mismatch occurred for the packet.
D5	R/W	ESA	**SOURCE ADDRESS SECURITY:** 0: Do not employ source address to implement security. 1: Employ source address to implement security.
D6	R/W	EDA	**DESTINATION ADDRESS SECURITY:** 0: Do not employ destination address to implement security. 1: Employ destination address to implement security.
D7	R	res	**RESERVED FOR FUTURE USE:** Reads as a logic 0.

Note 1: SA mismatch is still valid for broadcast packets.

Note 2: SA mismatch is still valid for multicast packets.

8.0 RIC II Registers (Continued)

PORT CAM POINTER REGISTER (PCPR) (PAGES 4H, 5H, 6H, 8H, 9H)

This register indicates which bytes of the six Ethernet address bytes has been stored in the CAM locations. When a byte has been loaded into the CAM location, the pointer increments. Thus, this register indicates which byte will get written on the subsequent CAM location access. After the complete address is stored in any of the two CAMs, the user must set the ''address valid'', ADV, bit so the address is not overwritten mistakenly. When in learning mode, this register could be read to see if an address has been learned.

D7	D6	D5	D4	D3	D2	D1	D0
ADV	PTR2	PTR1	PTR0	ADV	PTR2	PTR1	PTR0

Bit	R/W	Symbol	Description
D0	R	PTR0	D0 of the pointer for the port CAM location 1.
D1	R	PTR1	D1 of the pointer for the port CAM location 1.
D2	R	PTR2	D2 of the pointer for the port CAM location 1.
D3	R/W	ADV	**ADdress Valid:** 0: Address is not valid in port CAM location 1. 1: Address is valid in port CAM location 1.
D4	R	PTR0	D0 of the pointer for the port CAM location 2.
D5	R	PTR1	D1 of the pointer for the port CAM location 2.
D6	R	PTR2	D2 of the pointer for the port CAM location 2.
D7	R/W	ADV	**ADdress Valid:** 0: Address is not valid in port CAM location 2. 1: Address is valid in port CAM location 2.

PORT CAM REGISTER (PAGES 5H, 6H, 8H, 9H)

This register accesses the 48 bits of the port CAM address. Six write/read cycles are required to load/read the entire 48-bit address.

D7	D6	D5	D4	D3	D2	D1	D0
PCAMx__D7	PCAMx__D6	PCAMx__D5	PCAMx__D4	PCAMx__D3	PCAMx__D2	PCAMx__D1	PCAMx__D0

Bit	R/W	Symbol	Description
D(7:0)	R/W	PCAMx__D(7:0)	This register access the **P**ort **CAM** for the particular port. Note that **x** represents the port number. 1st access: bits [7:0] of the address, 2nd access: bits [15:8] of the address, 3rd access: bits [23:16] of the address, 4th access: bits [31:24] of the address, 5th access: bits [39:32] of the address, 6th access: bits [47:40] of the address.

8.0 RIC II Registers (Continued)

SHARED CAM VALIDATION REGISTER 1 (SCVR 1) (PAGE 9H ADDRESS 16H)

This register indicates the validity of an Ethernet address stored in any one of the shared CAMs. When a ''1'' is written in a specific SCVR, upon starting the network security, the CAM contents will be used for address comparison.

D7	D6	D5	D4	D3	D2	D1	D0
ADV8	ADV7	ADV6	ADV5	ADV4	ADV3	ADV2	ADV1

Bit	R/W	Symbol	Description
D0	R/W	ADV1	**ADdress Valid 1:** 0: Address is not valid in CAM 1. 1: Address is valid in CAM 1.
D1	R/W	ADV2	**ADdress Valid 2:** 0: Address is not valid in CAM 2. 1: Address is valid in CAM 2.
D2	R/W	ADV3	**ADdress Valid 3:** 0: Address is not valid in CAM 3. 1: Address is valid in CAM 3.
D3	R/W	ADV4	**ADdress Valid 4:** 0: Address is not valid in CAM 4. 1: Address is valid in CAM 4.
D4	R/W	ADV5	**ADdress Valid 5:** 0: Address is not valid in CAM 5. 1: Address is valid in CAM 5.
D5	R/W	ADV6	**ADdress Valid 6:** 0: Address is not valid in CAM 6. 1: Address is valid in CAM 6.
D6	R/W	ADV7	**ADdress Valid 7:** 0: Address is not valid in CAM 7. 1: Address is valid in CAM 7.
D7	R/W	ADV8	**ADdress Valid 8:** 0: Address is not valid in CAM 8. 1: Address is valid in CAM 8.

Note: Before writing to and changing any bits in this register, read the register first and then only change the desired bits. By doing this, a previous entry will not be invalidated mistakenly.

8.0 RIC II Registers (Continued)

SHARED CAM VALIDATION REGISTER 2 (SCVR 2) (PAGE 9H, ADDRESS 17H)

This register indicates the validity of an Ethernet address stored in any one of the shared CAMs. When a ''1'' is written in a specific SCVR, upon starting the network security, the CAM contents will be used for address comparison.

D7	D6	5	D4	D3	D2	D1	D0
ADV16	ADV15	ADV14	ADV13	ADV12	ADV11	ADV10	ADV9

Bit	R/W	Symbol	Description
D0	R/W	ADV9	**ADdress Valid 9:** 0: Address is not valid in CAM 9. 1: Address is valid in CAM 9.
D1	R/W	ADV10	**ADdress Valid 10:** 0: Address is not valid in CAM 10. 1: Address is valid in CAM 10.
D2	R/W	ADV11	**ADdress Valid 11:** 0: Address is not valid in CAM 11. 1: Address is valid in CAM 11.
D3	R/W	ADV12	**ADdress Valid 12:** 0: Address is not valid in CAM 12. 1: Address is valid in CAM 12.
D4	R/W	ADV13	**ADdress Valid 13:** 0: Address is not valid in CAM 13. 1: Address is valid in CAM 13.
D5	R/W	ADV14	**ADdress Valid 14:** 0: Address is not valid in CAM 14. 1: Address is valid in CAM 14.
D6	R/W	ADV15	**ADdress Valid 15:** 0: Address is not valid in CAM 15. 1: Address is valid in CAM 15.
D7	R/W	ADV16	**ADdress Valid 16:** 0: Address is not valid in CAM 16. 1: Address is valid in CAM 16.

Note: Before writing to and changing any bits in this register, read the register first and then only change the desired bits. By doing this, a previous entry will not be invalidated mistakenly.

8.0 RIC II Registers (Continued)

SHARED CAM VALIDATION REGISTER 3 (SCVR 3) (PAGE 9H, ADDRESS 18H)

This register indicates the validity of an Ethernet address stored in any one of the shared CAMs. When a ''1'' is written in a specific SCVR, upon starting the network security, the CAM contents will be used for address comparison.

D7	D6	5	D4	D3	D2	D1	D0
ADV24	ADV23	ADV22	ADV21	ADV20	ADV19	ADV18	ADV17

Bit	R/W	Symbol	Description
D0	R/W	ADV17	**ADdress Valid 17:** 0: Address is not valid in CAM 17. 1: Address is valid in CAM 17.
D1	R/W	ADV18	**ADdress Valid 18:** 0: Address is not valid in CAM 18. 1: Address is valid in CAM 18.
D2	R/W	ADV19	**ADdress Valid 19:** 0: Address is not valid in CAM 19. 1: Address is valid in CAM 19.
D3	R/W	ADV20	**ADdress Valid 20:** 0: Address is not valid in CAM 20. 1: Address is valid in CAM 20.
D4	R/W	ADV21	**ADdress Valid 21:** 0: Address is not valid in CAM 21. 1: Address is valid in CAM 21.
D5	R/W	ADV22	**ADdress Valid 22:** 0: Address is not valid in CAM 22. 1: Address is valid in CAM 22.
D6	R/W	ADV23	**ADdress Valid 23:** 0: Address is not valid in CAM 23. 1: Address is valid in CAM 23.
D7	R/W	ADV24	**ADdress Valid 24:** 0: Address is not valid in CAM 24. 1: Address is valid in CAM 24.

Note: Before writing to and changing any bits in this register, read the register first and then only change the desired bits. By doing this, a previous entry will not be invalidated mistakenly.

8.0 RIC II Registers (Continued)

SHARED CAM VALIDATION REGISTER 4 (SCVR 4) (PAGE 9H ADDRESS 19H)

This register indicates the validity of an Ethernet address stored in any one of the shared CAMs. When a ''1'' is written in a specific SCVR, upon starting the network security, the CAM contents will be used for address comparison.

D7	D6	5	D4	D3	D2	D1	D0
ADV32	ADV31	ADV30	ADV29	ADV28	ADV27	ADV26	ADV25

Bit	R/W	Symbol	Description
D0	R/W	ADV25	**ADdress Valid 25:** 0: Address is not valid in CAM 25. 1: Address is valid in CAM 25.
D1	R/W	ADV26	**ADdress Valid 26:** 0: Address is not valid in CAM 26. 1: Address is valid in CAM 26.
D2	R/W	ADV27	**ADdress Valid 27:** 0: Address is not valid in CAM 27. 1: Address is valid in CAM 27.
D3	R/W	ADV28	**ADdress Valid 28:** 0: Address is not valid in CAM 28. 1: Address is valid in CAM 28.
D4	R/W	ADV29	**ADdress Valid 29:** 0: Address is not valid in CAM 29. 1: Address is valid in CAM 29.
D5	R/W	ADV30	**ADdress Valid 30:** 0: Address is not valid in CAM 30. 1: Address is valid in CAM 30.
D6	R/W	ADV31	**ADdress Valid 31:** 0: Address is not valid in CAM 31. 1: Address is valid in CAM 31.
D7	R/W	ADV32	**ADdress Valid 32:** 0: Address is not valid in CAM 32. 1: Address is valid in CAM 32.

Note: Before writing to and changing any bits in this register, read the register first and then only change the desired bits. By doing this, a previous entry will not be invalidated mistakenly.

8.0 RIC II Registers (Continued)

SHARED CAM REGISTER (PAGES 9H, AH, BH, CH, DH, EH, FH)

This register accesses the 48 bits of the shared CAM address. Six write/read cycles are required to load/read the entire 48-bit address.

D7	D6	D5	D4	D3	D2	D1	D0
SCAMx __D7	SCAMx __D6	SCAMx __D5	SCAMx __D4	SCAMx __D3	SCAMx __D2	SCAMx __D1	SCAMx __D0

Bit	R/W	Symbol	Description
D(7:0)	R/W	SCAMx __D(7:0)	This register access the **S**hared **CAM** for the particular port. Note that **x** represents the port number. 1st access: bits [7:0] of the address, 2nd access: bits [15:8] of the address, 3rd access: bits [23:16] of the address, 4th access: bits [31:24] of the address, 5th access: bits [39:32] of the address, 6th access: bits [47:40] of the address.

8.0 RIC II Registers (Continued)

CAM LOCATION MASK REGISTER (CLMR) (PAGES 9H, AH, BH, CH, DH, EH, FH)

Each shared CAM has a CLMR, therefore there are 32 CLMRs. Any of the 32 CAMs can be shared among the ports. For example, multiple ports can share a single ethernet address, or multiple addresses can be associated with a single port. Assigning CAMs to ports, or vice-versa, is done through these registers.

CLMR Lo Byte Location

D7	D6	D5	D4	D3	D2	D1	D0
P8	P7	P6	P5	P4	P3	P2	P1

Bit	R/W	Symbol	Description
D0	R/W	P1	0: CAM entry does not belong to port 1. 1: CAM entry belongs to port 1.
D1	R/W	P2	0: CAM entry does not belong to port 2. 1: CAM entry belongs to port 2.
D2	R/W	P3	0: CAM entry does not belong to port 3. 1: CAM entry belongs to port 3.
D3	R/W	P4	0: CAM entry does not belong to port 4. 1: CAM entry belongs to port 4.
D4	R/W	P5	0: CAM entry does not belong to port 5. 1: CAM entry belongs to port 5.
D5	R/W	P6	0: CAM entry does not belong to port 6. 1: CAM entry belongs to port 6.
D6	R/W	P7	0: CAM entry does not belong to port 7. 1: CAM entry belongs to port 7.
D7	R/W	P8	0: CAM entry does not belong to port 8. 1: CAM entry belongs to port 8.

CLMR Hi Byte Location

D7	D6	D5	D4	D3	D2	D1	D0
PTR2	PTR1	PTR0	P13	P12	P11	P10	P9

Bit	R/W	Symbol	Description
D0	R/W	P9	0: CAM entry does not belong to port 9. 1: CAM entry belongs to port 9.
D1	R/W	P10	0: CAM entry does not belong to port 10. 1: CAM entry belongs to port 10.
D2	R/W	P11	0: CAM entry does not belong to port 11. 1: CAM entry belongs to port 11.
D3	R/W	P12	0: CAM entry does not belong to port 12. 1: CAM entry belongs to port 12.
D4	R/W	P13	0: CAM entry does not belong to port 13. 1: CAM entry belongs to port 13.
D5	R	PTR0	D0 of the pointer into the CAM location.
D6	R	PTR1	D1 of the pointer into the CAM location.
D7	R	PTR2	D2 of the pointer into the CAM location.

9.0 AC and DC Specifications

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	0.5V to 7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} + 0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	2W
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
ESD Rating (R_{zap} = 1.5k, C_{zap} = 120 pF)	1500V

DC Specifications T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

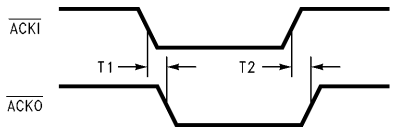
Symbol	Description	Conditions	Min	Max	Units
PROCESSOR, LED, TWISTED PAIR PORTS, INTER-RIC AND MANAGEMENT INTERFACES					
V_{OH}	Minimum High Level Output Voltage	I_{OH} = −8 mA	3.5		V
V_{OL}	Minimum Low Level Output Voltage	I_{OL} = 8 mA		0.4	V
V_{IH}	Minimum High Level Input Voltage		2.0		V
V_{IL}	Maximum Low Level Input Voltage			0.8	V
I_{IN}	Input Current	V_{IN} = V_{CC} or GND	−1.0	1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND	−10	10	μA
I_{CC}	Average Supply Current	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V		380	mA
AUI (PORT 1)					
V_{OD}	Differential Output Voltage (TX±)	78Ω Termination and 270Ω Pulldowns	±550	±1200	mV
V_{OB}	Differential Output Voltage Imbalance (TX±)	78Ω Termination and 270Ω Pulldowns	Typical: 40 mV		
V_U	Undershoot Voltage (TX±)	78Ω Termination and 270Ω Pulldowns	Typical: 80 mV		
V_{DS}	Differential Squelch Threshold (RX±, CD±)		−175	−300	mV
V_{CM}	Differential Input Common Mode Voltage (RX±, CD±) (Note 1)		0	5.5	V
PSEUDO AUI (PORTS 2–13)					
V_{POD}	Differential Output Voltage (TX±)	270Ω Termination and 1 kΩ Pulldowns	±450	±1200	mV
V_{POB}	Differential Output Voltage Imbalance (TX±)	270Ω Termination and 1 kΩ Pulldowns	Typical: 40 mV		
V_{PU}	Undershoot Voltage (TX±)	270Ω Termination and 1 kΩ Pulldowns	Typical: 80 mV		
V_{PDS}	Differential Squelch Threshold (RX±, CD±)		−175	−300	mV
V_{PCM}	Differential Input Common Mode Voltage (Rx±, CD±) (Note 1)		0	5.5	V
TWISTED PAIR (PORTS 2–13)					
V_{RON}	Minimum Receive Squelch Threshold	Normal Mode Reduced Mode	±300 (Note 2)	±585 ±340	mV

Note 1: This parameter is guaranteed by design and is not tested.

Note 2: The operation in Reduced Mode is not guaranteed below 300 mV.

10.0 Timing and Load Diagrams

PORT ARBITRATION TIMING



TL/F/12499–24

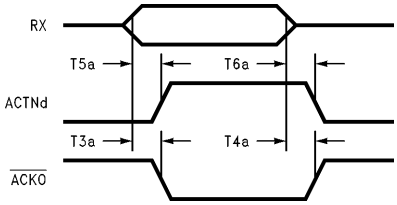
Number	Symbol	Parameter	Min	Max	Units
T1	ackilackol	$\overline{ACKI}$ Low to $\overline{ACKO}$ Low		24	ns
T2	ackihackoh	$\overline{ACKI}$ High to $\overline{ACKO}$ High		21	ns

Note: Timing valid with no receive or collision activities.

Note: In these diagrams the Inter-RIC and Management Busses are shown using active high signals, active low signals may also be used. See Mode Load Operation description.

RECEIVE TIMINGS—AUI PORTS

Receive activity propagation start up and end delays for ports in **non** 10BASE-T mode



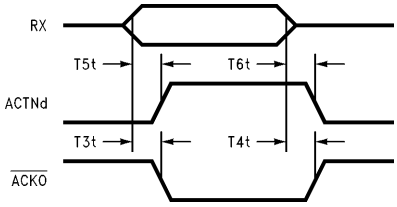
TL/F/12499–25

Number	Symbol	Parameter	Min	Max	Units
T3a	rxaackol	RX Active to $\overline{ACKO}$ Low		66	ns
T4a	rxiackoh	RX Inactive to $\overline{ACKO}$ High		325	ns
T5a	rxaactna	RX Active to ACTNd Active		105	ns
T6a	rxiactni	RX Inactive to ACTNd Inactive		325	ns

Note: $\overline{ACKI}$ assumed high.

RECEIVE TIMING—10BASE-T PORTS

Receive activity propagation start up and end delays for ports in 10BASE-T mode



TL/F/12499–26

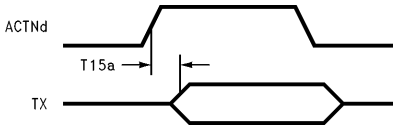
Number	Symbol	Parameter	Min	Max	Units
T3t	rxaackol	RX Active to $\overline{ACKO}$ Low		240	ns
T4t	rxiackoh	RX Inactive to $\overline{ACKO}$ High		255	ns
T5t	rxaactna	RX Active to ACTNd Active		270	ns
T6t	rxiactni	RX Inactive to ACTNd Inactive		265	ns

Note: $\overline{ACKI}$ assumed high.

10.0 Timing and Load Diagrams (Continued)

TRANSMIT TIMING—AUI PORTS

Transmit activity propagation start up and end delays for ports in **non** 10BASE-T mode



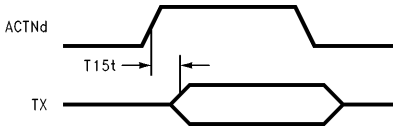
TL/F/12499–27

Number	Symbol	Parameter	Min	Max	Units
T15a	actnatxa	ACTNd Active to TX Active		585	ns

Note: $\overline{\text{ACKI}}$ assumed high.

TRANSMIT TIMING—10BASE-T PORTS

Receive activity propagation start up and end delays for ports in 10BASE-T mode



TL/F/12499–28

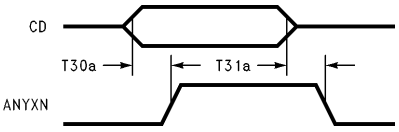
Number	Symbol	Parameter	Min	Max	Units
T15t	actnatxa	ACTNd Active to TX Active		790	ns

Note: $\overline{\text{ACKI}}$ assumed high.

COLLISION TIMING—AUI PORTS

Collision activity propagation start up and end delays for ports in **non** 10BASE-T mode

TRANSMIT COLLISION TIMING



TL/F/12499–29

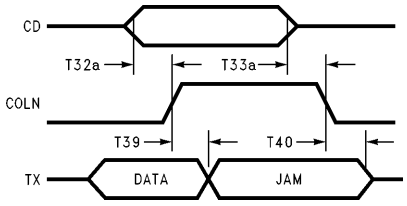
Number	Symbol	Parameter	Min	Max	Units
T30a	cdaanyxna	CD Active to ANYXN Active		65	ns
T31a	cdianyxni	CD Inactive to ANYXN Inactive (Notes 1, 2)		400	ns

Note 1: TX collision extension has already been performed and no other port is driving ANYXN.

Note 2: Includes TW2.

10.0 Timing and Load Diagrams (Continued)

RECEIVE COLLISION TIMING



TL/F/12499–30

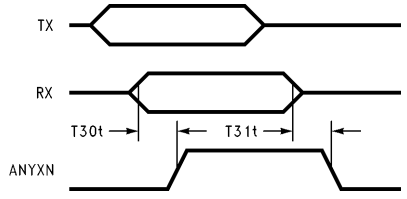
Number	Symbol	Parameter	Min	Max	Units
T32a	cdacolna	CD Active to COLN Active (Note 1)		55	ns
T33a	cdicolni	CD Inactive to COLN Inactive		215	ns
T39	colnajs	COLN Active to Start of Jam		400	ns
T40	colnije	COLN Inactive to End of Jam (Note 2)		800	ns

Note 1: PKEN assumed high.

Note 2: Assuming reception ended before COLN goes inactive. TW2 is included in this parameter. Assuming ACTNd to ACTNs delay is 0.

COLLISION TIMING—10BASE-T PORTS

Collision activity propagation start up and end delays for ports in 10BASE-T mode



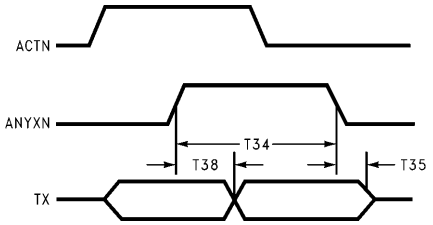
TL/F/12499–31

Number	Symbol	Parameter	Min	Max	Units
T30t	colaanya	Collision Active to ANYXN Active		800	ns
T31t	colianyi	Collision Inactive to ANYXN Inactive (Note 1)		400	ns

Note 1: TX collision extension has already been performed and no other port is asserting ANYXN.

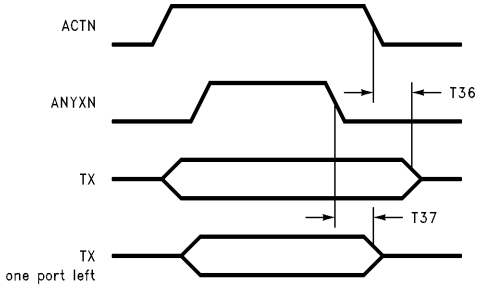
10.0 Timing and Load Diagrams (Continued)

COLLISION TIMING—AUI PORTS



TL/F/12499–32

Number	Symbol	Parameter	Min	Max	Units
T34	anyamin	ANYXN Active Time	96		Bits
T35	anyitxai	ANYXN Inactive to TX to all Inactive	120	170	ns
T38	anyasj	ANYXN Active to Start of Jam		400	ns

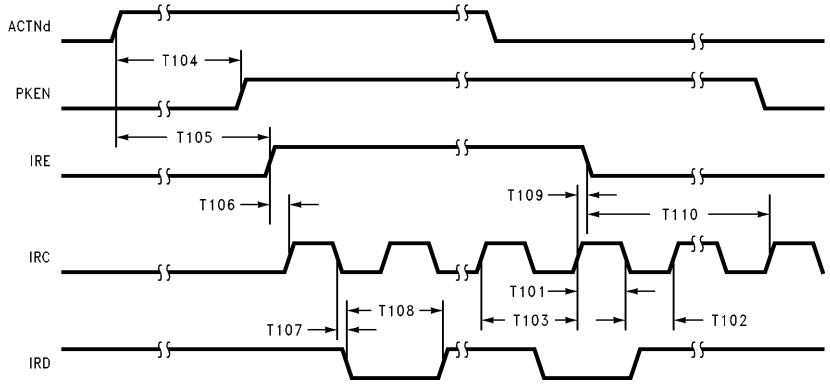


TL/F/12499–33

Number	Symbol	Parameter	Min	Max	Units
T36	actnitxi	ACTN Inactive to TX Inactive		405	ns
T37	anyitxoi	ANYXN Inactive to TX ‘‘One Port Left’’ Inactive	120	170	ns

10.0 Timing and Load Diagrams (Continued)

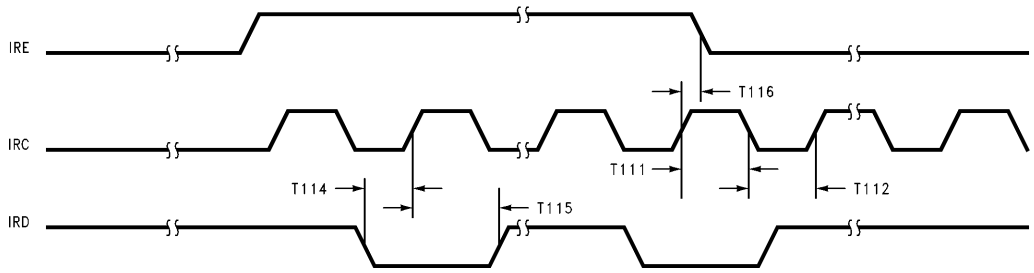
INTER RIC BUS OUTPUT TIMING



TL/F/12499–34

Number	Symbol	Parameter	Min	Max	Units
T101	ircoh	IRC Output High Time	45	55	ns
T102	ircol	IRC Output Low Time	45	55	ns
T103	ircoc	IRC Output Cycle Time	90	110	ns
T104	actndapkena	ACTNd Active to PKEN Active	555		ns
T105	actndairea	ACTNd Active to IRE Active	560		ns
T106	ireairca	IRE Output Active to IRC Active		1.8	μs
T107	irdov	IRD Output Valid from IRC		10	ns
T108	irdos	IRD Output Stable Valid Time	90		ns
T109	ircohirei	IRC Output High to IRE Inactive	30	70	ns
T110	ircclks	Number of IRCs after IRE Inactive	5		clks

INTER RIC BUS INPUT TIMING

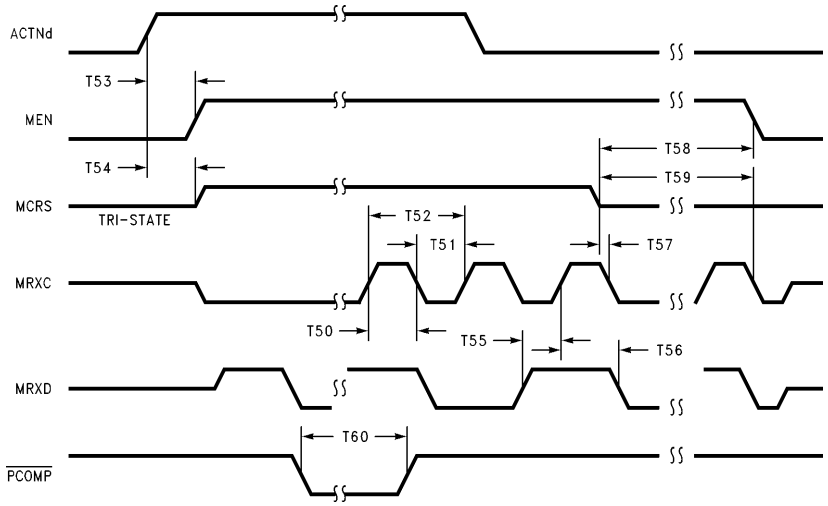


TL/F/12499–35

Number	Symbol	Parameter	Min	Max	Units
T111	ircih	IRC Input High Time	20		ns
T112	ircil	IRC Input Low Time	20		ns
T114	irdisirc	IRD Input Setup to IRC	5		ns
T115	irdihirc	IRD Input Hold from IRC	10		ns
T116	irchirei	IRC Input High to IRE Inactive	10	90	ns

10.0 Timing and Load Diagrams (Continued)

MANAGEMENT BUS TIMING



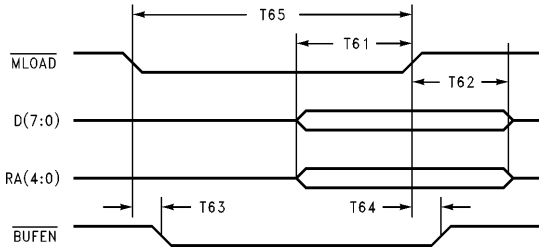
TL/F/12499–36

Number	Symbol	Parameter	Min	Max	Units
T50	mrxch	MRXC High Time	45	55	ns
T51	mrxcl	MRXC Low Time	45	55	ns
T52	mrxcd	MRXC Cycle Time	90	110	ns
T53	actndamena	ACTNd Active to MEN Active		715	ns
T54	actndamcrsa	ACTNd Active to MCRS Active		720	ns
T55	mrxds	MRXD Setup	40		ns
T56	mrxdh	MRXD Hold	45		ns
T57	mrxclmcrsi	MRXC Low to MCRS Inactive	−5	6	ns
T58	mcrsimenl	MCRS Inactive to MEN Low		510	ns
T59	mrxcclks	Min Number of MRXCs after MCRS Inactive	5	5	clks
T60	pcompw	PCOMP Pulse Width	20		ns

Note: The preamble on this bus consists of the following string; 01011.

10.0 Timing and Load Diagrams (Continued)

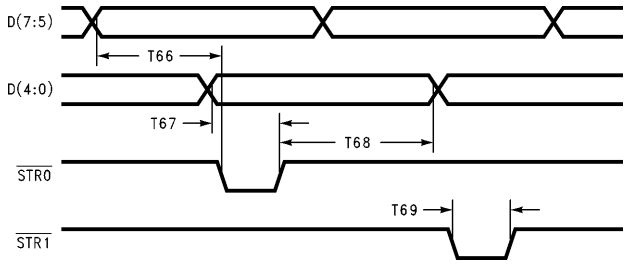
MLOAD TIMING



TL/F/12499–37

Number	Symbol	Parameter	Min	Max	Units
T61	mldats	Data Setup	10		ns
T62	mldath	Data Hold	10		ns
T63	mlabufa	MLOAD Active to BUFEN Active		35	ns
T64	mlibufi	MLOAD Inactive to BUFEN Inactive		35	ns
T65	mlw	MLOAD Width	800		ns

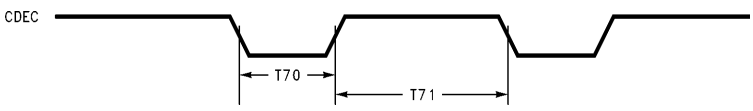
STROBE TIMING



TL/F/12499–38

Number	Symbol	Parameter	Min	Max	Units
T66	stradrs	Strobe Address Setup	80	115	ns
T67	strdats	Strobe Data Setup	40	65	ns
T68	strdath	Strobe Data Hold	135	160	ns
T69	strw	Strobe Width	30	65	ns

CDEC TIMING

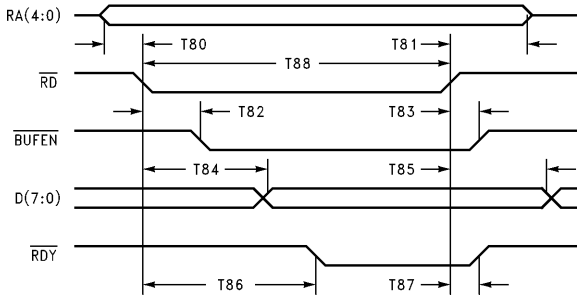


TL/F/12499–39

Number	Symbol	Parameter	Min	Max	Units
T70	cdecpw	CDEC Pulse Width	20	100	ns
T71	cdeccdec	CDEC to CDEC Width	200		ns

10.0 Timing and Load Diagrams (Continued)

REGISTER READ TIMING



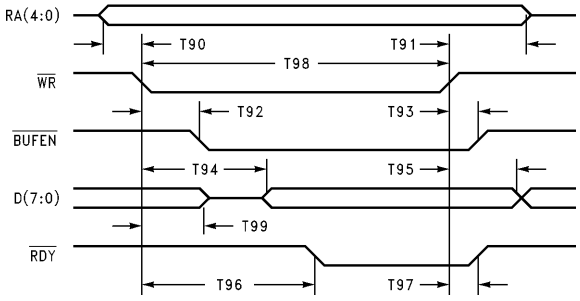
TL/F/12499–40

Number	Symbol	Parameter	Min	Max	Units
T80	rdadrs	Read Address Setup	0		ns
T81	rdadrh	Read Address Hold	0		ns
T82	rdabufa	Read Active to $\overline{\text{BUFEN}}$ Active	95	345	ns
T83	rdibufi	Read Inactive to $\overline{\text{BUFEN}}$ Inactive		35	ns
T84	rdadatv	Read Active to Data Valid	245		ns
T85	rddath	Read Data Hold	75		ns
T86	rdardya	Read Active to $\overline{\text{RDY}}$ Active	340	585	ns
T87	rdirdyi	Read Inactive to $\overline{\text{RDY}}$ Inactive		30	ns
T88	rdw	Read Width	600		ns

Note: Minimum high time between read/write cycles is 100 ns.

10.0 Timing and Load Diagrams (Continued)

REGISTER WRITE TIMING



TL/F/12499–41

Number	Symbol	Parameter	Min	Max	Units
T90	wradrs	Write Address Setup	0		ns
T91	wradrh	Write Address Hold	0		ns
T92	wrabufa	Write Active to $\overline{\text{BUFEN}}$ Active	95	355	ns
T93	wribufi	Write Inactive to $\overline{\text{BUFEN}}$ Inactive		35	ns
T94	wradatv	Write Active to Data Valid		275	ns
T95	wrdath	Write Data Hold	0		ns
T96	wrardya	Write Active to $\overline{\text{RDY}}$ Active	340	585	ns
T97	wrirdyi	Write Inactive to $\overline{\text{RDY}}$ Inactive		30	ns
T98	wrw	Write Width	600		ns
T99	wradt	Write Active to Data TRI-STATE		350	ns

Note: Assuming zero propagation delay on external buffer.

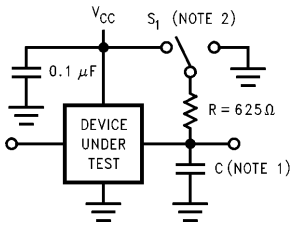
Note: Minimum high time between read/write cycles is 100 ns.

11.0 AC Timing Test Conditions

All specifications are valid only if the mandatory isolation is employed and all differential signals are taken to be at the AUI side of the pulse transformer.

Input Pulse Levels (TTL/CMOS)	GND to 3.0V
Input Rise and Fall Times (TTL/CMOS)	5 ns
Input and Output Reference Levels (TTL/CMOS)	1.5V
Input Pulse Levels (Diff.)	2.0 V_{P-P}
Input and Output Reference Levels (Diff.)	50% Point of the Differential
TRI-STATE Reference Levels	Float (ΔV) $\pm$0.5V

Output Load (See *Figure* Below)



TL/F/12499–42

Note 1: 100 pF, includes scope and jig capacitance.

Note 2: S1 = Open for timing tests for push pull outputs.

S1 = V_{CC} for V_{OL} test.

S1 = GND for V_{OH} test.

S1 = V_{CC} for High Impedance to active low and active low to High Impedance measurements.

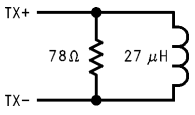
S1 = GND for High Impedance to active high and active high to High Impedance measurements.

Capacitance T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ	Units
C_{IN}	Input Capacitance	7	pF
C_{OUT}	Output Capacitance	7	pF

DERATING FACTOR

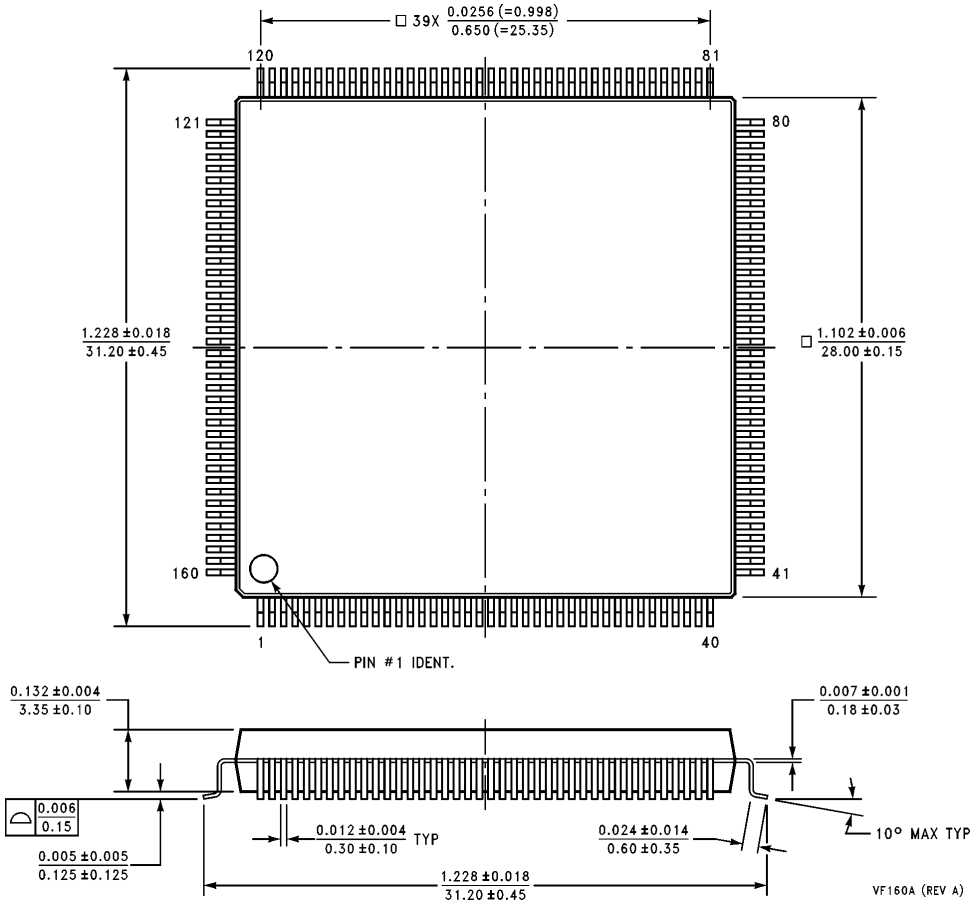
Output timings are measured with a purely capacitive load for 50 pF. The following correction factor can be used for other loads: $C_L \geq 50$ pF + 0.3 ns/pF.



TL/F/12499–43

Note: In the above diagram, the TX+ and TX− signals are taken from the AUI side of the isolation (pulse transformer). The pulse transformer used for all testing is the Pulse Engineering PE64103.

Physical Dimensions inches (millimeters)



160-Lead Plastic Quad Flatpak, EIAJ
NS Package Number VF160A

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