N a t i o n a l   S e m i c o n d u c t o r

CLC5958
14-bit, 52MSPS A/D Converter

General Description

The CLC5958 is a monolithic 14-bit, 52MSPS analog-to-digital converter. The ultra-wide dynamic range and high sample rate of the device make it an excellent choice for wideband receivers found in multi-channel basestations. The CLC5958 integrates a low distortion track-and-hold amplifier and a 14-bit multi-stage quantizer on a single die. Other features include differential analog inputs, low jitter differential clock inputs, an internal bandgap voltage reference, and CMOS/TTL compatible outputs. The CLC5958 is fabricated on the National ABIC-V 0.8 micron BiCMOS process.

The CLC5958 features a 90dB spurious free dynamic range (SFDR) and a 70dB signal to noise ratio (SNR). The balanced differential analog inputs ensure low even-order distortion, while the differential clock inputs permit the use of balanced clock signals to minimize clock jitter. The 48-pin CSP package provides an extremely small footprint for applications where space is a critical consideration. The package also provides a very low thermal resistance to ambient. The CLC5958 may be operated with a single +5V power supply. Alternatively, an additional supply may be used to program the digital output levels over the range of +3.3V to +5V. Operation over the industrial temperature range of -40°C to +85°C is guaranteed. National Semiconductor tests each part to verify compliance with the guaranteed specifications.
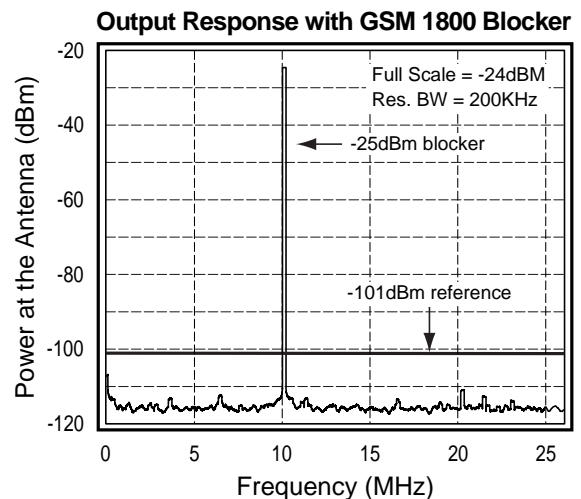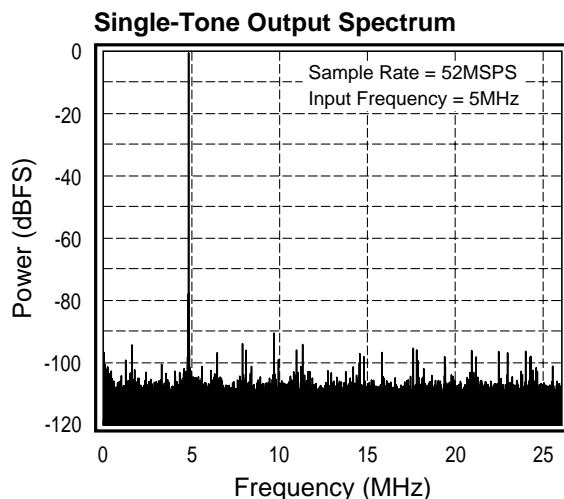
Features
- 14-bit
- 52MSPS
- Ultra-wide dynamic range
    Noise floor: -72dBFS
    SFDR: 90dB
- Excellent performance to Nyquist
- IF sampling capability
- Very small package: 48-pin CSP
- Programmable output levels:
    3.3V to 5V

Applications
- Multi-channel basestations
- Multi-standard basestations:
    GSM, WCDMA, DAMPS, etc.
- Smart antenna systems
- Wireless local loop
- Wideband digital communications

**Actual Size
(Bottom View)**

Single-Tone Output Spectrum

Output Response with GSM 1800 Blocker

CLC5958 Electrical Characteristics (V_{cc}= +5V, DV_{cc}= +3.3V, 52MSPS; unless specified, T_{min} = -40°C, T_{max} = +85°C)

PARAMETERS	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS	NOTES
RESOLUTION		Full		14		Bits	1
DIFF. INPUT VOLTAGE RANGE		Full		2.048		V	
MAXIMUM CONVERSION RATE		Full	52	65		MSPS	1
SNR	f_{in} = 5MHZ, A_{in} = -0.6dBFS	+25°C	TBD	70		dB	1
SFDR	f_{in} = 5MHZ, A_{in} = -0.6dBFS	+25°C	TBD	90		dB	1
SFDR EXCLUDING 2nd & 3rd HARM.	f_{in} = 5MHZ, A_{in} = -0.6dBFS	+25°C	TBD	92		dB	1
NO MISSING CODES	f_{in} = 5MHZ, A_{in} = -0.6dBFS	+25°C	Guaranteed				1
NOISE AND DISTORTION							2
noise floor							
f_{in} = 5MHz	A_{in} = -1dBFS	+25°C		-70.5		dBFS	
f_{in} = 5MHz	A_{in} = -20dBFS	+25°C		-72.0		dBFS	
2nd & 3rd harmonic distortion (w/o dither)							
f_{in} = 5MHz	A_{in} = -1dBFS	+25°C		-90		dBFS	
f_{in} = 20MHz	A_{in} = -1dBFS	+25°C		-87		dBFS	
f_{in} = 70MHz	A_{in} = -3dBFS	+25°C		-78		dBFS	
next worst harmonic distortion (w/o dither)							3
f_{in} = 5MHz	A_{in} = -1dBFS	+25°C		-92		dBFS	
f_{in} = 20MHz	A_{in} = -1dBFS	+25°C		-90		dBFS	
f_{in} = 70MHz	A_{in} = -3dBFS	+25°C		-90		dBFS	
worst harmonic distortion (with dither)							4
f_{in} = 5MHz	A_{in} = -6dBFS	+25°C		-95		dBFS	
f_{in} = 20MHz	A_{in} = -6dBFS	+25°C		-95		dBFS	
f_{in} = 70MHz	A_{in} = -6dBFS	+25°C		-82		dBFS	
f_{in} = 70MHz (2nd & 3rd excluded)	A_{in} = -6dBFS	+25°C		-95		dBFS	
2-Tone IM distortion (w/o dither)							
f_{in1} =12MHz, f_{in2} = 15MHz	A_{in1} = A_{in2} = -7dBFS	+25°C		-100		dBFS	
SINAD (w/o dither)							
f_{in} = 5MHz	A_{in} = -1dBFS	+25°C		69		dB	
CLOCK RELATED SPURIOUS TONES							
fs/8, fs/4		+25°C		-95		dBFS	
next worst clock spur		+25°C		-100		dBFS	5
calibration sideband coefficient		+25°C		100e-6			6
DC ACCURACY AND PERFORMANCE							
differential non-linearity		+25°C		±0.3		LSB	
integral non-linearity		+25°C		±1.5		LSB	
offset error		+25°C		±2.0		mV	
gain error		+25°C		2		% of FS	
DYNAMIC PERFORMANCE							
large-signal bandwidth		+25°C		210		MHz	
aperture jitter		+25°C		0.5		ps(rms)	
TIMING							
effective aperture delay (t_A)		+25°C		-0.2		ns	
pipeline delay (t_P)		Full		3		clk cycle	
output buffer delay (t_o)		+25°C		6.6		ns	
data valid buffer delay (t_{DAV})		+25°C		6.6		ns	
ANALOG INPUT CHARACTERISTICS							
single-ended input resistance		+25°C		500		Ω	
single-ended capacitance		+25°C		3.6		pF	
ENCODE INPUT CHARACTERISTICS							
VIH		Full	3.9		4.5	V	7
VIL		Full	3.0		3.8	V	7
differential input swing		Full	0.2			V	
IIL		Full		2		µA	
IIH		Full		25		µA	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.
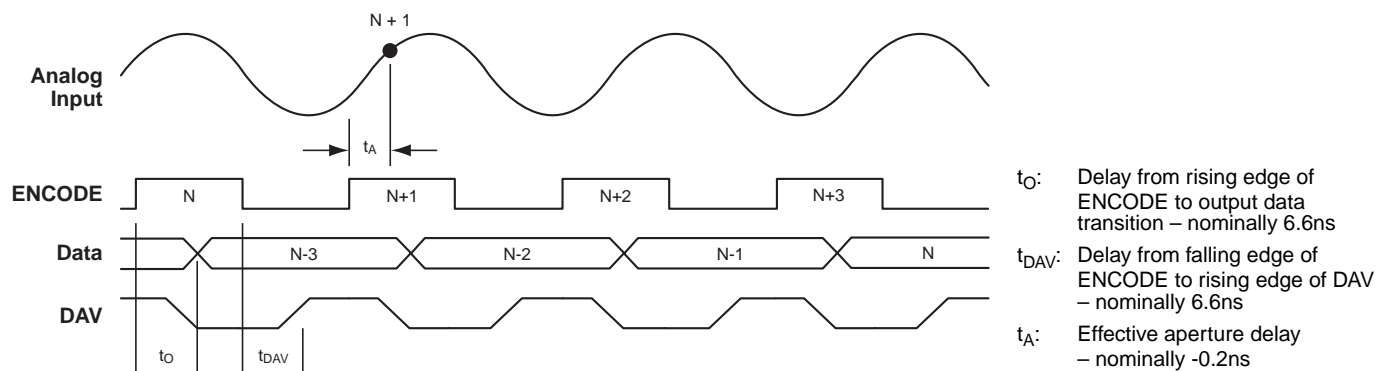
CLC5958 Electrical Characteristics (V_{cc}= +5V, DV_{cc}= +3.3V, 52MSPS; unless specified, T_{min} = -40°C, T_{max} = +85°C)

PARAMETERS	CONDITIONS	TEMP	RATINGS			UNITS	NOTES
			MIN	TYP	MAX		
DIGITAL OUTPUT CHARACTERISTICS							
VOH	IOH = 50µA	Full	3.2			V	
VOL	IOL = 50µA	Full			0.1	V	
SUPPLY CHARACTERISTICS							
+5V supply current (V_{CC})		+25°C		245	TBD	mA	1
+3.3V supply current (DV_{CC})		+25°C		32	TBD	mA	1
power dissipation		+25°C		1.33	TBD	W	1
V_{CC} power supply rejection ratio		+25°C		0.75		mV/V	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes

1) These parameters are 100% tested at 25°C.
2) Harmonics and clock spurious are removed in noise measurements.
3) 4th or higher harmonic.
4) Low frequency dither injected in the DC to 500KHz band.
5) Next worst clock spur is a subharmonic of fs, but not fs/8 or fs/4. See text on spurious.

6) See text on calibration sidebands in the application information section.
7) Encode levels are referenced to V_{CC}, i.e. the minimum VIH value is 1.1V below V_{CC}, and the maximum VIH value is 0.5V below V_{CC}.

t_O: Delay from rising edge of ENCODE to output data transition – nominally 6.6ns

t_{DAV}: Delay from falling edge of ENCODE to rising edge of DAV – nominally 6.6ns

t_A: Effective aperture delay – nominally -0.2ns

CLC5958 Timing Diagram

Absolute Maximum Ratings

positive supply voltage	(V_{CC}) -0.5V to +6V
differential voltage between any two grounds	<200mV
analog input voltage range	GND to V_{CC}
digital input voltage range	-0.5V to +V_{CC}
output short circuit duration (one-pin to ground)	infinite
junction temperature	175°C
storage temperature range	-65°C to 150°C
lead solder duration (+240°C)	5sec

Note: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Recommended Operating Conditions

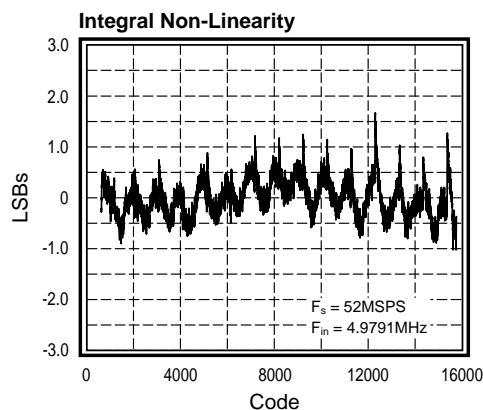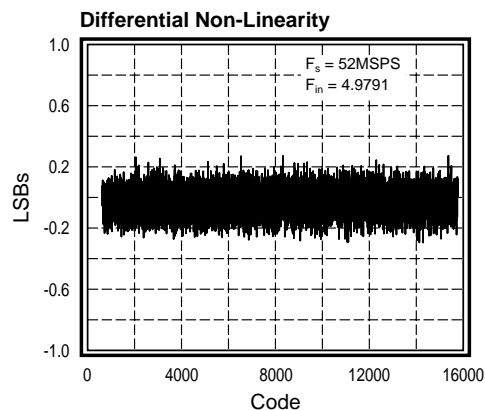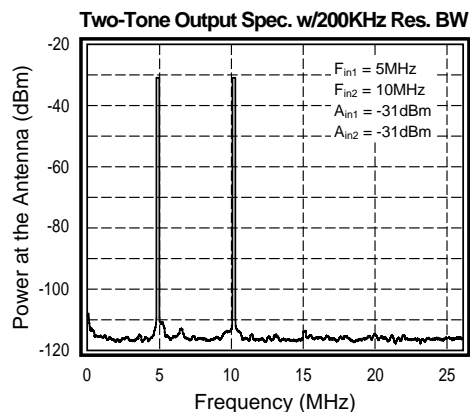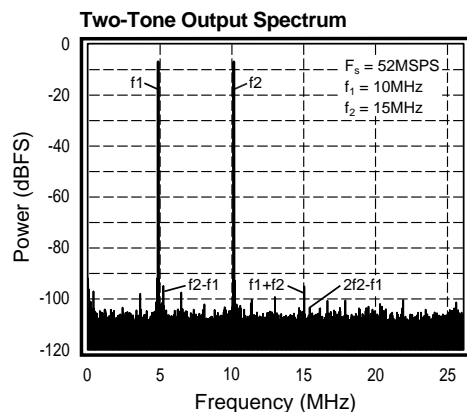|	
positive supply voltage (V_{CC})	+5V ±5%
analog input voltage range	2.048V_{pp} diff.
input coupling	AC
operating temperature range	-40°C to +85°C
digital output supply voltage (DV_{CC})	+3.3V ±5%
analog input common mode voltage (V_{cm})	+3.25 ±0.025V

Package Thermal Resistance

Package	θ_{JA}	θ_{JC}
48-pin CSP	39°C/W	5°C/W

Package Transistor Count

Transistor count	10,000

Ordering Information

Model	Temperature Range	Description
CLC5958SLB CLC5958PCASM	-40°C to +85°C	48-pin CSP (industrial temperature range) Fully loaded evaluation board with CLC5958 … ready for test.
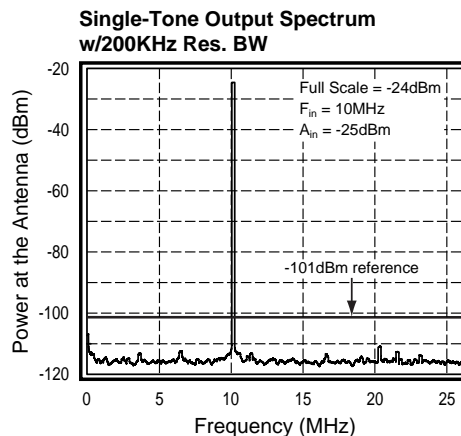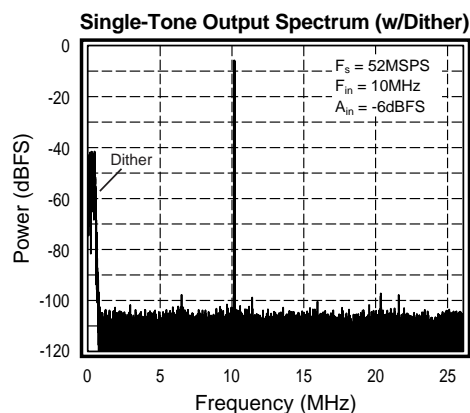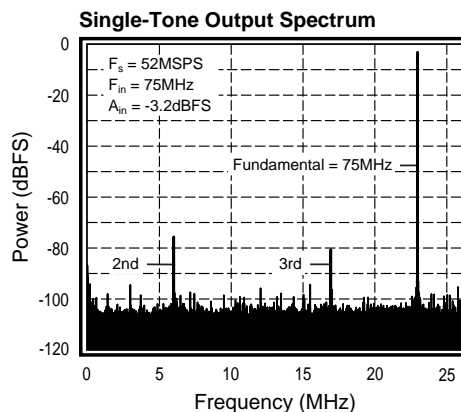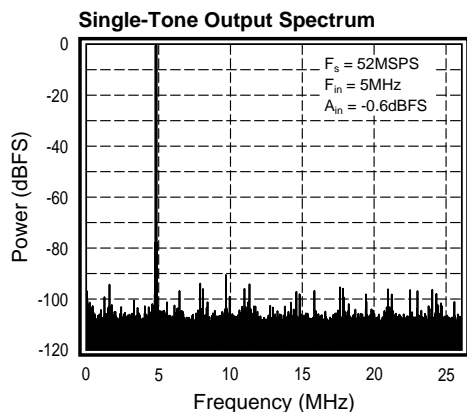
# CLC5958 Typical Performance Characteristics $(V_{CC}= +5V, 52MSPS; unless specified)$

Single-Tone Output Spectrum

F_s = 52MSPS
F_{in} = 5MHz
A_{in} = -0.6dBFS

Single-Tone Output Spectrum

F_s = 52MSPS
F_{in} = 75MHz
A_{in} = -3.2dBFS

Fundamental = 75MHz

2nd   3rd

Single-Tone Output Spectrum (w/Dither)

F_s = 52MSPS
F_{in} = 10MHz
A_{in} = -6dBFS

Dither

**Single-Tone Output Spectrum
w/200KHz Res. BW**

Full Scale = -24dBm
F_{in} = 10MHz
A_{in} = -25dBm

-101dBm reference

Two-Tone Output Spectrum

F_s = 52MSPS
f_1 = 10MHz
f_2 = 15MHz

f1   f2

f2-f1   f1+f2   2f2-f1

Two-Tone Output Spec. w/200KHz Res. BW

F_{in1} = 5MHz
F_{in2} = 10MHz
A_{in1} = -31dBm
A_{in2} = -31dBm

Differential Non-Linearity

F_s = 52MSPS
F_{in} = 4.9791

Integral Non-Linearity

F_s = 52MSPS
F_{in} = 4.9791MHz

**Noise and Spurious
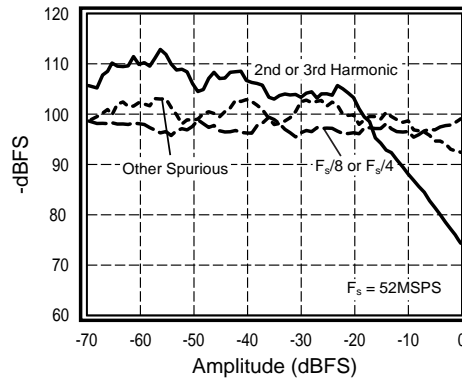vs. Amplitude at F_{in} = 10MHz**

**Spurious vs. Amplitude
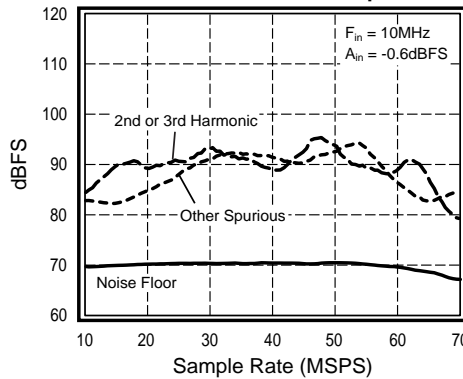with Dither at F_{in} = 10MHz**
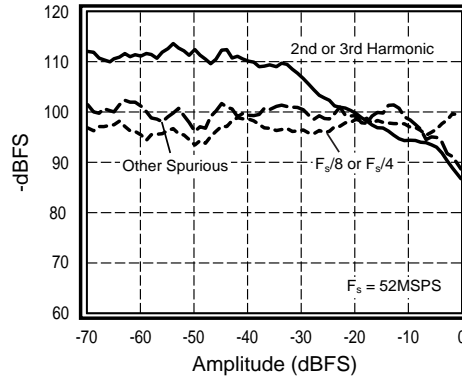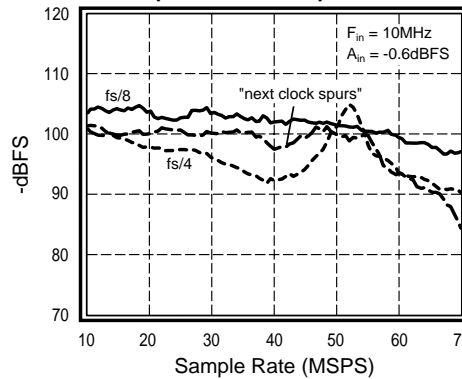

**Noise and Spurious
vs. Amplitude at F_{in} = 75MHz**
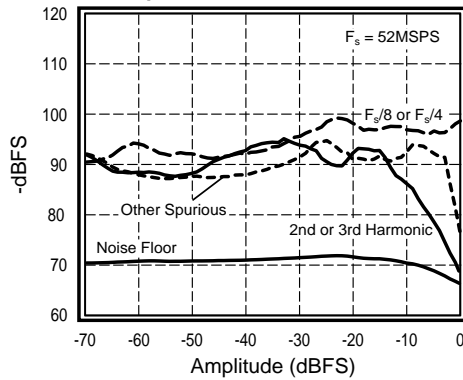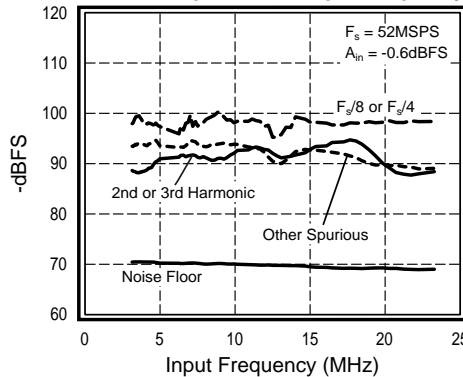

**Spurious vs. Amplitude
with Dither at F_{in} = 75MHz**
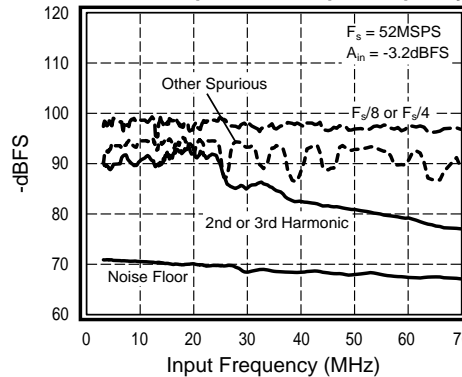

Noise and Distortion vs. Sample Rate

Clock Spurious vs. Sample Rate

Noise and Spurious vs. Input Frequency

Noise and Spurious vs. Input Frequency

5

CLC5958 Pin Definitions

```
 1  GND                              GND  48
 2  GND                              GND  47
 3  GND  ◎                           V_CC 46
 4  GND        CLC5958      (MSB) D13 45
 5  V_CC                             D12  44
 6  V_CC                             D11  43
 7  V_CC                             D10  42
 8  GND                              D9   41
 9  ENCODE                           D8   40
10  ENCODE                           D7   39
11  GND                              DV_CC 38
12  GND                              DV_CC 37
13  A_IN                             GND  36
14  A_IN                             GND  35
15  GND                              D6   34
16  V_CC                             D5   33
17  V_CC        vias                 D4   32
18  V_CC                             D3   31
19  GND                              D2   30
20  GND                              D1   29
21  V_CM                     (LSB) DO 28
22  V_CC                             DAV  27
23  GND                              GND  26
24  GND                              GND  25
```

A_{IN}, $\overline{A_{IN}}$ — (Pins 13, 14) Differential inputs. Self biased at a common mode voltage of +3.25V. The ADC full scale input is 2.048V_{pp} differential.

ENCODE, $\overline{ENCODE}$ — (Pins 9, 10) Differential clock inputs. ENCODE initiates a new data conversion cycle on each rising edge. Clock signals may be sinusoidal or square waves with PECL encode levels. The falling edge of ENCODE clocks internal pipeline stages.

D0-$\overline{D13}$ — (Pins 28 - 34, 39 - 45) Digital data outputs. CMOS and TTL compatible. D0 is the LSB and $\overline{D13}$ is the inverted MSB. Output coding is two's complement.

DAV — (Pin 27) Data valid. The rising edge of this signal occurs when output data is valid and may be used to latch data into following circuitry.

V_{CM} — (Pin 21) Internal analog input common mode voltage reference. Nominally +3.25V. Can be used to establish the analog input common mode voltage for DC coupled applications (DC coupling not recommended, see applications section).

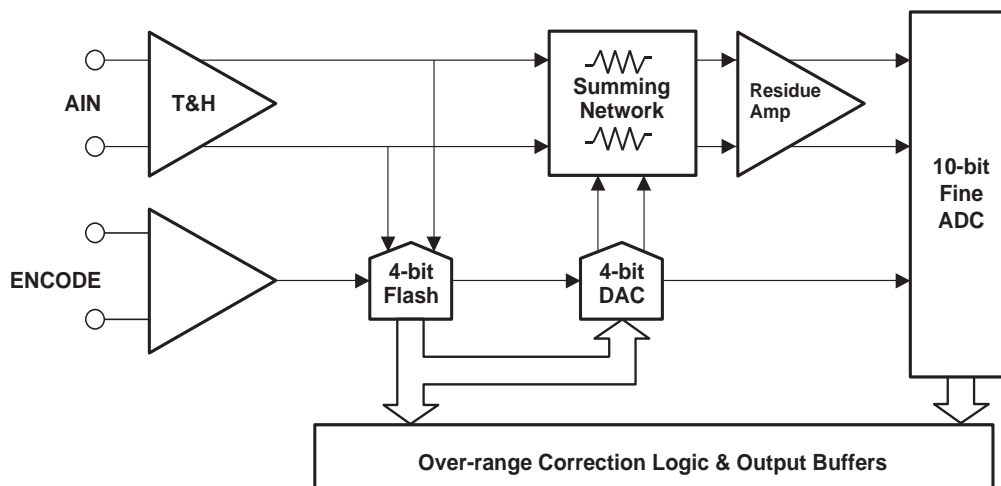**GND** — (Pins 1 - 4, 8, 11, 12, 15, 19, 20, 23 - 26, 35, 36, 47, 48, and vias) circuit ground.

V_{CC} — (Pins 5 - 7, 16 - 18, 22, 46) +5V power supply. Bypass each group of supply pins to ground with a 0.01μF capacitor.

DV_{CC} — (Pins 37, 38) +3.3V to +5V power supply for the digital outputs. Establishes the high output level for the digital outputs. Bypass to ground with a 0.1μF capacitor.

CLC5958 Block Diagram

DIMENSIONS ARE IN MILLIMETERS

RECOMMENDED LAND PATTERN
1:1 RATIO WITH PACKAGE SOLDER PADS

PIN 1 ID

PIN 1 INDEX AREA

Driving the Analog Inputs

The differential analog inputs, AIN and $\overline{\text{AIN}}$, are biased from an internal 3.25V reference (a 2.4V bandgap reference plus a diode) through an on-chip resistance of 500Ω. This bias voltage is set for optimum performance, and varies with temperature. Since DC coupling the inputs overrides the internal common mode voltage, it is recommended that the inputs to the CLC5958 be AC coupled whenever possible. The time constant of the input coupling network must be greater than 1μsec to minimize distortion due to nonlinear input bias currents. Additionally, the common mode source impedance should be less than 100Ω at the sample rate.

If DC coupling is required, then the V_{CM} output may be used to establish the input common mode voltage. The CLC5958 samples the common mode voltage at the internal track-and-hold output and servos the V_{CM} output to establish the optimum common mode potential at the track-and-hold. It is possible to use the V_{CM} output to construct an external servo loop.

Figure 1 below illustrates one input coupling method. The transformer provides noiseless single-ended to differential conversion. The two 50Ω resistors in the secondary define the input impedance and provide a low common mode source impedance through the bypass capacitors.
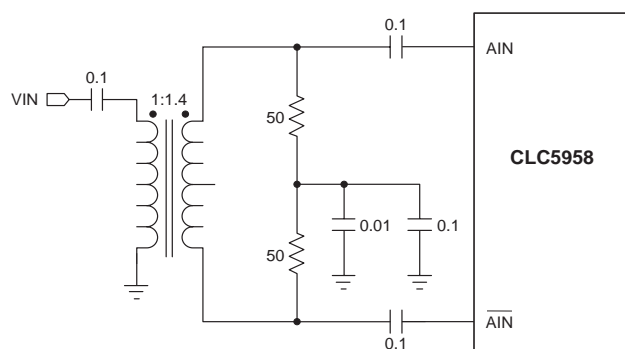

Figure 1: Input Coupling

Alternatively, the inputs can be driven using a differential amplifier as shown in Figure 2.

The network of Figure 2 uses a simple RC low-pass filter to roll off the noise of the differential amplifier. The network has a cutoff frequency of 40MHz. Different noise filter designs are required for different applications. For example, an IF application would require a band-pass noise filter.

The analog input lines should be routed close together so that any coupling from other sources is common mode.
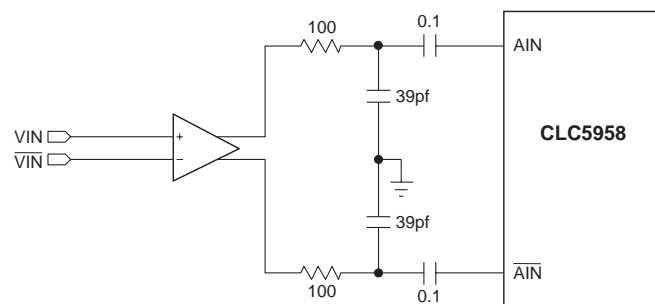

Figure 2: Differential Amplifier

Driving the ENCODE Inputs

The ENCODE and $\overline{\text{ENCODE}}$ inputs are differential clock inputs that are referenced to V_{CC}. They may be driven with PECL input levels. Alternatively they may be driven with a differential input (e.g. a sine input) that is centered at 1.2 Volts below V_{CC} and which meets the min and max ratings for V_{IL} and V_{IH}. Low noise differential clock signals provide the best SNR performance for the converter.

The ENCODE inputs are not self biasing, so a DC bias current path must be provided to each of the inputs.

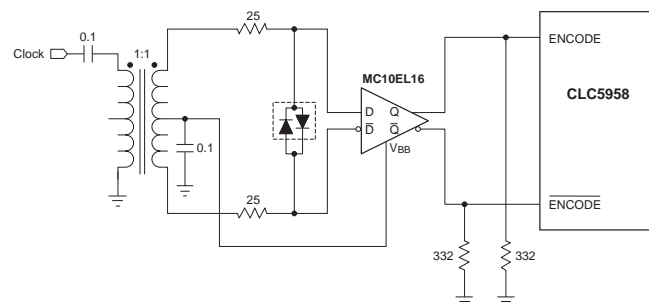Figure 3 shows one method of driving the encode inputs.

Figure 3: ENCODE Inputs

The transformer converts the single-ended clock signal to a differential signal. The center-tap of the secondary is biased by the V_{BB} potential of the ECL buffer. The diodes in the secondary limit the input swing to the buffer.

Since the encode inputs are close to the analog inputs, it is recommended that the analog inputs be routed on the top of the board directly over a ground plane and that the encode lines be routed on the back of the board and then connected through via to the encode inputs.

Latching the Output Data

The rising edge of DAV is approximately centered in the data transition window, and may be used to latch the output data. The DAV output has twice the load driving capability of the data outputs so that two latch clock inputs may be driven by this output.

Routing Output Data Lines

It is recommended that the ground plane be removed under the data output lines to minimize the capacitive loading of these lines. In some systems this may not be permissible because of EMI considerations.

Harmonics and Clock Spurious

Harmonics are created by non-linearity in the track-and-hold and the quantizer. Harmonics that arise from repetitive non-linearities in the quantizer may be reduced by the application of a dither signal.

Transformers and baluns can contribute harmonic distortion, particularly at low frequencies where transformer operation relies on magnetic flux in the core. If a transformer is used to perform single-ended to differential conversion at the input, care should be taken in the selection of the transformer.

The clock is internally divided by the CLC5958 in order to generate internal control signals. These divided clocks can contribute spurious energy, principally at $f_s/4$ and $f_s/8$. The clock spurious is typically less than -90dBFS.

Calibration Sidebands

The CLC5958 incorporates on-board calibration. The calibration process creates low level sideband spurious close to the carrier and near DC for some input frequencies. In most applications these sidebands will not be an issue. The sidebands add negligible power to the carrier and therefore do not reduce sensitivity in receiver applications. Also, the sidebands never fall in adjacent channels with any appreciable power. They may be visible in some very narrow-band applications, and so are documented here for completeness.

The offset of the sidebands relative to the carrier and relative to DC is derived using the equations:

$$n = round\left(\frac{32\,f_{in}}{f_s}\right) \qquad f_\Delta = \left|f_{in} - \frac{nf_s}{32}\right|$$

where $f\Delta$ is the sideband offset, f_{in} is the input frequency, f_s is the sample rate, and round($\bullet$) denotes integer rounding. The magnitude of the sideband relative to the carrier for a full scale input tone is approximated by the equations:

$$x = 1024\,\pi f_\Delta\,/\,f_s \qquad a_\Delta = \alpha\left|\frac{\sin(x)}{x}\right|$$

where a_Δ is the sideband magnitude relative to the input, and α is the calibration sideband coefficient. The value of α rolls off 2dB per dB as the input amplitude is reduced.

For example, assume the input frequency is 4.8671MHz and the sample rate is 52MSPS. Then the sideband offset is derived as follows:

$$n = round\left(\frac{32 * 4.8671e^6}{52e^6}\right) = 3$$

$$f_\Delta = \left|4.8671e^6 - \frac{3 * 52e^6}{32}\right| = 7.9KHz$$

If the input is a full scale input, then the magnitude of the sidebands is derived as:

$$x = 1024\,\pi\,7.9e^3\,/\,52e^6 = 0.489$$

$$a_\Delta = 100e^{-6} * \left|\frac{\sin(.489)}{.489}\right| = 96e^{-6} = -80dBc$$

The sidebands roll off rapidly with increasing sideband offset. For example, if the sideband is offset 200KHz from the carrier (in an adjacent GSM channel) as opposed to the 7.9KHz offset from the previous example, the sideband magnitude is reduced to -116dBc.

Figure 4 shows how the sideband offset frequency varies with input frequency at a sample rate of 52MSPS.
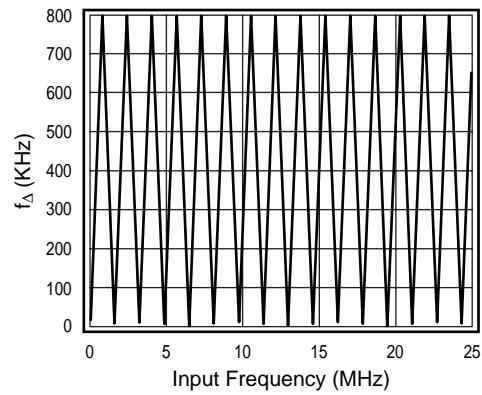

Figure 4: Sideband Offset vs. Input Frequency

The sideband magnitude is a function of the sideband offset, as illustrated in Figure 5.
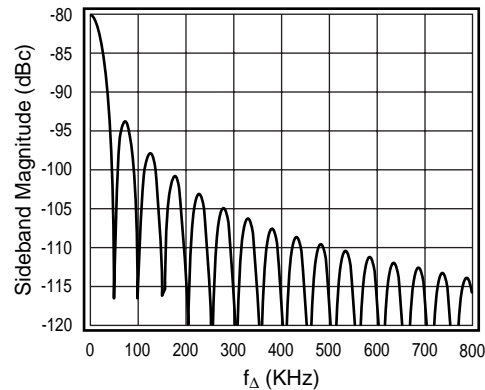

Figure 5: Sideband Magnitude vs. Sideband Offset

Power Supplies

The V_{CC} pins supply power to all of the CLC5958 circuitry with the exception of the digital output buffers. The DV_{CC} pins provide power to the digital output buffers. Each supply pin should be connected to a supply (i.e. do not leave any supply pins floating).

Local groups of supply pins should be bypassed with .01uF capacitors. These capacitors should be placed as close to the part as possible. Avoid using via to the ground plane. If vias to the ground plane cannot be avoided, then use multiple vias in close proximity to the bypass capacitor.

The supplies should be bypassed in a manner to prevent supply return currents from flowing near the analog inputs. The evaluation board layout is an example of how to accomplish this.

The digital output buffer supplies (DV_{CC}) provide a means for programming the output buffer high level. Supply values ranging from 3.3V to 5.0V may be applied to these pins. In general, best performance is achieved with DV_{CC} set to 3.3V.

Layout Recommendations for the CSP

The 48 lead chip scale package not only provides a small footprint, but also provides an excellent connection to ground. The thermal vias on the bottom of the package also serve as additional ground pads. The solder pad dimensions on the pc board should match the package pads 1:1.

Soldering Recommendations for the CSP

A 4 mil thick stencil for the solder screen printing is recommended. The suggested IR reflow profile is:

Ramp Up:	2°/sec
Dwell Time > 183°C:	75 sec
Solder Temperature:	215°C
(max solder temperature):	235°C
Dwell Time @ Max Temp:	5 sec
Ramp Down:	2°C/sec

CLC5958 Evaluation Board

Description

The CLC5958 evaluation printed circuit board provides a convenient test bed for rapid evaluation of the CLC5958. It illustrates the proper approach to layout in order to achieve best performance, and provides a performance benchmark.

Analog Input

The CLC5958 evaluation board is configured to be driven by a single-ended signal at the AIN SMA connector (the $\overline{AIN}$ connector is disconnected). The AIN SMA connector should be driven from a 50Ω source impedance. A full scale input is approximately 1.4V_{pp} (7dBm). The single-ended input is converted to a differential input by an on-board transformer.

When performing sine wave testing, it is critical that the input sine wave be filtered to remove harmonics and source noise.

Encode Input

The CLK SMA connector is the encode input and should also be driven from a 50Ω source. A low jitter 16dBm sine wave should be applied at this input. In some cases it may be necessary to band-pass filter the sine wave in order to achieve low jitter.

The single-ended clock input is converted to a differential signal by an on-board transformer and buffered by an ECL buffer.

Digital Outputs

The digital outputs are available at the Eurocard connector (J1). Data bits D0 through $\overline{D13}$ are available at J1 pins 18B through 5B. The data ready signal (labeled DR in the schematic) is available at J1 pin 20B. These outputs are also available at the HP 01650-63203 termination adapter for direct connection to an HP logic analyzer (see evaluation board schematic). The outputs are buffered by 3.3V digital latches. The falling edge of the data ready signal may be used to latch the output data.

Supply Voltages

Power is sourced to the board through the Eurocard connector. A 5V supply should be connected at J1 pins 32A and 32B. A 3.3V supply should be connected at J1 pins 31A and 31 B. The ground return for these supplies is at J1 pins 27A, 27B, 28A, and 28B. It is recommended that low noise linear supplies be used.
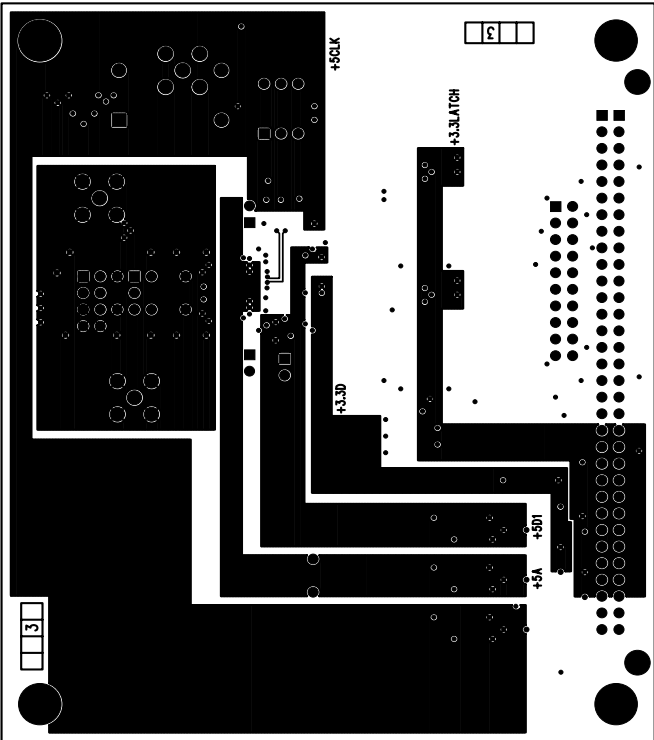
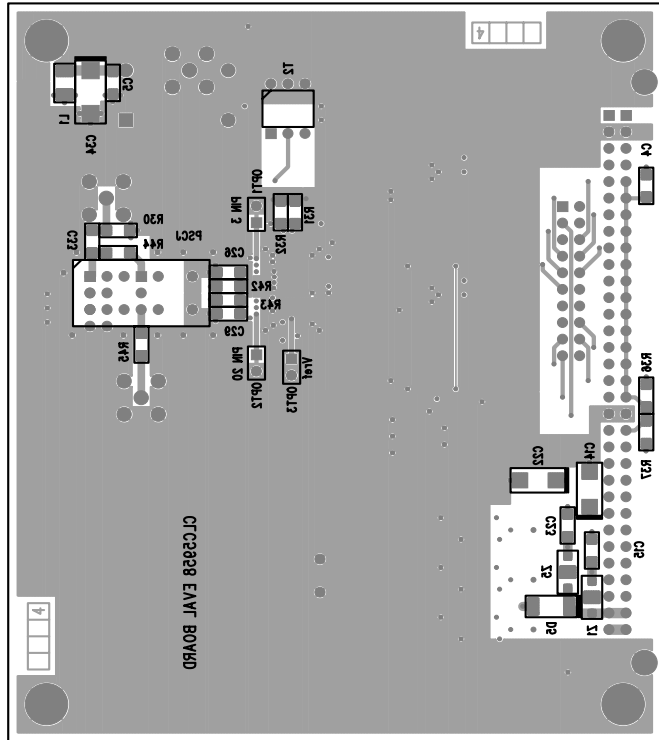# CLC5958 Evaluation Board Layout
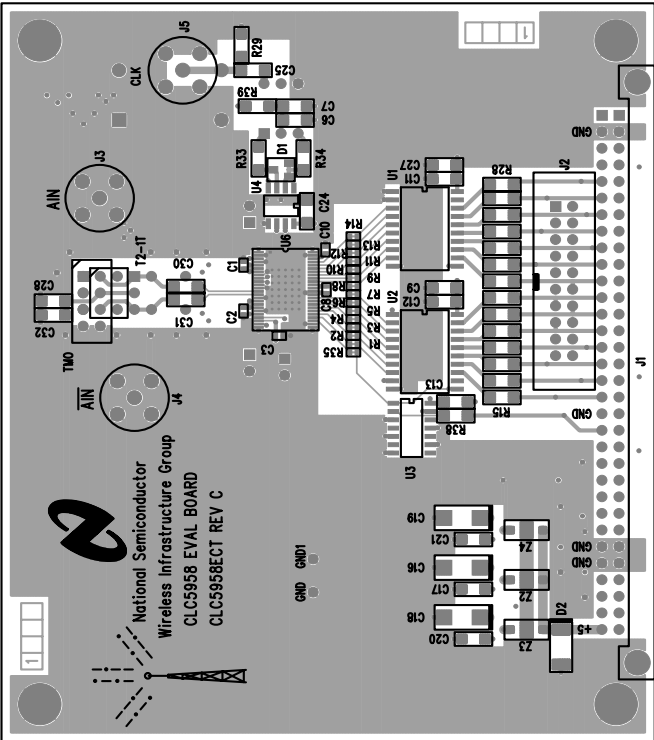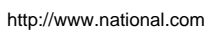

CLC5958PCASM Layer 1
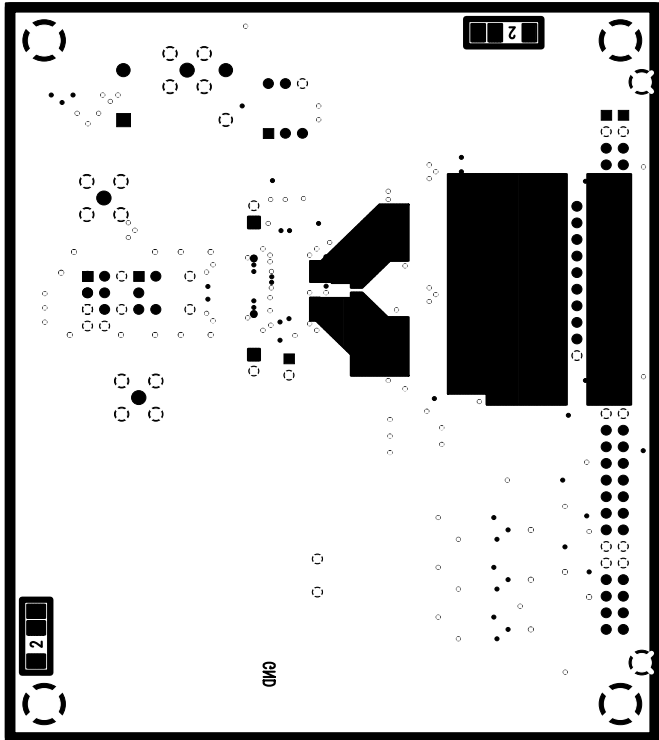
CLC5958PCASM Layer 2

CLC5958PCASM Layer 3

CLC5958PCASM Layer 4

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