National Semiconductor

CLC5956
12-bit, 65MSPS Broadband Monolithic A/D Converter

General Description

The CLC5956 is a monolithic 12-bit, 65MSPS analog-to-digital converter subsystem. The device has been optimized for use in cellular base stations and other applications where high resolution, high sampling rate, wide dynamic range, low power dissipation, and compact size are required. The CLC5956 features differential analog inputs, low jitter differential PECL clock inputs, a low distortion track-and-hold with 0-300MHz input bandwidth, a bandgap voltage reference, TTL compatible CMOS output logic, and a proprietary 12-bit multi-stage quantizer. The CLC5956 is fabricated on the ABIC-IV 0.8 micron BiCMOS process. The part features a 73dB spurious free dynamic range (SFDR) and 67dB SNR. The wideband track-and-hold allows sampling of IF signals to greater than 250MHz. The part produces two-tone, dithered, spurious-free dynamic range of 83dBFS at 75MHz input frequency. The differential analog input provides excellent common-mode-rejection, while the differential PECL clock inputs permit the use of balanced transmission to minimize jitter in distributed systems. The 48-pin TSSOP package provides an extremely small footprint for applications where space is a critical consideration. The CLC5956 operates from single +5V power supply. The CLC5956 operates over the industrial temperature range of -40 to +85°C. National thoroughly tests each part to verify full compliance with the guaranteed specifications.

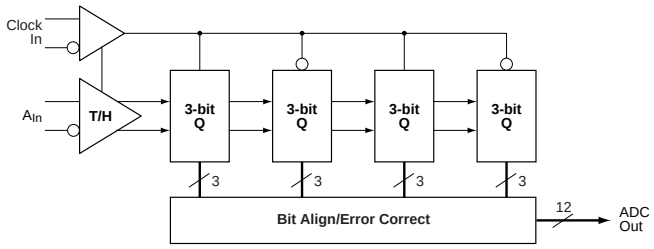
Features

- 65MSPS
- Wide dynamic range
  SFDR: 73dBc
  SFDR w/dither: 85dBFS
  SNR: 67dB
- IF sampling capability
- Input bandwidth = 0-300MHz
- Low power dissipation: 615mW
- Very small package: 48-pin TSSOP
- Single +5V supply
- Low cost

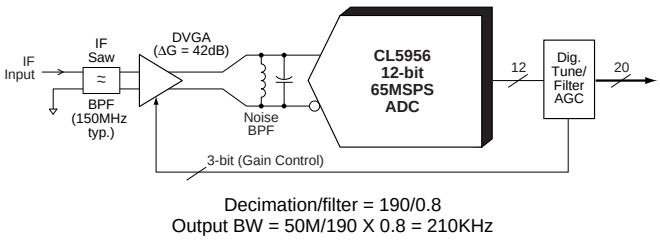
Applications

- Cellular base-stations
- Digital communications
- Infrared/CCD imaging
- IF sampling
- Electro-optics
- Instrumentation
- Medical imaging
- High definition video

Actual Size

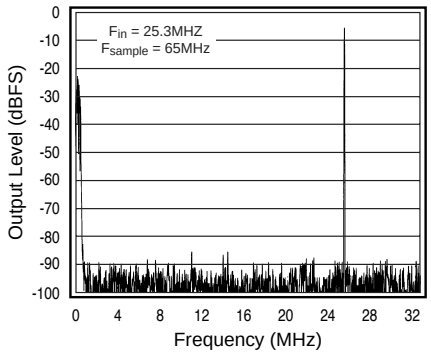


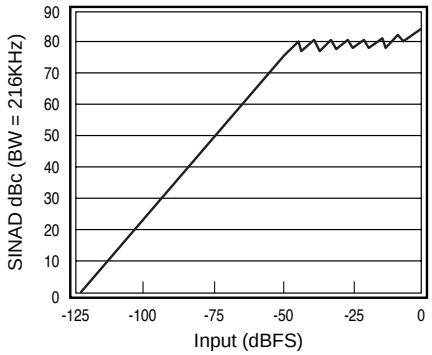
ADC Block Diagram



Decimation/filter = 190/0.8
Output BW = 50M/190 X 0.8 = 210KHz

Single IF Down Converter





CLC5956 Electrical Characteristics (V_{cc}= +5V, 52MSPS; unless specified) (T_{min} = -40°C, T_{max} = +85°C)

PARAMETERS	CONDITIONS	TEMP	RATINGS			UNITS	NOTES
			MIN	TYP	MAX		2
DYNAMIC PERFORMANCE							
large-signal bandwidth	V_{in} = FS-3dB	+25°C		300		MHz	
overvoltage recovery time	V_{in} = 1.5FS (0.01%)	+25°C		12		ns	
effective aperture delay		+25°C		-0.21		ns	
aperture jitter		+25°C		0.4		ps(rms)	
NOISE AND DISTORTION (52MSPS)							
signal-to-noise ratio (w/o harmonics)							
20MHz	FS-1dB	+25°C	63	66		dBFS	1
5.0MHz	FS-3dB	+25°C		67		dBFS	
25MHz	FS-3dB	+25°C		66		dBFS	
75MHz	FS-3dB	+25°C		64		dBFS	
150MHz	FS-3dB	+25°C		62		dBFS	
250MHz	FS-3dB	+25°C		59		dBFS	
spurious-free dynamic range							
20MHz	FS-1dB	+25°C	66	70		dBc	1
5.0MHz	FS-3dB	+25°C		73		dBc	
25MHz	FS-3dB	+25°C		70		dBc	
75MHz	FS-3dB	+25°C		68		dBc	
150MHz	FS-3dB	+25°C		58		dBc	
250MHz	FS-3dB	+25°C		55		dBc	
intermodulation distortion							
149.84MHz (f_1), 149.7MHz (f_2)	FS-10dB	+25°C		68		dBFS	
249.86MHz (f_1), 249.69MHz (f_2)	FS-10dB	+25°C		58		dBFS	
dithered performance							
spurious-free dynamic range							
19MHz	FS-6dB	+25°C		85		dBFS	
intermodulation distortion							
74MHz (f_1), 75MHz (f_2)	FS-12dB	+25°C		83		dBFS	
DC ACCURACY AND PERFORMANCE							
differential non-linearity	DC; FS	+25°C		0.65		LSB	
integral non-linearity	DC; FS	+25°C		1.7		LSB	
bipolar offset error		+25°C		-1		mV	
bipolar gain error		+25°C		-0.1		%FS	
ANALOG INPUTS							
analog differential input voltage range		+25°C		2.048		V_{pp}	
analog input resistance (single ended)		+25°C		500		Ω	
analog input resistance (differential)		+25°C		1000		Ω	
analog input capacitance		+25°C		2		pF	
ENCODE INPUTS							
input voltage	logic LOW	Full	3.0		3.5	V	1
	logic HIGH	Full	4.0		4.5	V	1
input current	logic LOW	Full		1	5	µA	1
	logic HIGH	Full		16	25	µA	1
DIGITAL OUTPUTS							
output voltage	logic LOW	Full			0.4	V	1
	logic HIGH	Full	2.4			V	1
TIMING							
maximum conversion rate		+25°C		65		MSPS	
minimum conversion rate		Fulll		10		MSPS	
pulse width high		Full		7.7		ns	
pulse width low		Full		7.7		ns	
pipeline delay		Full			3.0	clk cycle	
output propagation delay		+25°C		1.6		ns	
POWER REQUIREMENTS							
+5V supply current	65MSPS	+25°C		123	150	mA	1
power dissipation	65MSPS	+25°C		615	750	mW	1
V_{CC} power supply rejection ratio		+25°C		64		dB	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes

1) These parameters are 100% tested at 25°C.

2) Typical specifications are the mean values of the distributions of deliverable converters tested to date.

Absolute Maximum Ratings

positive supply voltage (V_{cc})	-0.5V to +6V
differential voltage between any two grounds	<200mV
analog input voltage range	GND to V_{cc}
digital input voltage range	-0.5V to +V_{cc}
output short circuit duration (one-pin to ground)	infinite
junction temperature	175°C
storage temperature range	-65°C to 150°C
lead solder duration (+300°C)	10sec

Note: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Recommended Operating Conditions

positive supply voltage (V_{cc})	+5V ±5%
analog input voltage range	2.048V_{pp} diff.
operating temperature range	-40°C to +85°C

Package Thermal Resistance

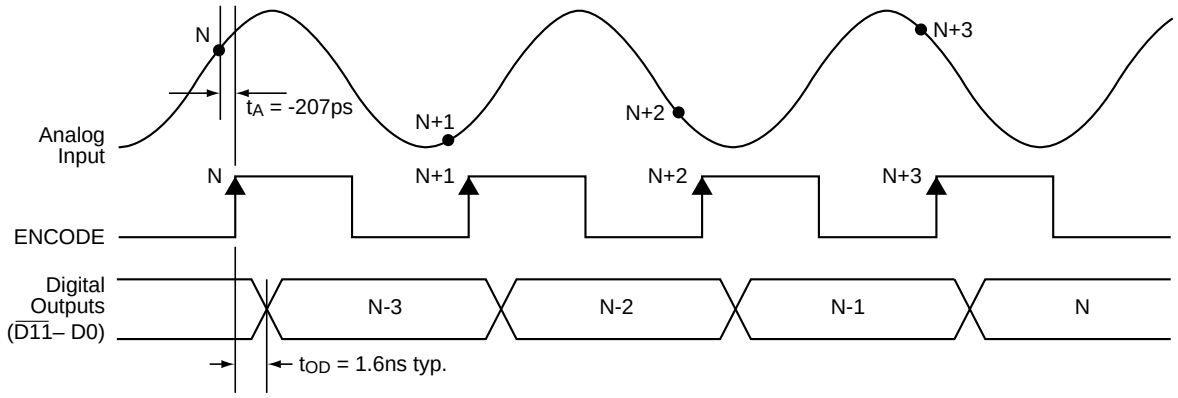
Package	θ_{JA}	θ_{JC}
48-pin TSSOP	56°C/W	16°C/W

Reliability Information

Transistor count	5000

Ordering Information

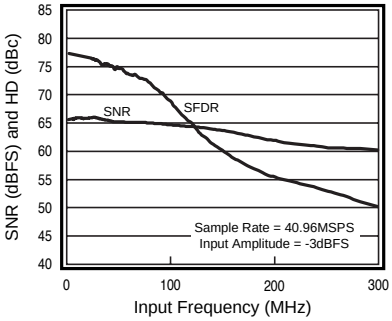
Model	Temperature Range	Description
CLC5956IMTD	-40°C to +85°C	48-pin TSSOP (industrial part)
CLC5956IMTDX	-40°C to +85°C	48-pin TSSOP (TNR 1000 pc reel)
CLC5956PCASM		Fully loaded evaluation board with CLC5956 … ready for test.



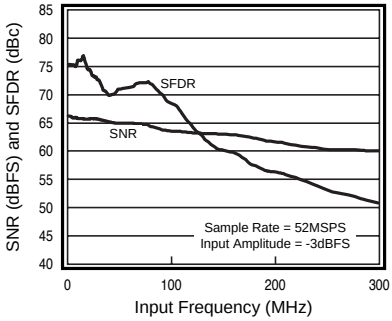
CLC5956 Timing Diagram

CLC5956 Typical Performance Characteristics (V_{CC} = +5V)

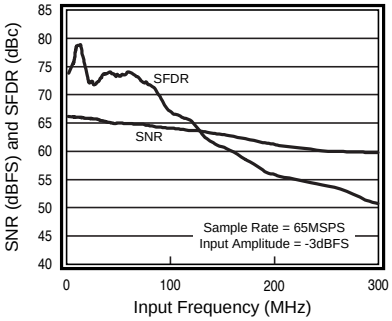
SNR and SFDR vs. Input Frequency



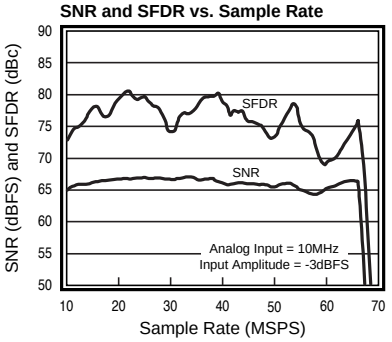
SNR and SFDR vs. Input Frequency



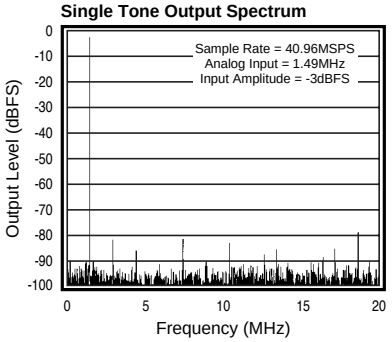
SNR and SFDR vs. Input Frequency



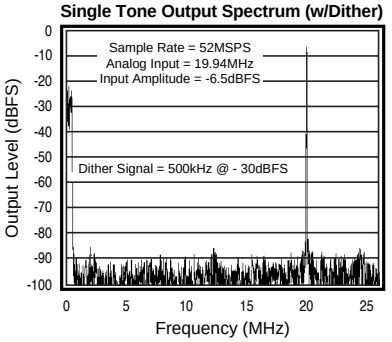
SNR and SFDR vs. Sample Rate



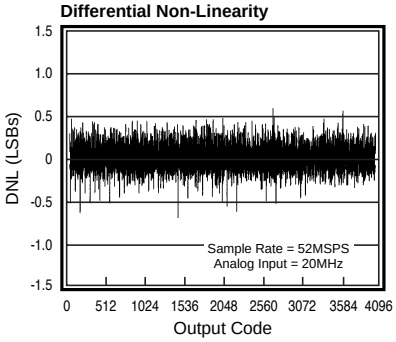
Single Tone Output Spectrum



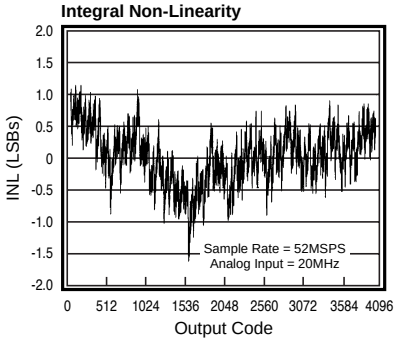
Single Tone Output Spectrum (w/Dither)



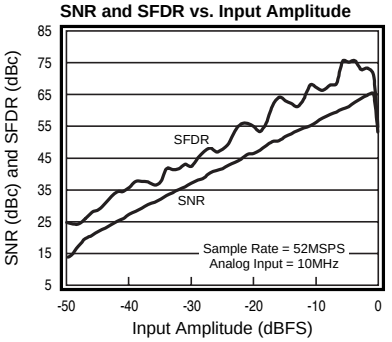
Differential Non-Linearity



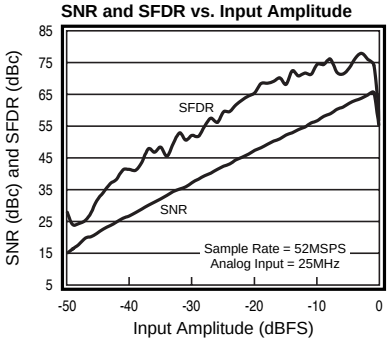
Integral Non-Linearity



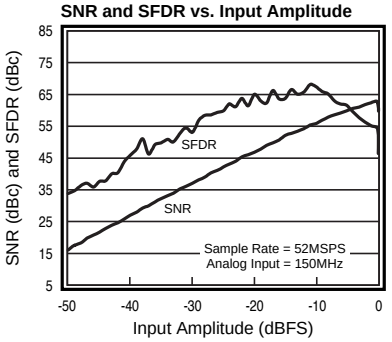
SNR and SFDR vs. Input Amplitude



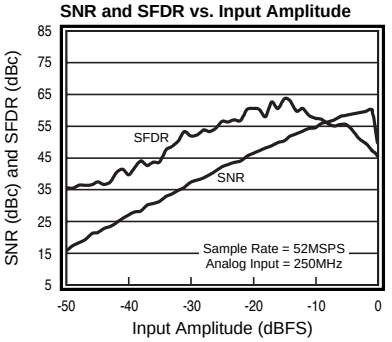
SNR and SFDR vs. Input Amplitude



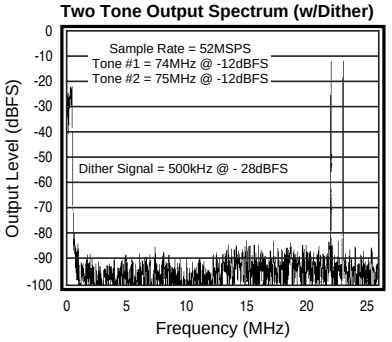
SNR and SFDR vs. Input Amplitude



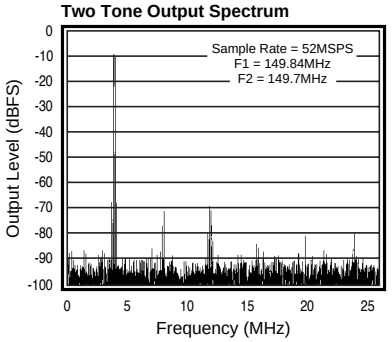
SNR and SFDR vs. Input Amplitude



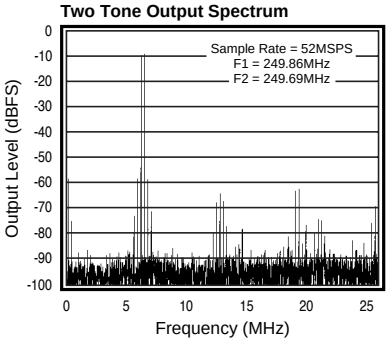
Two Tone Output Spectrum (w/Dither)



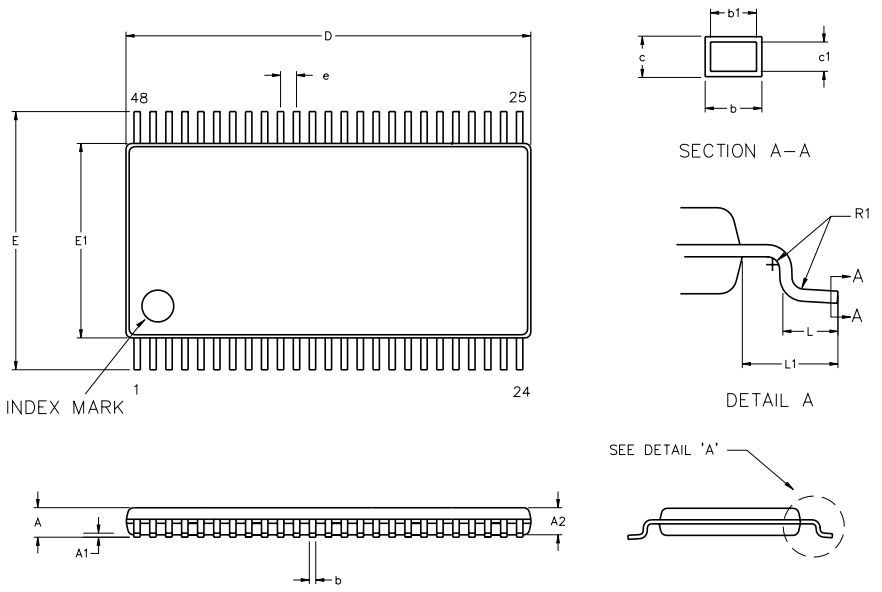
Two Tone Output Spectrum



Two Tone Output Spectrum



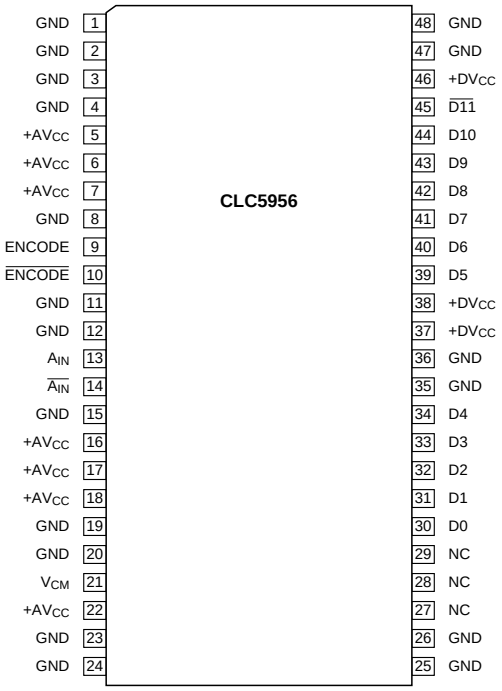
Physical Dimensions



Symbol	Min	Max	Notes
A	–	1.10	
A1	0.05	0.15	
A2	0.80	1.05	
b	0.17	0.27	
b1	0.17	0.23	
c	0.09	0.20	
c1	0.09	0.16	
D	12.40	12.60	2
E	8.1 BSC		
E1	6.00	6.20	2
e	0.50 BSC		
L	0.50	0.75	
L1	1.00 REF		
R1	0.127		

Notes:
1. All dimensions are in millimeters.
2. Dimensions D and E1 do not include mold protrusion. Allowable protrusion is 0.20mm per side.

CLC5956 Pin Definitions



A_{IN}
$\overline{A_{IN}}$ (Pin 13, 14) Differential input with a common mode voltage of +2.4V. The ADC full scale input is $1.024V_{pp}$ on each of the complimentary input signals.

ENCODE (Pin 9, 10) Differential clock where ENCODE initiates a new data conversion cycle on each rising edge.

$\overline{\text{ENCODE}}$ Logic for these inputs are a 50% duty cycle differential PECL signal.

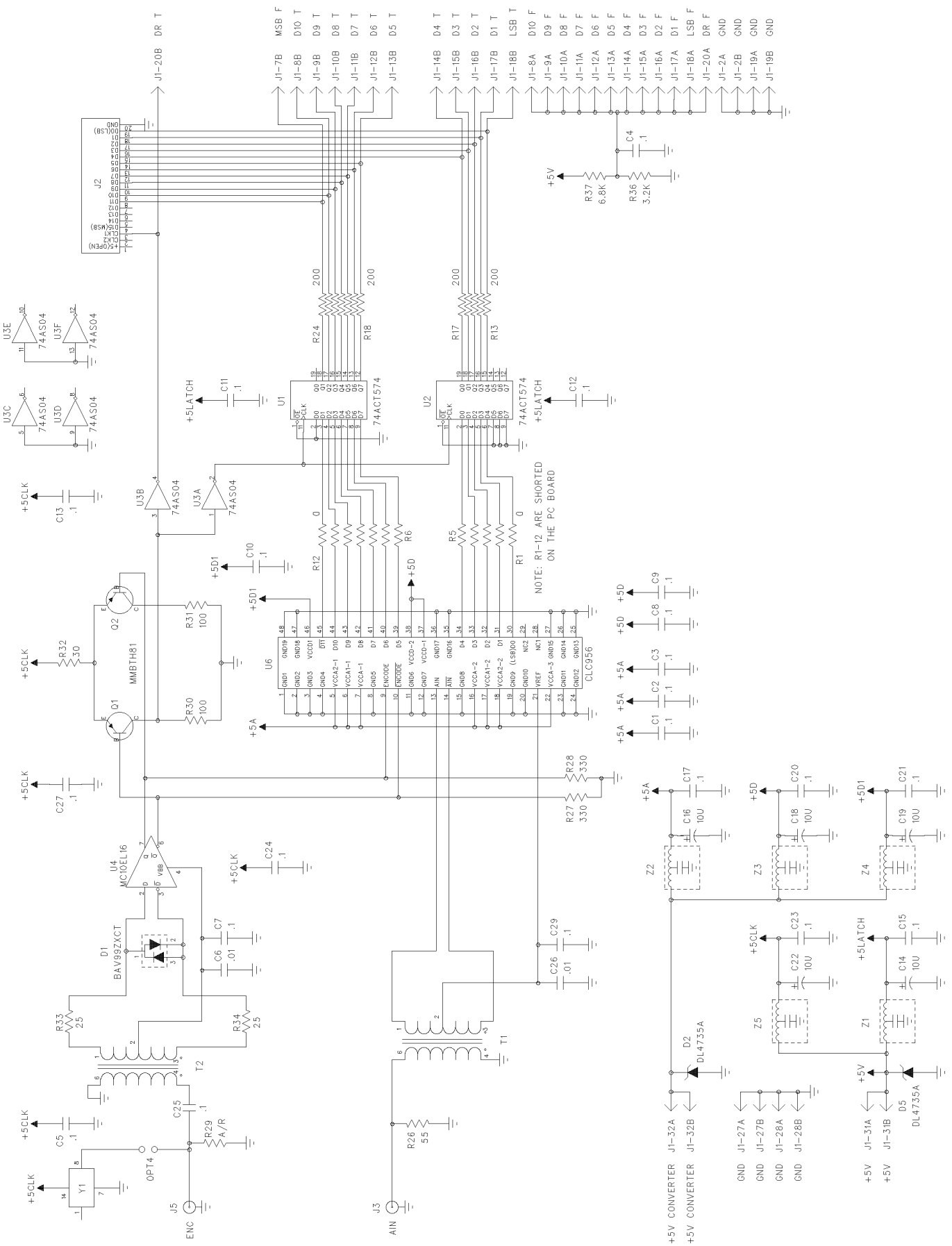
VCM (Pin 21) Internal common mode voltage reference. Nominally +2.4V. Can be used for the input common mode voltage. This voltage is derived from an internal bandgap reference.

D0-$\overline{\text{D11}}$ (Pins 30-34, 39-45) Digital data outputs are CMOS and TTL compatible. D0 is the LSB and $\overline{\text{D11}}$ is the MSB. MSB is inverted. Output coding is two's complement.

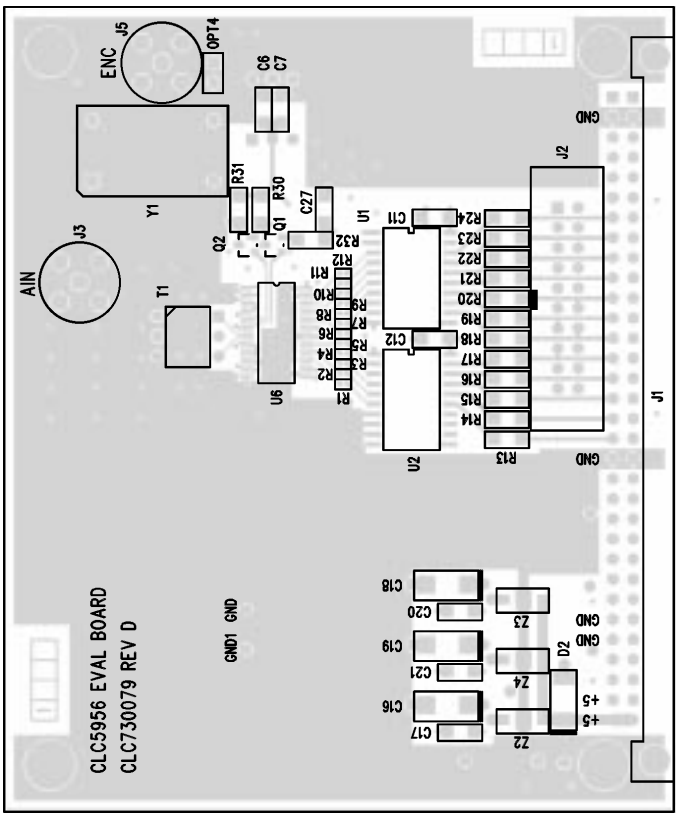
GND (Pins 1-4, 8, 11, 12, 15, 19, 20, 23-26, 35, 36, 47, 48) circuit ground.

$+AV_{CC}$ (Pins 5-7, 16-18, 22,) +5V power supply for the analog section. Bypass to ground with a 0.1µF capacitor.

$+DV_{CC}$ (Pin 37, 38, 46) +5V power supply for the digital section. Bypass to ground with a 0.1µF capacitor.

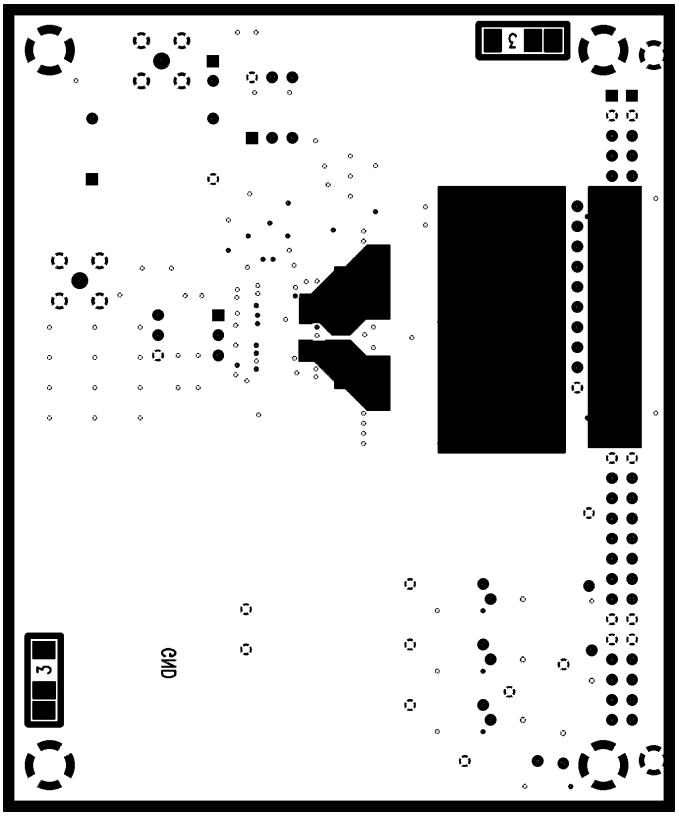


Evaluation Board Schematic

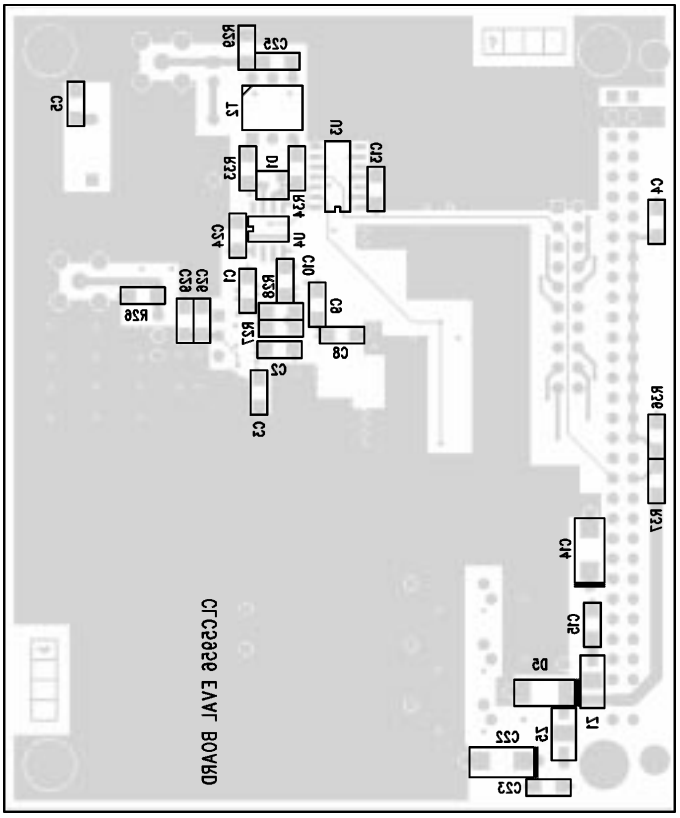


CLC730079 Layer 1

CLC730079 Layer 2



CLC730079 Layer 3



CLC730079 Layer 4

CLC5956 Evaluation Printed Circuit Board
The Evaluation board for the CLC5956 allows for easy test and evaluation of the product. The part may be ordered with all components loaded and tested. The order number is the CLC5956PCASM. The user supplies an analog input signal, encode signal and power to the board and is able to take latched 12-bit digital data out of the board.

ENCODE Input (ENC)
The ENCODE input is an SMA connector with a 50Ω termination. The signal is converted from single to differential and its **frequency is divided by four** to produce a low jitter, symmetrical encode signal for the CLC5956. The user should provide a sinusoidal or square wave signal of 10 to 16dBm amplitude at **four times the converter's desired sample rate.** It is recommended that the source be low jitter to maintain best performance. The transformer will pass signals in the 40 to 260MHz range which allows sample rates of 10 to 65Msps.

CLC5956 Clock Option
The CLC5956 board is configured for a 4x clock input to provide optimal performance with some (i.e. HP8662) synthesizers. The HP8662 output has lower jitter above 160MHz. Using a 208MHz clock to sample at 52MHz minimizes the effect of the synthesizer on the measurement.

To use a 1x clock, replace the divide-by-4 sine-to-PECL converter (U4, MC10EL33D) with an MC10EL16D. The MC10EL16D sine-to-PECL converter does not divide the clock. This approach would be suitable for use with a synthesizer that has optimal jitter performance at 52MHz (i.e. HP8643 or HP8644).

The best ADC performance is obtained with a low-jitter crystal oscillator module installed at Y1 on the evaluation board. U4 should be replaced with an MC10EL16D. Placing the clock source on the evaluation board reduces ground loop issues and thus improves performance.

Analog Input (AIN)
The analog input is an SMA connector with a 50Ω termination. The signal is converted from single to differential by a transformer with a 5 to 260MHz bandwidth and approximately one dB loss. Full scale is approximately 11dBm or $2.2V_{pp}$. It is recommended that the source for the analog input signal be low jitter, low noise and low distortion to allow for proper test and evaluation of the CLC5956.

Supply Voltages (J1 pins 31 A&B and 32 A&B)
The CLC5956PCASM is powered from a single 5V supply connected from the referenced pins on the Eurocard connector. The recommended supplies are low noise linear supplies.

Digital Outputs (J1 pins 7A ($\overline{\text{MSB}}$, $\overline{\text{D11}}$), 8B (D10) through 18B (LSB) and 20B (Data Ready))
The digital outputs are provided on the Eurocard connector. The outputs are buffered by 5V CMOS latches with 50Ω series output resistors. The rising edge of Data Ready may be used to clock the output data into data collection cards or logic analyzers. The board has a location for the HP 01650-63203 termination adapter for HP 16500 logic analyzers to simplify connection to the analyzer.

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