

## CLC5644

# Low-Power, Low-Cost, Quad Operational Amplifier

### General Description

The CLC5644 is a quad, current feedback operational amplifier that is perfect for many cost-sensitive applications that require high performance, especially when power dissipation is critical. Not only does the CLC5644 offer excellent economy in board space, but has an excellent performance vs power tradeoff which yields a 170MHz Small Signal Bandwidth while dissipating only 25mW. Applications requiring significant density of high speed devices such as video routers, matrix switches and high-order active filters will benefit from the configuration of the CLC5644 and the low channel-to-channel crosstalk of 76dB at 1MHz.

The CLC5644 provides excellent performance for video applications. Differential gain and phase of 0.04% and 0.07° makes this device well suited for many professional composite video systems, but consumer applications will also be able to take advantage of these features due to the device's low cost. The CLC5644 offers superior dynamic performance with a small signal bandwidth of 170MHz and slew rate of 1000V/μs. These attributes are well suited for many component video applications such as driving RGB signals down significant lengths of cable. These and many other applications can also take advantage of the 0.1dB flatness to 25MHz.

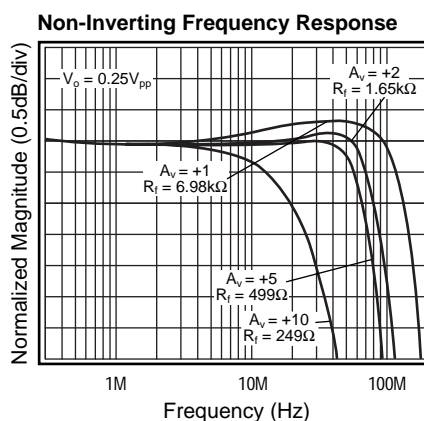
Combining wide bandwidth with low cost makes the the CLC5644 an attractive option for active filters. SAW filters are often used in IF filters in the 10's of MHz range, but higher order filters designed around a quad operational amplifier may offer an economical alternative to the typical SAW approach and offer greater freedom in the selection of filter parameters. National Semiconductor's Comlinear Products Group has published a wide array of literature on active filters and a list of these publications can be found on the last page of this datasheet.

### Features

- 170MHz small signal bandwidth
- 1000 V/μs slew rate
- 2.5mA / channel supply current
- -72/-79dBc HD2/HD3 (5MHz)
- 0.04%, 0.07° differential gain, phase
- 70mA output current
- 16ns settling to 0.1%

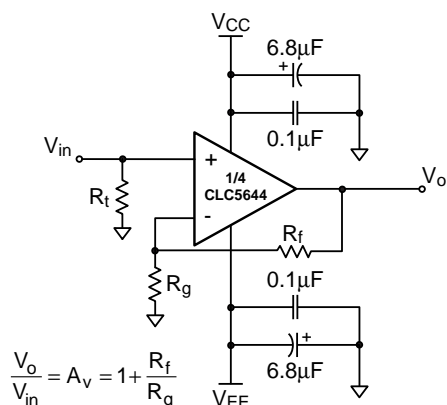
### Applications

- Portable equipment
- Video switchers & routers
- Video line driver
- Active filters
- IF amplifier
- Twisted pair driver/receiver

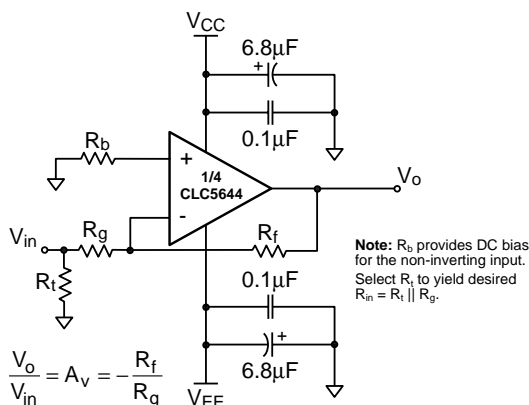


### Typical Configurations

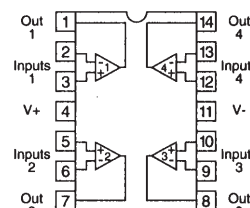
#### Non-Inverting Gain



#### Inverting Gain



#### Pinout DIP & SOIC



# CLC5644 Electrical Characteristics ( $A_v = +2$ , $R_f = 1.65k\Omega$ , $R_L = 100\Omega$ , $V_s = \pm 5V$ , unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS		UNITS	NOTES
Ambient Temperature	CLC5644I	+25°C	+25°C	-40 to 85°C		
<b>FREQUENCY DOMAIN RESPONSE</b>						
-3dB bandwidth	$A_v = 1$ $V_o < 0.5V_{pp}$ $V_o < 5V_{pp}$	170 125 50	— — —	— — —	MHz MHz MHz	
0.1dB bandwidth		25	—	—	MHz	
differential gain	NTSC, $R_L = 150\Omega$	0.04	—	—	dB	
differential phase	NTSC, $R_L = 150\Omega$	0.07	—	—	dB	
<b>TIME DOMAIN RESPONSE</b>						
rise and fall time	0.5V step	2.7	—	—	ns	
	5V step	7	—	—	ns	
settling time to 0.1%	1V step	16	—	—	ns	
overshoot	0.5V step	4	—	—	%	
slew rate		1000	—	—	V/ $\mu$ s	
<b>DISTORTION AND NOISE RESPONSE</b>						
2 <sup>nd</sup> harmonic distortion	$2V_{pp}$ , 1MHz	-72	—	—	dBc	
3 <sup>rd</sup> harmonic distortion	$2V_{pp}$ , 1MHz	-79	—	—	dBc	
equivalent input noise						
voltage ( $e_{ni}$ )	>1MHz	4.5	—	—	nV/ $\sqrt{Hz}$	
non-inverting current ( $i_{bn}$ )	>1MHz	1.5	—	—	pA/ $\sqrt{Hz}$	
inverting current ( $i_{bi}$ )	>1MHz	10	—	—	pA/ $\sqrt{Hz}$	
crosstalk (input inferred)	10MHz	76	—	—	dBc	
<b>STATIC DC PERFORMANCE</b>						
input offset voltage		2.5	7	15	mV	A
average drift		25	—	90	$\mu$ V/°C	
input bias current (non-inverting)		2	6	10	$\mu$ A	A
average drift		15	—	80	nA/°C	
input bias current (inverting)		2.5	7.5	22	$\mu$ A	A
average drift		24	—	150	nA/°C	
power supply rejection ratio	DC	50	46	44	dB	
common-mode rejection ratio	DC	50	45	43	dB	
supply current (per channel)	$R_L = \infty$	2.5	3	3	mA	A
<b>MISCELLANEOUS PERFORMANCE</b>						
input resistance (non-inverting)		2	1	0.5	M $\Omega$	
input capacitance (non-inverting)		1	2	2	pF	
common-mode input range		$\pm 2.2$	$\pm 2.0$	$\pm 1.4$	V	
output voltage range	$R_L = 150\Omega$	$\pm 2.8$	$\pm 2.6$	$\pm 2.5$	V	
output current		70	50	30	mA	
output resistance, closed loop	DC	0.2	0.3	0.6	m $\Omega$	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

## Notes

A) I-level: spec is 100% tested at +25°C.

## Reliability Information

Transistor Count	152
MTBF (based on limited test data)	23.6Mhr

## Package Thermal Resistance

Package	$\theta_{JC}$	$\theta_{JA}$
Plastic (IN)	60°C/W	110°C/W
Surface Mount (IM)	55°C/W	125°C/W

## Absolute Maximum Ratings

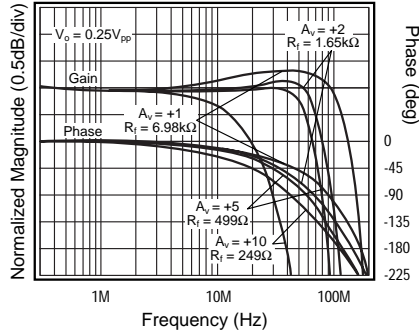
supply voltage ( $V_{CC} - V_{EE}$ )	+14V
output current	95mA
common-mode input voltage	$V_{EE}$ to $V_{CC}$
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

## Ordering Information

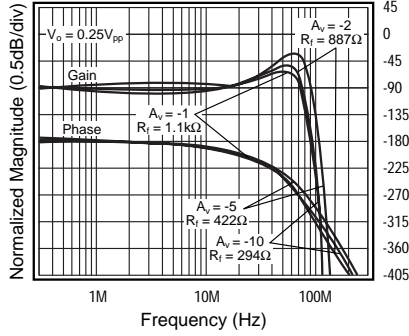
Model	Temperature Range	Description
CLC5644IN	-40°C to +85°C	14-pin PDIP
CLC5644IM	-40°C to +85°C	14-pin SOIC
CLC5644IMX	-40°C to +85°C	14-pin tape and reel

# CLC5644 Typical Performance ( $A_v = +2$ , $R_f = 1.65k\Omega$ , $R_L = 100\Omega$ , $V_s = +5V$ , unless specified)

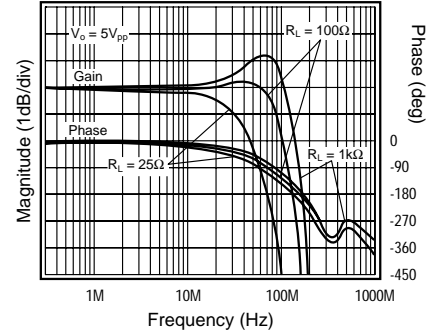
**Non-Inverting Frequency Response**



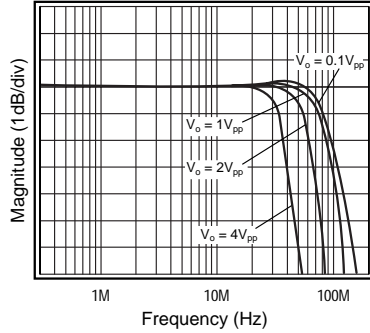
**Inverting Frequency Response**



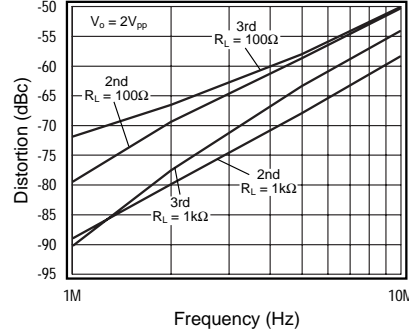
**Frequency Response vs.  $R_L$**



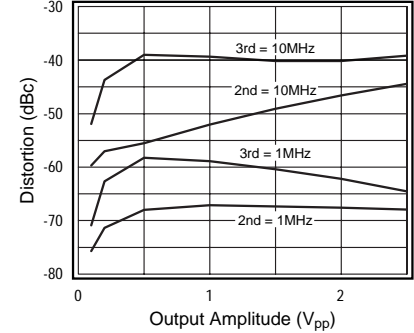
**Frequency Response vs.  $V_o$**



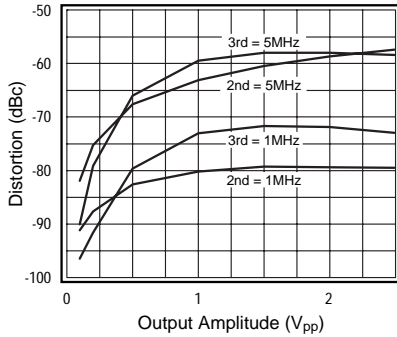
**2nd & 3rd Harmonic Distortion**



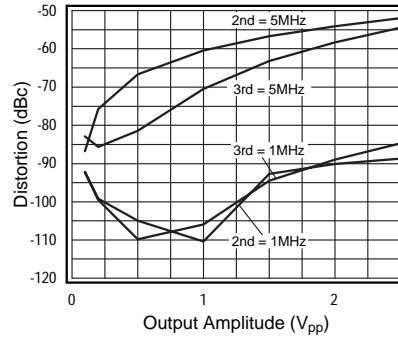
**2nd & 3rd Harmonic Distortion,  $R_L = 250\Omega$**



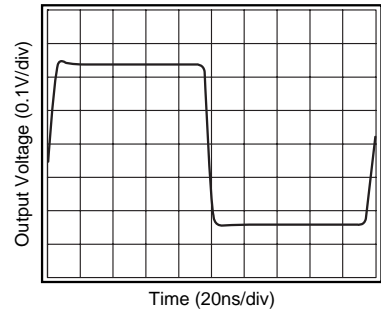
**2nd & 3rd Harmonic Distortion,  $R_L = 100\Omega$**



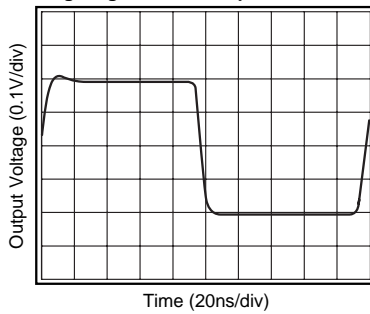
**2nd & 3rd Harmonic Distortion,  $R_L = 1k\Omega$**



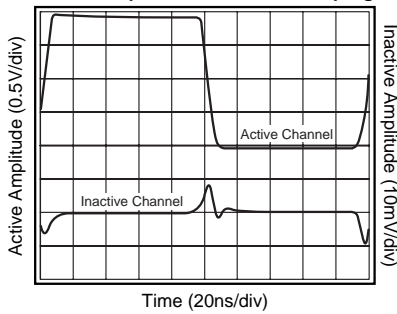
**Small Signal Pulse Response**



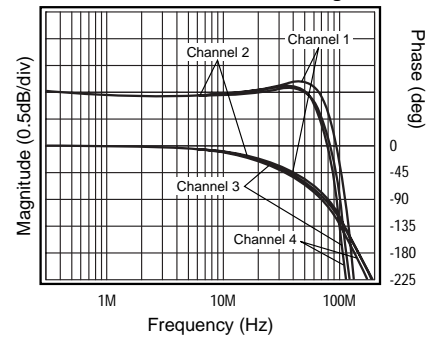
**Large Signal Pulse Response**



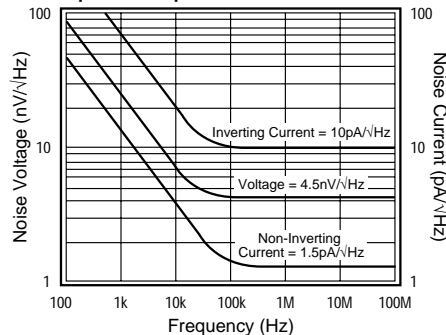
**Most Susceptible Channel Pulse Coupling**



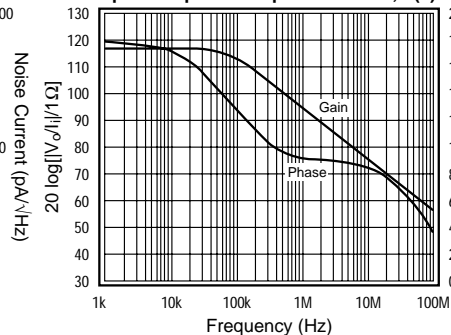
**Channel to Channel Gain Matching**



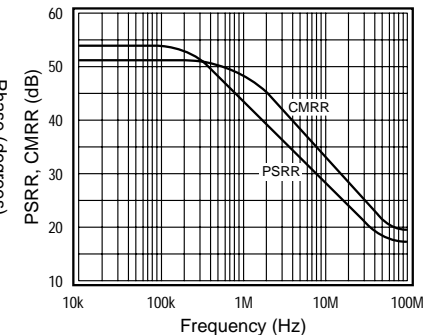
**Equivalent Input Noise**



**Open-Loop Transimpedance Gain,  $Z(s)$**



**PSRR and CMRR**



## Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with  $R_f$
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$\frac{V_o}{V_i} = \frac{A_v}{1 + \frac{R_f}{Z(j\omega)}} \quad \text{Equation 1}$$

where:

$A_v$  is the closed loop DC voltage gain

$R_f$  is the feedback resistor

$Z(j\omega)$  is the open loop transimpedance gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the -3dB corner frequency, the interaction between  $R_f$  and  $Z(j\omega)$  dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing  $R_f$  has the following affects:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

## Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC5644 (CLC730024 - DIP, CLC730031 - SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization. General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

- Include 6.8 $\mu$ F tantalum and 0.1 $\mu$ F ceramic capacitors on both supplies.
- Place the 6.8 $\mu$ F capacitors within 0.75 inches of the power pins.
- Place the 0.1 $\mu$ F capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.

## Active Filter Application Notes

- OA-21 Simplified Component Pre-Distortion for High Speed Active Filters
- OA-26 Designing High-Speed Active Filters
- OA-27 Low-Sensitivity, Lowpass Filter Design
- OA-28 Low-Sensitivity, Bandpass Filter Design with Tuning Method
- OA-29 Low-Sensitivity, Highpass Filter Design with Parasitic Compensation

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