National Semiconductor

CLC5526
Digital Variable Gain Amplifier (DVGA)

General Description

The CLC5526 is a high performance, digitally controlled, variable-gain amplifier (DVGA). It has been designed for use in a broad range of mixed signal and digital communication applications such as mobile radio, cellular base stations, and back-channel modems where automatic-gain-control (AGC) is required to increase system dynamic range.

The CLC5526 has differential input and output, allowing large signal swings on a single 5V rail. The input impedance is 200Ω. The differential output impedance is 600Ω and is designed to drive a 1kΩ differential load. The output amplifier has excellent intermodulation performance. The CLC5526 is designed to accept signals from RF elements and maintain a terminated impedance environment.

The CLC5526 maintains a 350MHz bandwidth over its entire gain and attenuation range from +30dB to -12dB. Internal clamping ensures very fast overdrive recovery. Two tone inter-modulation distortion is excellent: at 150MHz, $1V_{pp}$ it is -60 dBc.

Input signals to the CLC5526 are scaled by an accurate, differential R-2R resistive ladder with an input impedance of 200Ω. A scaled version of the input is selected under digital control and passed to the internal amplifier. The input common mode level is set at 2.4V via a bandgap referenced bias generator which can be overridden by an external input.

Following the resistive ladder is a fixed, 30dB gain amplifier. The output stage common mode voltage of the CLC5526 is set to 3V, by internal, positive supply connected resistors.

Digital control of the CLC5526 is accomplished by a 3-bit parallel gain control input and a data valid pin to latch the data. If the data is not latched, the DVGA is transparent to gain control updates. All digital inputs are TTL/CMOS compatible.

A shutdown input reduces the CLC5526 supply current to a few mA. During shutdown, the input termination is maintained and current attenuation settings are held.

The CLC5526 operates over the industrial temperature range of -40°C to +85°C. The part is available in a 20 pin SSOP package.

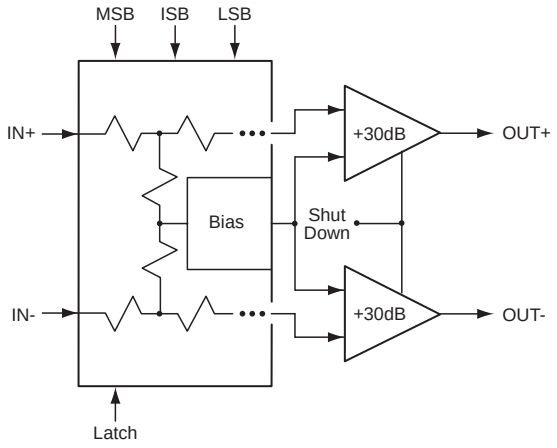
Features

- 350MHz bandwidth
- Differential input and output
- Low two tone intermod. distortion: -60dBc @ $1V_{pp}$, 150MHz
- Low noise: 2.5nV/√Hz (max gain)
- Wide gain range: +30dB to -12dB
- Gain control: parallel w/data latching
- Gain step size: 6dB
- Supply voltage: +5V
- Supply current: 48mA

Applications

- Cellular/PCS base stations
- IF sampling receivers
- Infrared/CCD imaging
- Back-channel modems
- Electro-optics
- Instrumentation
- Medical imaging
- High definition video

CLC5526 Block Diagram



CLC5526 Electrical Characteristics (V_{CC}= +5V, R_L = 1kΩ, maximum gain setting; unless specified)

PARAMETERS	CONDITIONS	TEMP	RATINGS			UNITS	NOTES
			MIN	TYP	MAX		2
DYNAMIC PERFORMANCE							
small-signal bandwidth		+25°C		350		MHz	
NOISE AND DISTORTION							
2nd harmonic distortion							
	$1V_{pp}$, 150MHz	+25°C	53	67		dBc	1
	$1V_{pp}$, 250MHz	+25°C		64		dBc	
	$2V_{pp}$, 150MHz	+25°C	43	62		dBc	1
	$2V_{pp}$, 250MHz	+25°C		58		dBc	
3rd harmonic distortion							
	$1V_{pp}$, 150MHz	+25°C	53	71		dBc	1
	$1V_{pp}$, 250MHz	+25°C		70		dBc	
	$2V_{pp}$, 150MHz	+25°C	43	57		dBc	1
	$2V_{pp}$, 250MHz	+25°C		56		dBc	
two tone intermodulation distortion							
149.9MHz (f_1), 150.1MHz (f_2)	$1V_{pp}$ composite	+25°C		64		dBc	
	$2V_{pp}$ composite	+25°C		61		dBc	
249.9MHz (f_1), 250.1MHz (f_2)	$1V_{pp}$ composite	+25°C		63		dBc	
	$2V_{pp}$ composite	+25°C		54		dBc	
thermal noise							
	minimum gain	+25°C		2.2		nV/√Hz	
	maximum gain	+25°C		2.5		nV/√Hz	
noise figure	maximum gain	+25°C		9.3		dB	
ANALOG I/O							
differential input impedance		+25°C		200		Ω	
differential output impedance		+25°C		600		Ω	
input signal level (AC coupled)	maximum gain	Full		126		mV	
maximum input signal level	recommended	Full		6		V_{pp}	
maximum output signal level	recommended	Full		4		V_{pp}	
output clipping		Full		8		V_{pp}	
GAIN PARAMETERS							
maximum gain		+25°C		30		dB	
minimum gain		+25°C		-12		dB	
gain step size		+25°C		6.02		dB	
gain step accuracy	(1 sigma)	+25°C		0.03		dB	
cumulative gain step error	(1 sigma)	+25°C		0.085		dB	
DIGITAL INPUTS/TIMING							
logic compatibility		Full		TTL/CMOS			
input voltage	logic LOW	Full			0.8	V	
	logic HIGH	Full	2.0			V	
setup time (Tsu)		+25°C		3		nsec	
hold time (Thold)		+25°C		3		nsec	
minimum pulse width (Tpw)		+25°C		3		nsec	
POWER REQUIREMENTS							
+5V supply current		+25°C		48	60	mA	1
	shutdown	+25°C		9		mA	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes

1) These parameters are 100% tested at 25°C.

2) Typical specifications are the mean values of the distributions of deliverable amplifiers tested to date.

Absolute Maximum Ratings

positive supply voltage (V_{CC})	-0.5V to +6V
differential voltage between any two grounds	<200mV
analog input voltage range	-0.5V to +V_{CC}
digital input voltage range	-0.5V to +V_{CC}
output short circuit duration (one-pin to ground)	infinite
junction temperature	175°C
storage temperature range	-65°C to 150°C
lead solder duration (+300°C)	10sec

Note: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Recommended Operating Conditions

positive supply voltage (V_{CC})	+5V ±5%
differential voltage between any two grounds	<10mV
analog input voltage range, AC coupled	±0.5V
operating temperature range	-40°C to +85°C

Package Thermal Resistance

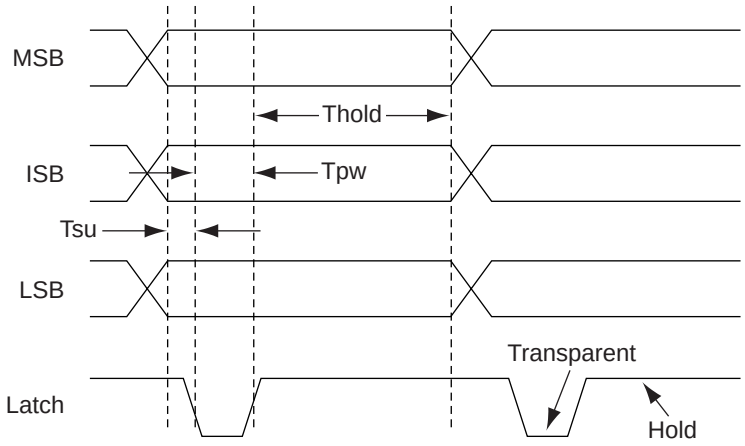
Package	θ_{JA}	θ_{JC}
20-pin SSOP	90°C/W	38°C/W

Reliability Information

Transistor count	300

Ordering Information

Model	Temperature Range	Description
CLC5526MSA	-40°C to +85°C	20-pin SSOP (industrial part)
CLC5526PCASM		Fully loaded evaluation board with CLC5526 … ready for test.



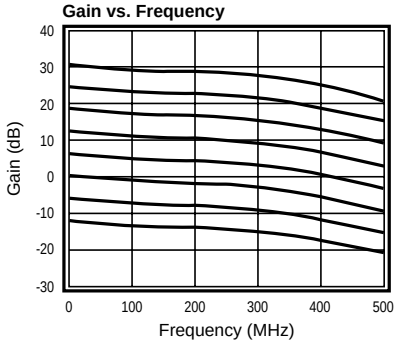
CLC5526 Timing Diagram

Gain Word	MSB	ISB	LSB	Gain (dB)
0	0	0	0	-12
1	0	0	1	-6
2	0	1	0	0
3	0	1	1	+6
4	1	0	0	+12
5	1	0	1	+18
6	1	1	0	+24
7	1	1	1	+30

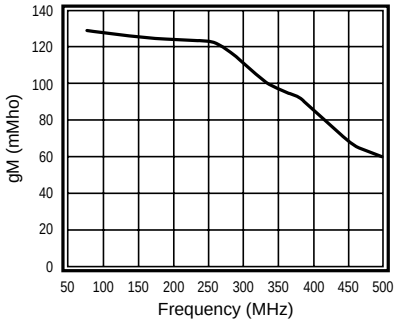
CLC5526 Truth Table

CLC5526 Typical Performance Characteristics (V_{CC} = +5V, R_L = 1kΩ, max gain; unless specified)

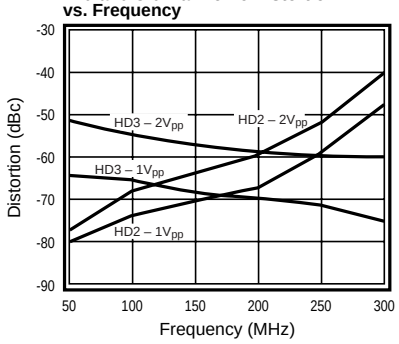
Gain vs. Frequency



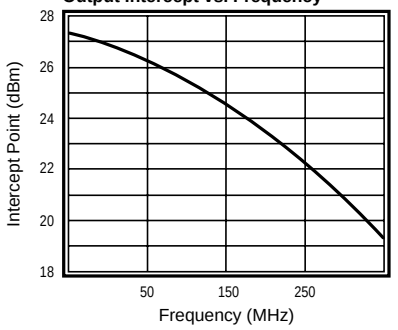
Transconductance vs. Frequency



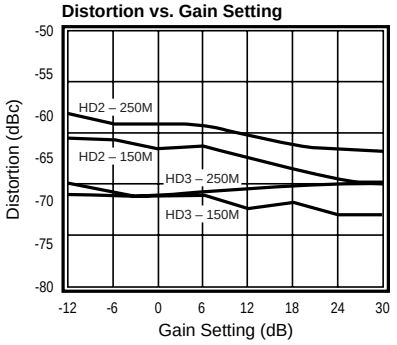
2nd and 3rd Harmonic Distortion vs. Frequency



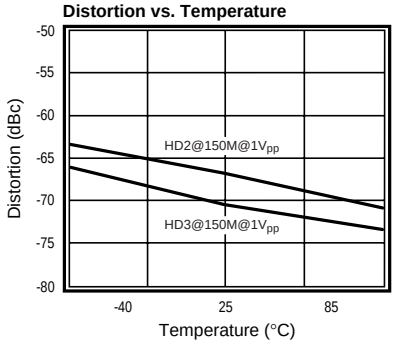
2-Tone, 3rd Order Intermodulation Output Intercept vs. Frequency



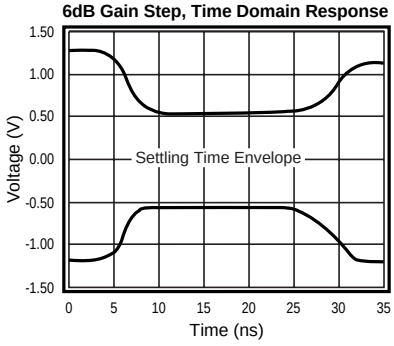
Distortion vs. Gain Setting



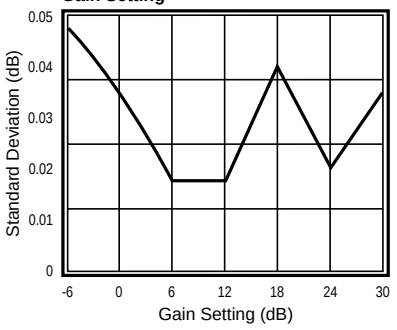
Distortion vs. Temperature



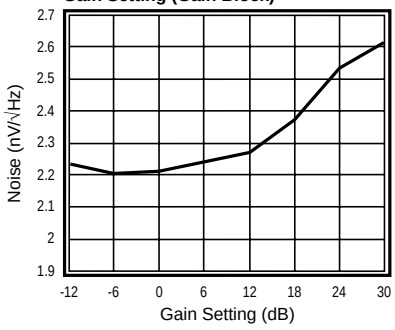
6dB Gain Step, Time Domain Response



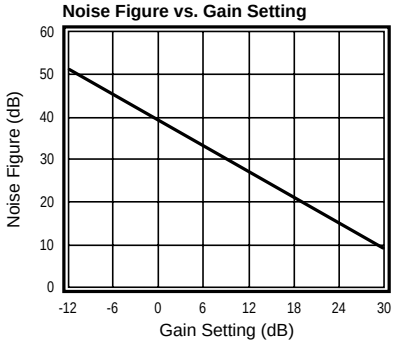
Gain Step Error Deviation vs. Gain Setting



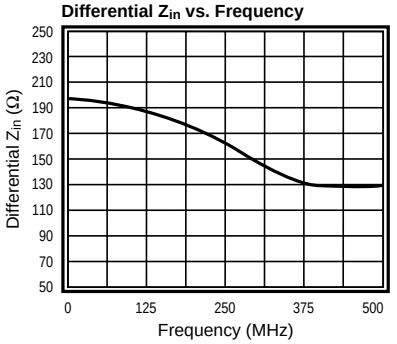
Input Referred Thermal Noise vs. Gain Setting (Gain Block)



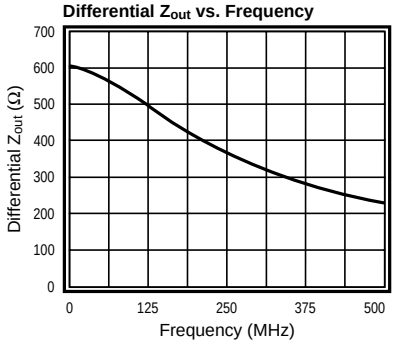
Noise Figure vs. Gain Setting



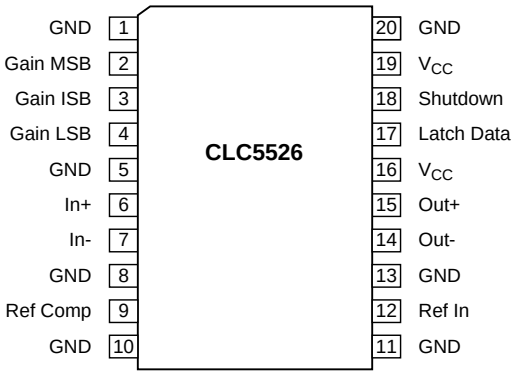
Differential Z_{in} vs. Frequency



Differential Z_{out} vs. Frequency

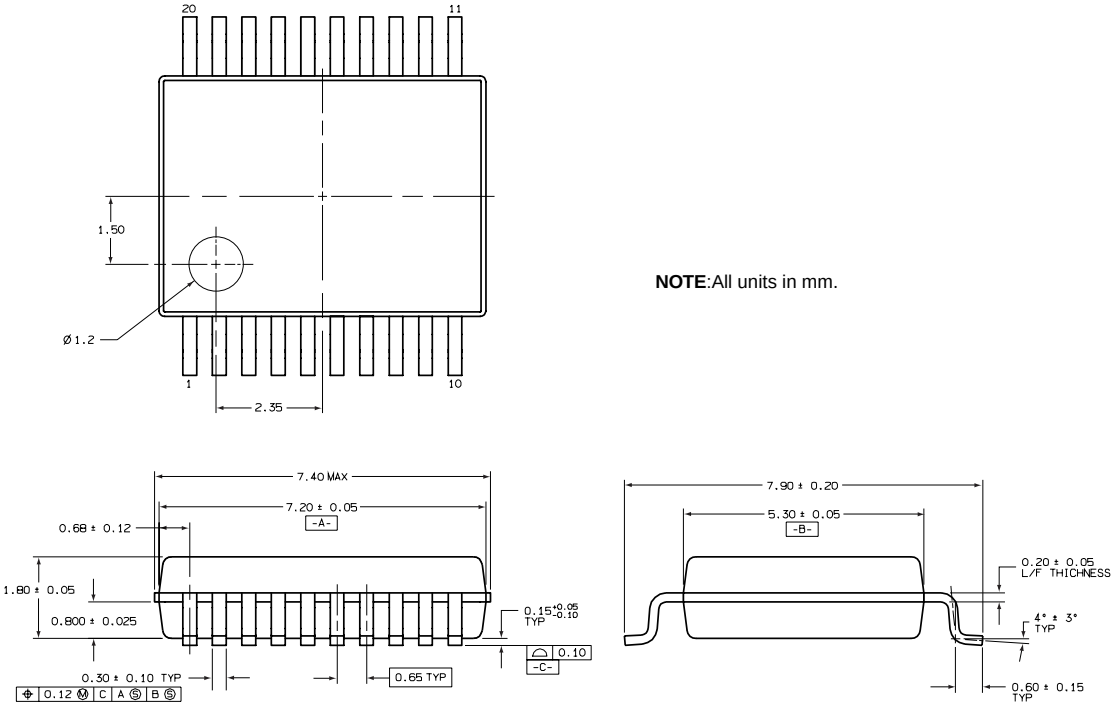


CLC5526 PIN DEFINITIONS



GND	(Pins 1, 5, 8, 10, 11, 13, 20) Circuit Ground
Gain MSB	(Pin 2) Gain Selection Most Significant Bit
Gain ISB	(Pin 3) Gain Selection Data Bit
Gain LSB	(Pin 4) Gain Selection Least Significant Bit
In+	(Pin 6) Positive Differential Input
In-	(Pin 7) Negative Differential Input
Ref Comp	(Pin 9) Reference Compensation
V_{CC}	(Pin 16, 19) Positive Supply Voltage
Shutdown	(Pin 18) Low Power Standby Control (Active High)
Latch Data	(Pin 17) Data Latch Control (Active High)
Out+	(Pin 15) Positive Differential Output
Out-	(Pin 14) Negative Differential Output
Ref In	(Pin 12) External Reference Input

CLC5526 PHYSICAL DIMENSIONS



NOTE:All units in mm.

CLC5526 APPLICATIONS

Description

The CLC5526 is a digitally programmable, variable gain amplifier with the following features:

- 8 gain settings ranging from -12 to +30dB in 6dB steps
- Differential inputs and outputs (externally AC coupled)
- Self biased input common-mode voltage
- 3-Bit parallel digital control
- Single +5V supply
- Low-Power standby mode

Please refer to Figure 1 for a representative block diagram.

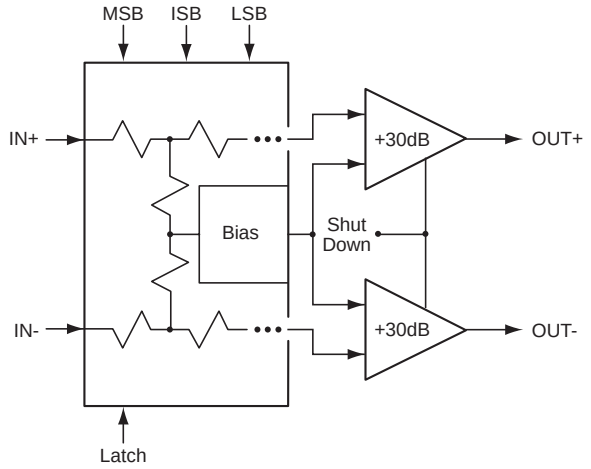


Figure 1: CLC5526 Block Diagram

Gain Selection

Gain levels can be decreased from the maximum value in -6dB steps via the 3-bit digital inputs. Table 1 shows the gain selection truth table for a 1000Ω differential load.

Gain Word	MSB	ISB	LSB	Gain (dB)
0	0	0	0	-12
1	0	0	1	-6
2	0	1	0	0
3	0	1	1	+6
4	1	0	0	+12
5	1	0	1	+18
6	1	1	0	+24
7	1	1	1	+30

Table 1: Gain Selection Truth Table

Gain settings can be calculated as follows:
GAIN = -12 dB + (Gain Word) * 6.02dB

Gain selection has two modes: Transparent or latched, depending on the LATCH input. If the LATCH input is held LOW, then the device is in the transparent mode. Changes on data inputs will result in direct changes to the gain setting.

Input data will be latched upon the LOW to HIGH transition of LATCH. While LATCH is HIGH, digital data will be ignored until LATCH is strobed low again.

Note: Upon power-up the analog inputs are disconnected from the internal amplifier. LATCH will need to be strobed LOW before an analog output will be present!

Differential I/O Considerations

Analog inputs and outputs need to be AC coupled to prevent DC loading of the common-mode voltages. If driving the CLC5526 from a single-ended 50Ω source is required, a 1:2 transformer should be used to generate the differential inputs. As the differential input impedance of the CLC5526 is 200Ω, the 1:4 impedance ratio will allow for optimum matching to the 50Ω source. The secondary outputs of the transformer should be AC coupled to the CLC5526 analog inputs, while the secondary center tap of the transformer should be directly connected to the system ground.

The CLC5526 is designed to drive differential circuits, such as the CLC5956 Analog to Digital converter. Figure 2 below shows a typical application of the CLC5526.

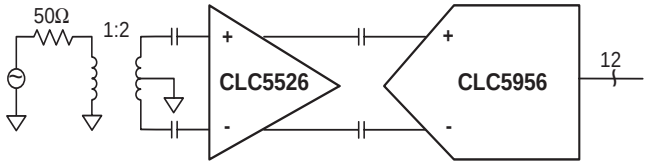


Figure 2: Differential I/O Connections

Driving Loads

Actual gain of the CLC5525 will vary with the output load. The device is designed to provide +30dB Maximum gain with a 1000Ω differential load.

Each output of the CLC5526 contains an internal 300Ω resistor to the V_{CC} rail. Actual gain calculations need to take this in account with a given external load resistor. The effective load resistance can be used with the following equation to calculate Max gain values.

$A_v = 20 \log (0.0843 * R_{leff})$
Where: $R_{leff} = R_{int} \parallel R_{ext(diff)}$
$R_{int} = 600\Omega$ differential

Chart 1 below shows maximum gain values over output load. Resistor values are for differential loads.

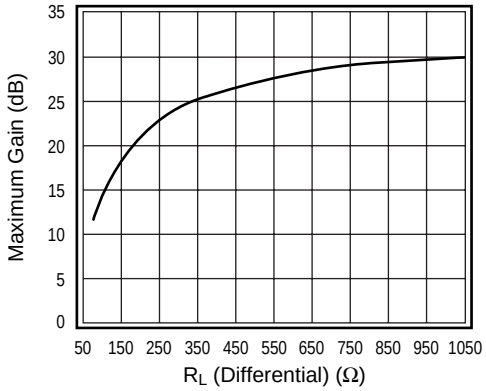


Chart 1: Maximum Gain vs. Rload

Stray capacitance at the output, along with the output load value will form a pole, which can degrade the CLC5526 bandwidth. For a narrow-band application this problem can be alleviated by using a tuned load, which will incorporate any stray parasitic impedance into a resonant circuit. By tuning the resonant load, full gain can be achieved with a given resistive load.

A typical tuned load is shown below in Figure 3, where the resonant frequency is tuned about 150MHz.

The 1000Ω load in this circuit can represent the input impedance of the CLC5956 Analog to Digital converter. Actual values for the reactive components may vary slightly to account for board and device parasitic elements.

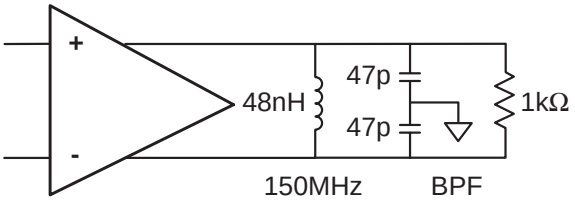


Figure 3: CLC5526 Driving a tuned load.

CLC5526 Typical Application

Although the CLC5526 can be used as a general purpose digital variable gain amplifier, it was specifically designed to provide the variable gain function in National's Diversity Receiver Chipset. In this application, the CLC5526 drives a tuned BPF and the CLC5956 Analog to Digital converter. Digitized IF data is downsampled and tuned with the CLC5902 dual digital tuner which also provides the AGC control function. AGC data is fed back to the CLC5526. The CLC5956 differential input impedance is 1000 ohms, so with the tuned load, full gain of the CLC5526 is achieved. Figure 4 shows the block diagram of the Diversity Receiver Chipset application. Figure 5 shows the SINAD vs. Input Power of the diversity receiver chipset. For input power levels ranging from 0 to -110 dB, the chip set provides a signal to noise ratio in excess of the 9dB required for a typical GSM system.

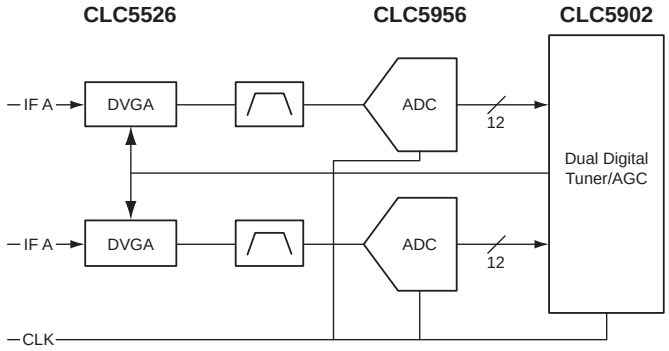


Figure 4: Diversity Receiver Chipset Block Diagram

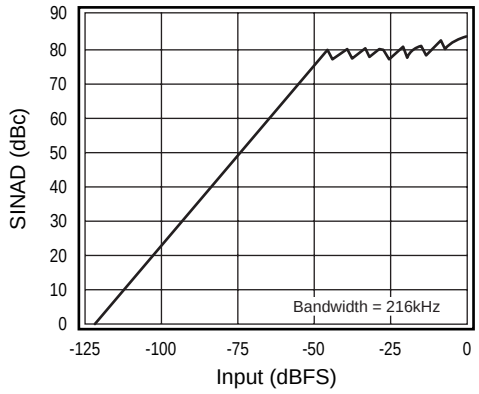


Figure 5: Diversity Receiver ChipSet SINAD vs. Input Power

Layout Considerations

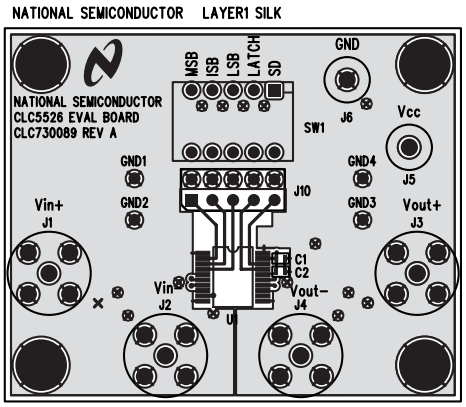
A proper printed circuit layout is essential for achieving high frequency performance. National Semiconductor provides evaluation boards for the CLC5526, which include input and output transformers for impedance matching and single to differential signal conversion.

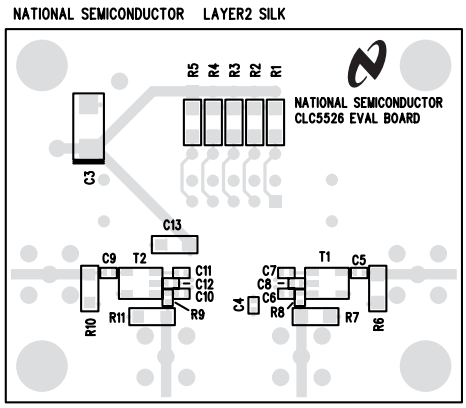
Supply bypassing is required for best performance. Provide a 6.8µF Tantalum and 0.1µF ceramic capacitor as close as possible to the supply pin.

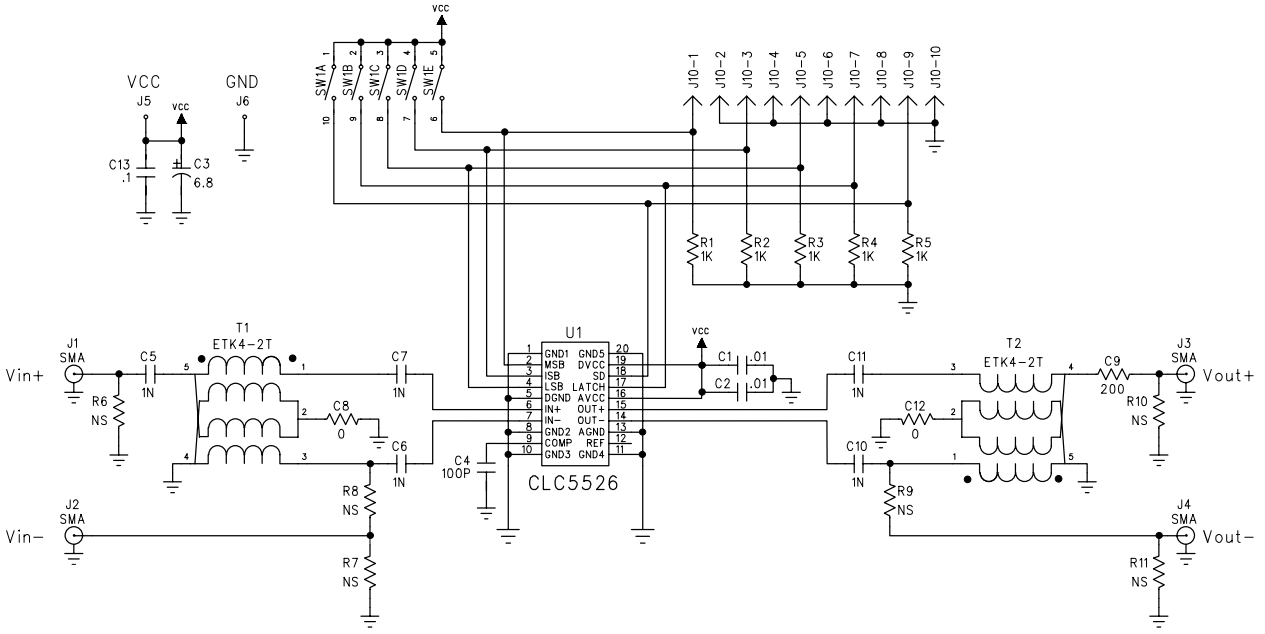
In addition, a 100pf ceramic capacitor should be placed between the COMP pin (pin 9) and the system ground. This will filter high frequency noise from the common-mode level.

Ceramic coupling capacitors should be used to AC couple both the input and output. Actual values will depend upon the signal frequency.

Evaluation Board Layout and Schematic Diagram







Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at **1-800-272-9959** or fax **1-800-737-7018**.

Life Support Policy

National's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of National Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
E-mail: europe.support.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Francais Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block
Ocean Centre, 5 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408