National Semiconductor

CLC5523
Low-Power, Variable Gain Amplifier

General Descriptions

The CLC5523 is a low power, wideband, DC-coupled, voltage-controlled gain amplifier. It provides a voltage-controlled gain block coupled with a current feedback output amplifier. High impedance inputs and minimum dependence of bandwidth on gain make the CLC5523 easy to use in a wide range of applications. This amplifier is suitable as a continuous gain control element in a variety of electronic systems which benefit from a wide bandwidth of 250MHz and high slew rate of 1800V/µs, with only 135mW of power dissipation.

Input impedances in the megaohm range on both the signal and gain control inputs simplify driving the CLC5523 in any application. The CLC5523 can be configured to use pin 3 as a low impedance input making it an ideal interface for current inputs. By using the CLC5523's inverting configuration in which R_G is driven directly, inputs which exceed the device's input voltage range may be used.

The gain control input (V_G), with a 0 to 2V input range, and a linear-in-dB gain control, simplifies the implementation of AGC circuits. The gain control circuit can adjust the gain as fast as 4dB/ns. Maximum gains from 2 to 100 are accurately and simply set by two external resistors while attenuation of up to 80dB from this gain can be achieved.

The extremely high slew rate of 1800V/µs and wide bandwidth provides high speed rise and fall times of 2.0ns, with settling time for a 2 volt step of only 22ns to 0.2%. In time domain applications where linear phase is important with gain adjust, the internal current mode circuitry maintains low deviation of delay over a wide gain adjust range.

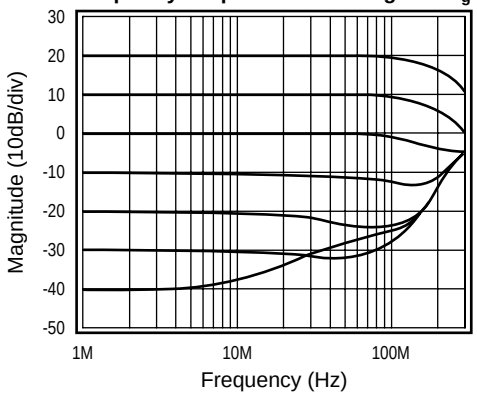
Features

- Low power: 135mW
- 250MHz, -3dB bandwidth
- Slew rate 1800V/µs
- Gain flatness 0.2dB @ 75MHz
- Rise & fall times 2.0ns
- Low input voltage noise 4nV/√Hz

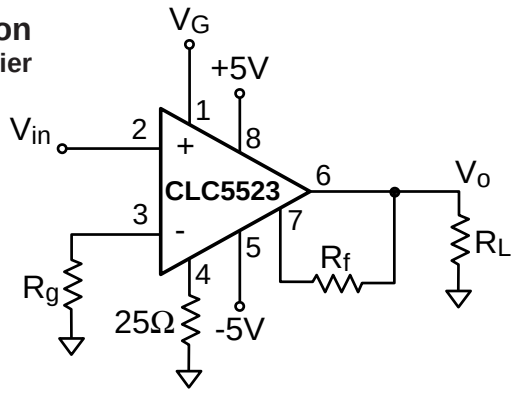
Applications

- Automatic gain control
- Voltage controlled filters
- Automatic signal leveling for A/D
- Amplitude modulation
- Variable gain transimpedance

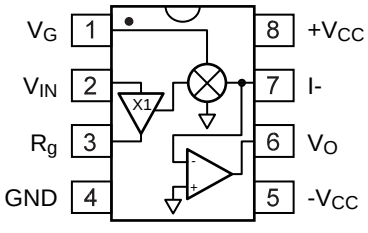
Frequency Response with Changes in V_g



Typical Application
Variable Gain Amplifier Circuit



Pinout
DIP & SOIC



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CLC5523 Electrical Characteristics (V_{CC} = ±5V, R_f = 1k, R_g = 100Ω, R_L = 100Ω, V_G = 2V; unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS		UNITS	NOTES
Ambient Temperature	CLC5523I	+25˚C	25˚C	-40 to 85˚C		
FREQUENCY DOMAIN RESPONSE						
-3dB bandwidth	V_o < 0.5V_{pp}	250	150	125	MHz	
	V_o < 4.0V_{pp}	100	45	35	MHz	
peaking	DC to 200MHz (V_o = 0.5V_{pp})	0	0.8	2.0	dB	
rolloff	DC to 75MHz (V_o = 0.5V_{pp})	0.2	1.0	1.2	dB	
linear phase deviation	DC to 75MHz (V_o = 0.5V_{pp})	0.6	1.5	3.0	deg	
gain control bandwidth	V_{in} = 0.2V_{DC}, V_g = 1V_{DC}	95	70	60	MHz	
TIME DOMAIN RESPONSE						
rise and fall time	0.5V step	2.0	2.8	3.0	ns	
overshoot	0.5V step	6.0	15	20	%	
settling time to 0.2%	2V step	22	30	60	ns	
non-inverting slew rate	4V step	700	450	400	V/µs	
inverting slew rate	4V step	1800	1000	700	V/µs	
gain control response rate		4			dB/nS	1
DISTORTION AND NOISE RESPONSE						
2nd harmonic distortion	1V_{pp}, 5MHz	-65	–	–	dBc	
3rd harmonic distortion	1V_{pp}, 5MHz	-80	–	–	dBc	
2nd harmonic distortion	1V_{pp}, 10MHz	-57	-52	-40	dBc	
3rd harmonic distortion	1V_{pp}, 10MHz	-75	-58	-54	dBc	
input referred total noise	V_g = 2V	5	6	7	nV/√Hz	
input referred voltage noise		4	5.5	5.5	nV/√Hz	
R_g referred current noise		36	50	60	pA/√Hz	
STATIC DC PERFORMANCE						
output offset voltage		50	120	150	mV	A
V_{in} signal input						
input voltage range	R_g open	±3.8	±3.6	±3.3	V	
input bias current		3.0	8.0	16	µA	A
input resistance		3.0	1.0	0.8	MΩ	
input capacitance		1.0	1.5	1.7	pF	
I_{Rgmax}	0° to 70°C	7.0	5.0	4.0	mA	
I_{Rgmax}	-40° to 85°C	7.0	5.0	2.5	mA	
signal ch. non-linearity SGNL	V_o = 2V_{pp}	0.04	0.1	0.2	%	
gain accuracy*		0.3	0.5	0.9	dB	A
V_g gain input						
input bias current		0.5	2.0	4.0	µA	
input resistance		10	2.0	2.0	MΩ	
input capacitance		1.0	1.5	1.5	pF	
ground pin current		40	55	65	µA	
power supply rejection ratio	input-referred	57	50	46	dB	
supply current	R_L = ∞	13.5	15	16	mA	A
output voltage range	no load	±3.4	±3.0	±2.3	V	
output voltage range	R_L = 100Ω	±3.0	±2.5	±2.3	V	
output impedance		0.1	0.15	0.15	Ω	
output current		80	65	50	mA	
transistor count		146				

*maximum gain is defined as R_f/R_g

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes

A) I-level: spec is 100% tested at +25˚C.

1) See plot *"Gain Control Settling Time"*.

Absolute Maximum Ratings

supply voltage	±7V
output current	±96mA
maximum junction temperature	+175˚C
storage temperature range	-65˚C to +150˚C
lead temperature (soldering 10 sec)	+300˚C
ESD rating (human body model)	TBD

Ordering Information

Model	Temp Range	Description
CLC5523IN	-40°C to +85°C	8-pin DIP
CLC5523IM	-40°C to +85°C	8-pin Small outline
CLC5523IMX	-40°C to +85°C	8-pin Small outline tape and reel

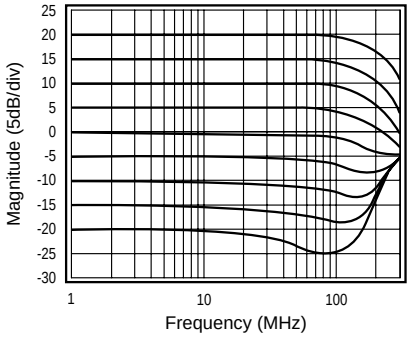
Contact the factory for other packages.

Package Thermal Resistance

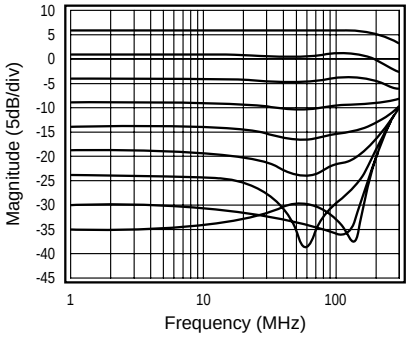
Package	θ_{JC}	θ_{JA}
DIP (IN)	65°C/W	115°C/W
Small Outline (IM)	55°C/W	135°C/W

CLC5523 Typical Performance (V_G = +2V, R_f = 1kΩ, R_g = 100Ω, R_L = 100Ω, V_o = 0.5V_{pp}; unless specified)

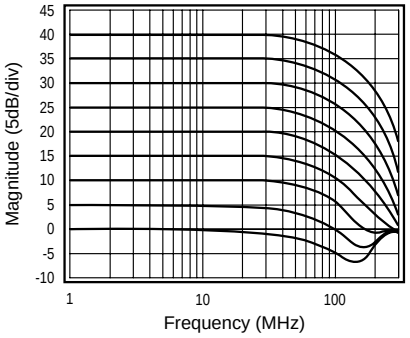
Frequency Response (A_{vmax} =10)



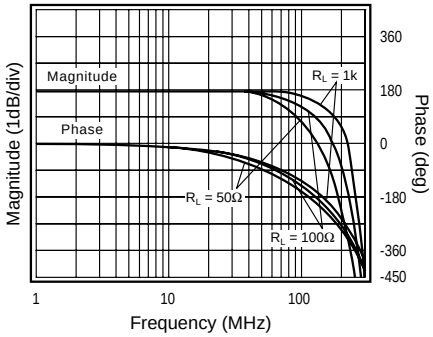
Frequency Response (A_{vmax} = 2)



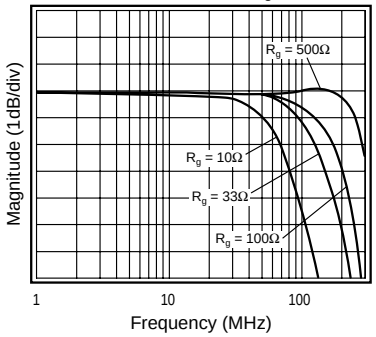
Frequency Response (A_{vmax} = 100)



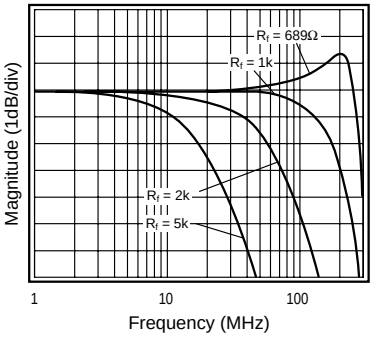
Frequency Response vs. R_L



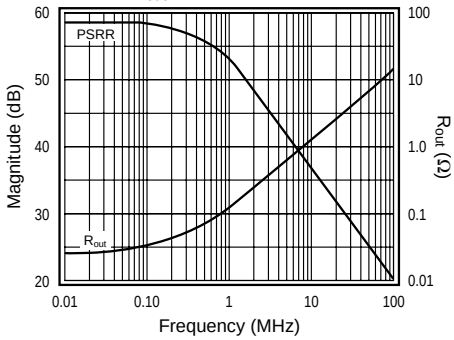
Frequency Response vs. R_g



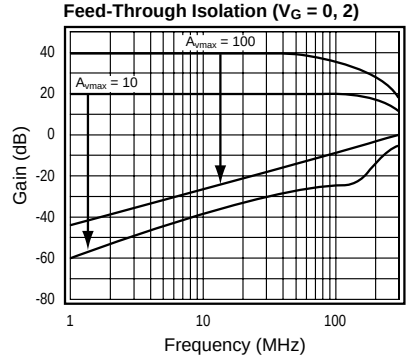
Frequency Response vs. R_f



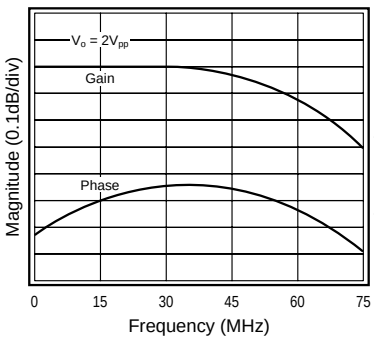
PSRR & R_{out}



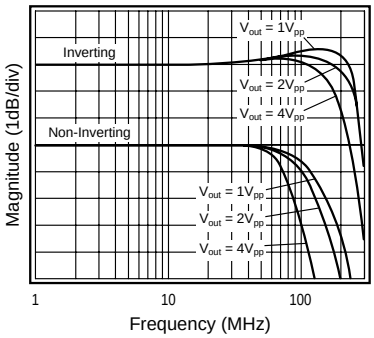
Feed-Through Isolation (V_G = 0, 2)



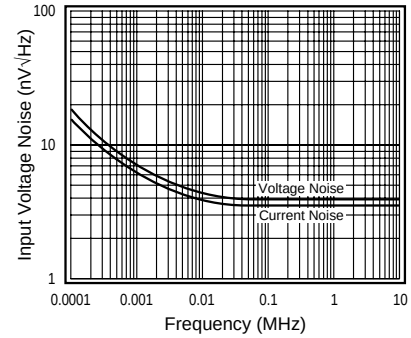
Gain Flatness & Linear Phase Deviation



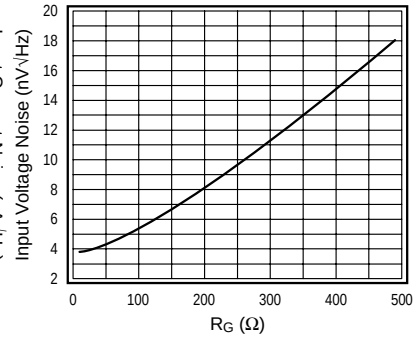
Large Signal Frequency Response



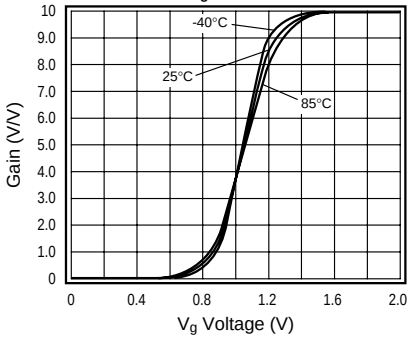
Equivalent Input Noise



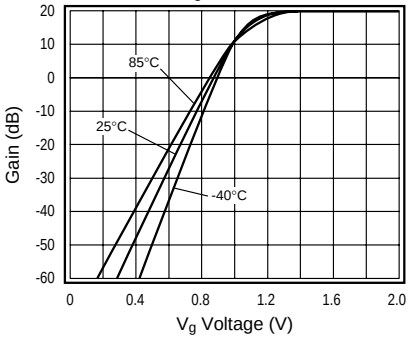
Input Referred Total Noise



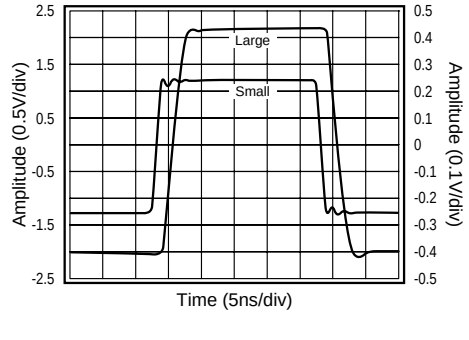
Gain (V/V) vs. V_g



Gain (dB) vs. V_g

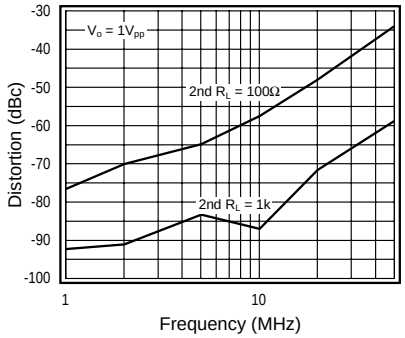


Large & Small Signal Pulse Response

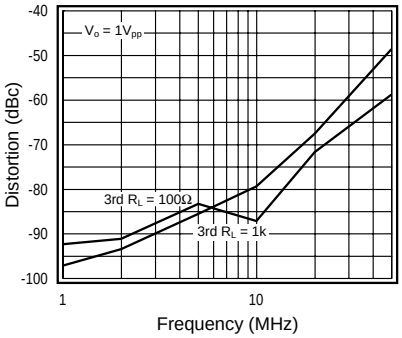


CLC5523 Typical Performance (V_G = +2V, R_f = 1kΩ, R_g = 100Ω, A_{vmax} = 10; unless specified)

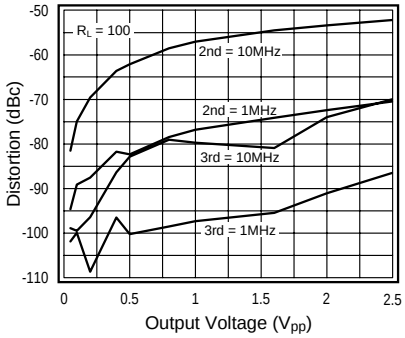
2nd Harmonic Distortion vs. Frequency



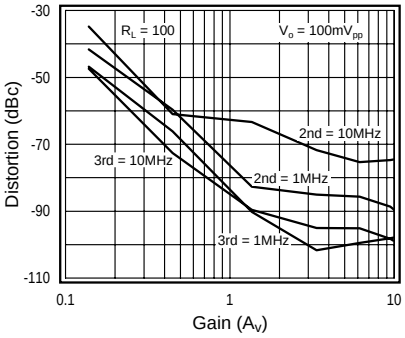
3rd Harmonic Distortion vs. Frequency



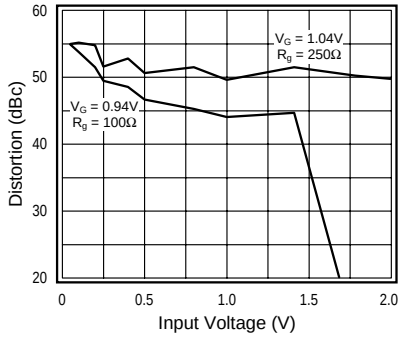
Harmonic Distortion vs. Output Voltage



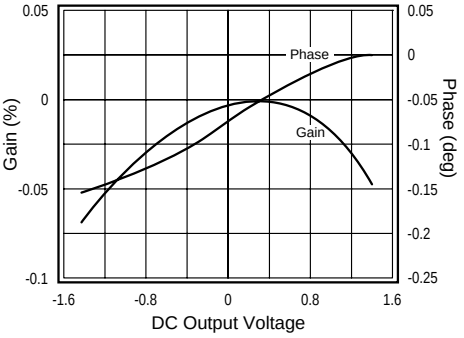
Harmonic Distortion vs. Gain



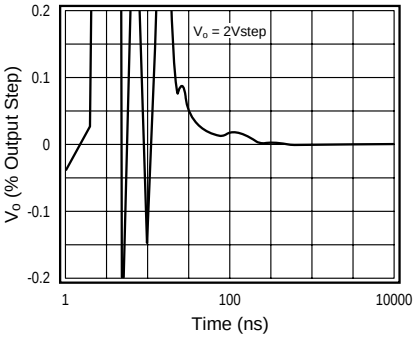
Input Harmonic Distortion (A_v = 2)



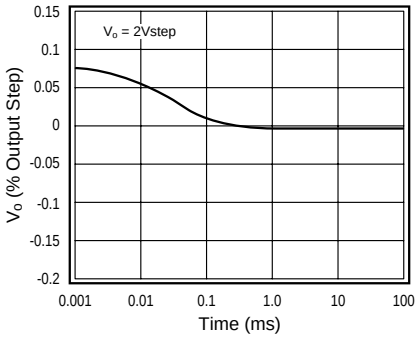
Differential Gain & Phase (NTSC)



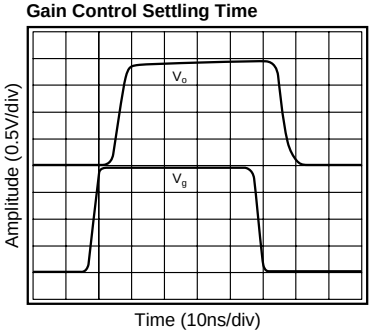
Short Term Settling Time



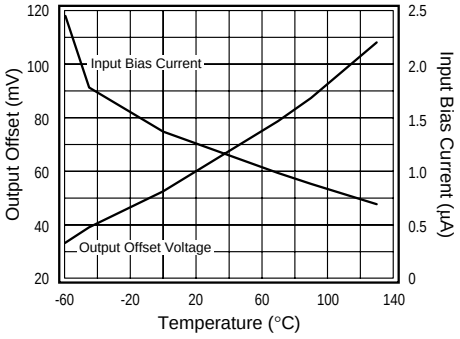
Long Term Settling Time



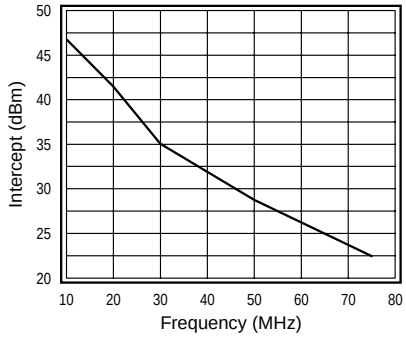
Gain Control Settling Time



DC Offset vs. Temperature



2nd Tone, 3rd Order Intermod Intercept



CLC5523 Operation

The key features of the CLC5523 are:

- Low Power
- Broad voltage controlled gain and attenuation range
- Bandwidth independent, resistor programmable gain range
- Broad signal and gain control bandwidths
- Frequency response may be adjusted with R_f
- High Impedance signal and gain control Inputs

The CLC5523 combines a closed loop input buffer, a voltage controlled variable gain cell and an output amplifier. The input buffer is a transconductance stage whose gain is set by the gain setting resistor, R_g. The output amplifier is a current feedback op amp and is configured as a transimpedance stage whose gain is set by, and equal to, the feedback resistor, R_f. The maximum gain, A_{vmax}, of the CLC5523 is defined by the ratio; R_f / R_g. As the gain control input (V_G) is adjusted over its 0 to 2V range, the gain is adjusted over a range of 80dB relative to the maximum set gain.

Setting the CLC5523 Maximum Gain

$$A_{vmax} = \frac{R_f}{R_g}$$

Although the CLC5523 is specified at A_{vmax} = 10, the recommended A_{vmax} varies between 2 and 100. Higher gains are possible but usually impractical due to output offsets, noise and distortion. When varying A_{vmax} several tradeoffs are made:

R_g: determines the input voltage range
R_f: determines overall bandwidth

The amount of current which the input buffer can source into R_g is limited and is specified in the $I_{R_g max}$ spec. This sets the maximum input voltage:

$$V_{in}(max) = I_{R_g max} \cdot R_g$$

The effects of maximum input range on harmonic distortion are illustrated in the *Input Harmonic Distortion* plot. Variations in R_g will also have an effect on the small signal bandwidth due to its loading of the input buffer and can be seen in *Frequency Response vs. R_g*. Changes in R_f will have a more dramatic effect on the small signal bandwidth. The output amplifier of the CLC5523 is a current feedback amplifier(CFA) and its bandwidth is determined by R_f. As with any CFA, doubling the feedback resistor will roughly cut the bandwidth of the device in half (refer to the plot *Frequency Response vs. R_f*). For more information covering CFA's, there is a basic tutorial, OA-20, *Current Feedback Myths Debunked* or a more rigorous analysis, OA-13, *Current Feedback Amplifier Loop Gain Analysis and Performance Enhancements*.

Using the CLC5523 in AGC Applications

In AGC applications, the control loop forces the CLC5523 to have a fixed output amplitude. The input amplitude will vary over a wide range and this can be the issue that limits dynamic range. At high input amplitudes, the distortion due to the input buffer driving R_g may exceed that which is produced by the output amplifier driving the load. In the plot, *Harmonic Distortion vs. Gain*, second and third harmonic distortion are plotted over a gain range of nearly 40dB for a fixed output amplitude of $100mV_{pp}$ in the specified configuration, R_f = 1k, R_g = 100Ω. When the gain is adjusted to 0.1 (i.e. 40dB down from A_{vmax}), the input amplitude would be $1V_{pp}$ and we can see the distortion is at its worst at this gain. If the output amplitude of the AGC were to be raised above 100mV, the input amplitudes for gains 40dB down from A_{vmax} would be even higher and the distortion would degrade further. It is for this reason that we recommend lower output amplitudes if wide gain ranges are desired. Using a post-amp like the CLC404 or CLC409 would be the best way to preserve dynamic range and yield output amplitudes much higher than $100mV_{pp}$.

Another way of addressing distortion performance and its limitations on dynamic range, would be to raise the value of R_g. Just like any other high-speed amplifier, by increasing the load resistance, and therefore decreasing the demanded load current, the distortion performance will be improved in most cases. With an increased R_g, R_f will also have to be increased to keep the same A_{vmax} and this will decrease the overall bandwidth.

Gain Partitioning

If high levels of gain are needed, gain partitioning should be considered.

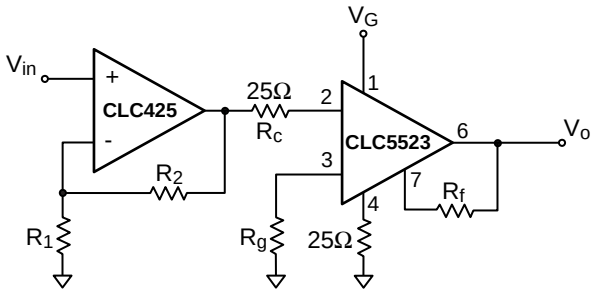


Figure 1: Gain Partitioning

The maximum gain range for this circuit is given by the following equation:

$$\text{maximum gain} = \left(1 + \frac{R_2}{R_1}\right) \cdot \left(\frac{R_f}{R_g}\right)$$

The CLC425 is a low noise wideband voltage feedback amplifier. Setting R2 at 909Ω and R1 at 100Ω produces a gain of 20dB. Setting R_f at 1000Ω as recommended and R_g at 50Ω, produces a gain of 26dB in the CLC5523. The total gain of this circuit is therefore approximately 46dB. It is important to understand that when partitioning to obtain high levels of gain, very small signal levels will drive the amplifiers to full scale output. For example, with 46dB of gain, a 20mV signal at the input will drive the output of the CLC425 to 200mV, the output of the CLC5523 to 4V. Accordingly, the designer must carefully consider the contributions of each stage to the overall characteristics. Through gain partitioning the designer is provided with an opportunity to optimize the frequency response, noise, distortion, settling time, and loading effects of each amplifier to achieve improved overall performance.

CLC5523 Gain Control Range and Minimum Gain

Before discussing Gain Control Range, it is important to understand the issues which limit it. The minimum gain of the CLC5523, theoretically, is zero, but in practical circuits is limited by the amount of feedthrough, here defined as the difference in output levels when V_G = 2V and when V_G = 0V. Capacitive coupling through the board and package as well as coupling through the supplies will determine the amount of feedthrough. Even at DC, the input signal will not be completely rejected. At high frequencies feedthrough will get worse because of its capacitive nature. At low frequencies, the feedthrough will be 80dB below the maximum gain, and therefore it can be said that the CLC5523 has an 80dB Gain Control Range.

CLC5523 Gain Control Function

In the two plots, *Gain vs. V_G*, we can see the gain as a function of the control voltage. The first plot, sometimes referred to as the S-curve, is the linear (V/V) gain. This is a hyperbolic tangent relationship. The second gain curve plots the gain in dB and is linear over a wide range of gains. Because of this, the CLC5523 gain control is referred to as “linear-in-dB.”

For applications where the CLC5523 will be used at the heart of a closed loop AGC circuit, the S-curve control characteristic provides a broad linear (in dB) control range with soft limiting at the highest gains where large changes in control voltage result in small changes in gain. For applications, requiring a fully linear (in dB) control characteristic, use the CLC5523 at half gain and below ($V_G \leq 1V$).

Avoiding Overdrive of the CLC5523 Gain Control Input

There is an additional requirement for the CLC5523 Gain Control Input (V_G): V_G must not exceed +2.5V. The gain control circuitry may saturate and the gain may actually be reduced. In applications where V_G is being driven from a DAC, this can easily be addressed in the software. If there is a linear loop driving V_G, such as an AGC loop, other methods of limiting the input voltage should be implemented. One simple solution is to place a 2:1 resistive divider on the V_G input. If the device driving this divider is operating off of ±5V supplies as well, its output will not exceed 5V and through the divider V_G can not exceed 2.5V.

Improving the CLC5523 Large Signal Performance

Figure 2 illustrates an inverting gain scheme for the CLC5523.

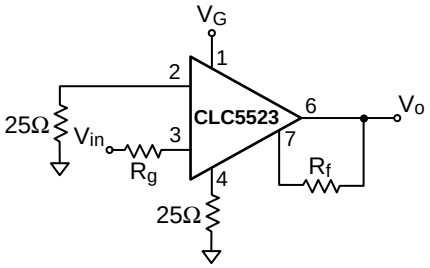


Figure 2: Inverting the CLC5523

The input signal is applied through the R_g resistor. The V_{in} pin should be grounded through a 25Ω resistor. The maximum gain range of this configuration is given in the following equation:

$$A_{vmax} = -\left(\frac{R_f}{R_g}\right)$$

The inverting slew rate of the CLC5523 is much higher than that of the non-inverting slew rate. This 2.5X performance improvement comes about because in the non-inverting configuration, the slew rate of the overall amplifier is limited by the input buffer. In the inverting circuit, the input buffer remains at a fixed voltage and does not affect slew rate.

Transmission Line Matching

One method for matching the characteristic impedance of a transmission line is to place the appropriate resistor at the input or output of the amplifier. Figure 3 shows a typical circuit configuration for matching transmission lines.

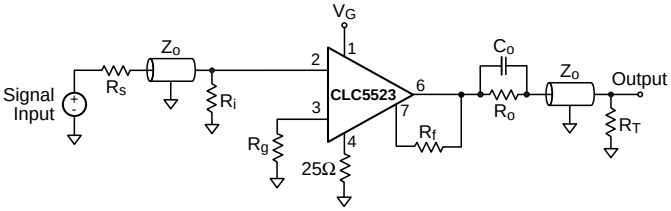


Figure 3: Transmission Line Matching

The resistors R_S, R_i, R_o, and R_T are equal to the characteristic impedance, Z_o, of the transmission line or cable. Use C_o to match the output transmission line over a greater frequency range. It compensates for the increase of the op amp’s output impedance with frequency.

Minimizing Parasitic Effects on Small Signal Bandwidth

The best way to minimize parasitic effects is to use the small outline package and surface mount components. For designs utilizing through-hole components, specifically axial resistors, resistor self-capacitance should be considered. Example: the average magnitude of parasitic capacitance of RN55D 1% metal film resistors is about 0.15pF with variations of as much as 0.1pF between lots. Given the CLC5523's extended bandwidth, these small parasitic reactance variations can cause measurable frequency response variations in the highest octave. We therefore recommend the use of surface mount resistors to minimize these parasitic reactance effects. If an axial component is preferred, we recommend PRP8351 resistors which are available from Precision Resistive Products, Inc., Highway 61 South, Mediapolis, Iowa.

Small Signal Response at Low A_{vmax}

When the maximum gain, as set by R_g and R_f, is greater than or equal to A_{vmax} = 10, little or no peaking should be observed in the amplifier response. When the gain range is set to less than A_{vmax} = 10, some peaking may be observed at higher frequencies. At gain ranges of $2 \le A_{vmax} \le 10$ peaking can be minimized by increasing R_f. At gain ranges of $A_{vmax} < 2$ peaking reaches approximately 6dB in the upper octave.

If peaking is observed with the recommended R_f resistor, and a small increase in the R_f resistor does not solve the problem, then investigate the possible causes and remedies listed below.

- **Capacitance across R_f**
  - Do not place a capacitor across R_f
  - Keep traces connecting R_f separated and as short as possible
- **Capacitive Loads**
  - Place a small resistor (20-50Ω) between the output and C_L
- **Long traces and/or lead lengths between R_f and the CLC5523**
  - Keep these traces as short as possible
- **Long traces between CLC5523 and 0.1μF bypass capacitors**
  - Keep these traces less than 0.2 inches (5mm)
  - For the devices in the PDIP package, an additional 1000pF monolithic capacitor should be placed less than 0.1" (3mm) from the pin
- **Extra capacitance between the R_g pin and ground (C_G)**
  - See the *Printed Circuit Board Layout* sub-section below for suggestions on reducing C_G
  - Increase R_f if peaking is still observed after reducing C_G
- **Non-inverting input pin connected directly to ground**
  - Place a 50 to 200Ω resistor between the non-inverting pin and ground

Adjusting Offsets and DC Level Shifting

Offsets can be broken into two parts: an input-referred term and an output-referred term. These errors can be trimmed using the circuit in Figure 4. First set V_G to 0V and adjust the trim pot R4 to null the offset voltage at the output. This will eliminate the output stage offsets. Next set V_G to 2V and adjust the trim pot R1 to null the offset voltage at the output. This will eliminate the input stage offsets.

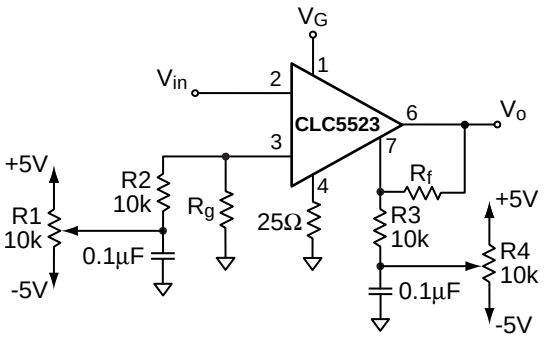


Figure 4: Offset Adjust Circuit

Printed Circuit Board Layout

High frequency op amp performance is strongly dependent on proper layout, proper resistive termination and adequate power supply decoupling. The most important layout points to follow are:

- Use a ground plane
- Bypass each power supply pin with these capacitors:
  - a high-quality 0.1µF ceramic capacitor placed less than 0.2" (5mm) from the pin
  - a 6.8µF tantalum capacitor less than 2" (50mm) from the pin
  - for the plastic DIP package, a high-quality 1000pF ceramic capacitor placed less than 0.1" (3mm) from the pin

Capacitively bypassing power pins to a good ground plane with a minimum of trace length (inductance) is necessary for any high speed device, but it is particularly important for the CLC5523.

- Establish wide, low impedance, power supply traces
- For the plastic DIP package, a 25Ω resistor should be connected from pin 4 to ground with a minimum length trace
- Minimize or eliminate sources of capacitance between the R_f pin and the output pin. Avoid adjacent feedthrough vias between the R_f and output leads since such a geometry may give rise to a significant source of capacitance.
- Minimize trace and lead lengths for components between the inverting and output pins
  - Remove ground plane 0.1" (3mm) from all input/output pads
  - For prototyping, use flush-mount printed circuit board pins; *never use high profile DIP sockets*

To minimize high frequency distortion, other layout issues need be addressed:

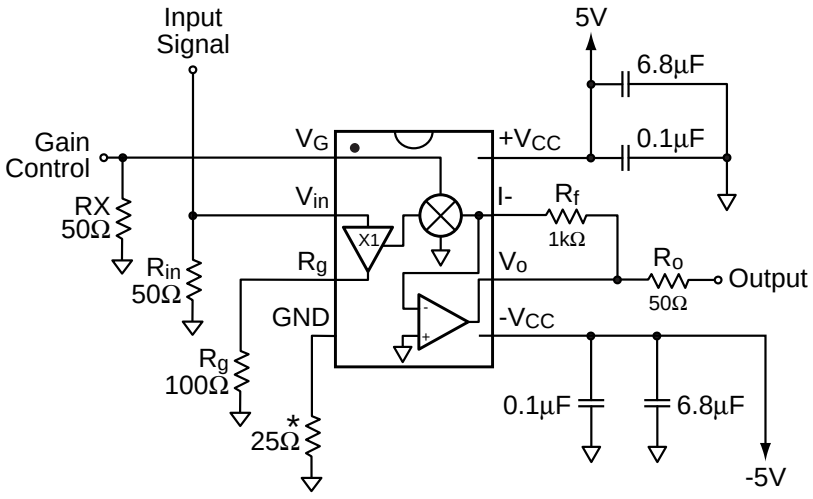
- Short, equal length, low impedance power supply return paths from the load to the supplies
- avoid returning output ground currents near the input stage.

Evaluation Boards

Evaluation boards are available for both the 8-pin DIP and small outline package types. Evaluation kits that contain an evaluation board and CLC5523 samples can be obtained by calling National Semiconductor's Customer Service Center at 1-800-272-9959. The 8-pin DIP evaluation kit part number is CLC730065. The 8-pin small outline evaluation kit part number is CLC730066.

The DIP evaluation kit has been designed to utilize axial lead components. The small outline evaluation kit has been designed to utilize surface mount components.

The circuit diagram shown in Figure 5, applies to both the DIP and the small outline evaluation boards.



* 25Ω series resistor is not required on the small outline device and does not appear on the small outline board

Figure 5: Evaluation Board Schematic

Comlinear Layer1

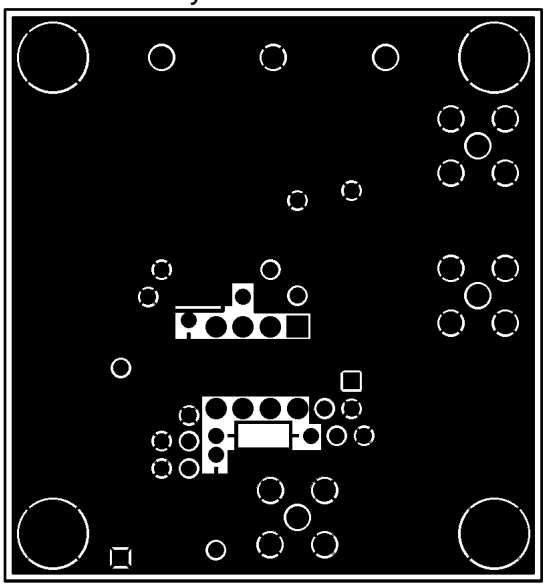


Figure 6: DIP Evaluation Board (Top Layer)

Comlinear Layer2

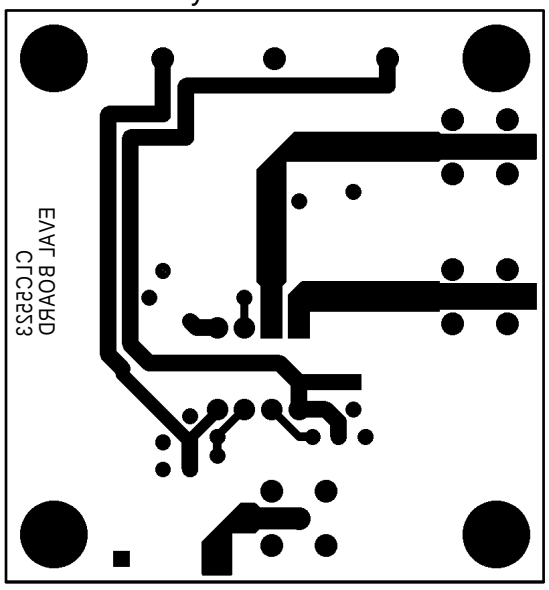


Figure 7: DIP Evaluation Board (Bottom Layer)

Comlinear Layer1 Silk

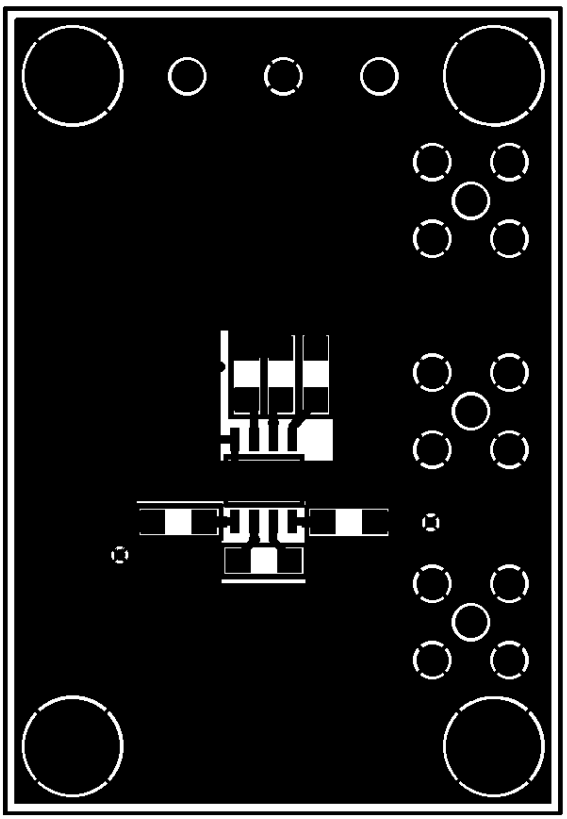


Figure 8: Small Outline Evaluation Board (Top Layer)

Comlinear Layer2 Silk

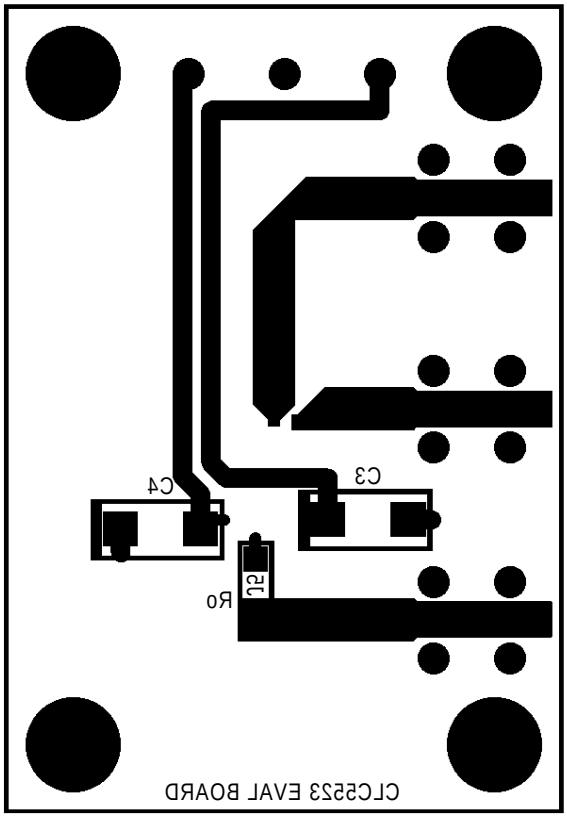


Figure 9: Small Outline Evaluation Board (Bottom Layer)

(Not drawn to scale)

Digital Gain Control

Digitally variable gain control can be easily realized by driving the CLC5523's gain control input with a digital-to-analog converter (DAC). Figure 10 illustrates such an application. This circuit employs National Semiconductor's eight-bit DAC0830, the LM351 JFET input op-amp, and the CLC5523 VGA. With V_{ref} set to 2V, the circuit provides up to 80dB of gain control in 512 steps with up to 0.05% full scale resolution. The maximum gain of this circuit is 20dB.

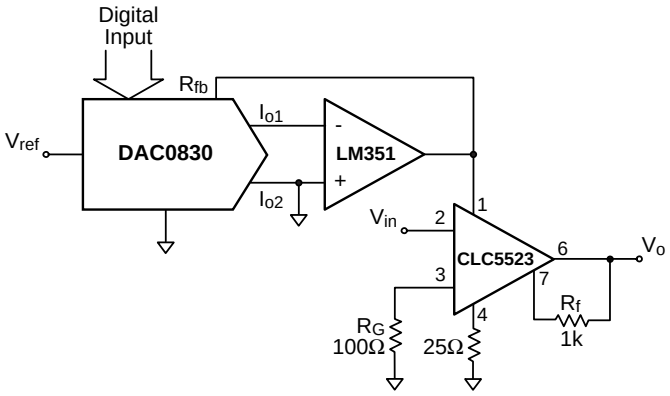


Figure 10: Digital Gain Control

Automatic Gain Control (AGC) #1

Fast Response AGC Loop

The AGC circuit shown in Figure 11 will correct a 6dB input amplitude step in 100ns. The circuit includes a two op-amp precision rectifier amplitude detector (U1 and U2), and an integrator (U3) to provide high loop gain at low frequencies. The output amplitude is set by R9.

Some notes on building fast AGC loops:

Precision rectifiers work best with large output signals. Accuracy is improved by blocking DC offsets, as shown in Figure 11.

Signal frequencies must not reach the gain control port of the CLC5523, or the output signal will be distorted (modulated by itself). A fast settling AGC needs additional filtering beyond the integrator stage to block signal frequencies. This is provided in Figure 11 by a simple R-C filter (R10 and C3); better distortion performance can be achieved with a more complex filter. These filters should be scaled with the input signal frequency. Loops with slower response time (longer integration time constants) may not need the R10 – C3 filter.

Checking the loop stability can be done by monitoring the V_g voltage while applying a step change in input signal amplitude. Changing the input signal amplitude can be easily done with either an arbitrary waveform generator or a fast multiplexer such as the CLC532.

Automatic Gain Control (AGC) #2

Figure 12 on the following page, illustrates an automatic gain control circuit that employs two CLC5523's. In this circuit, U1 receives the input signal and produces an output signal of constant amplitude. U2 is configured to provide negative feedback. U2 generates a rectified gain control signal that works against an adjustable bias level which may be set by the potentiometer and R_b. C_i integrates the bias and negative feedback. The resultant gain control signal is applied to the U1 gain control input V_g. The bias adjustment allows the U1 output to be set at an arbitrary level less than the maximum output specification of the amplifier. Rectification is accomplished in U2 by driving both the amplifier input and the gain control input with the U1 output signal. The voltage divider that is formed by R1, R2 and the V_g input (pin 1) resistance, sets the rectifier gain.

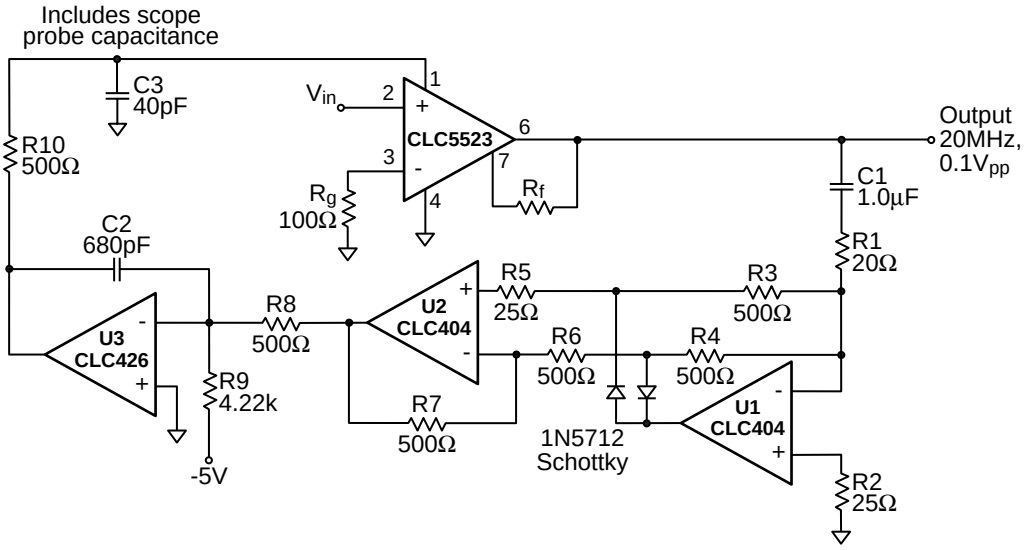


Figure 11: Automatic Gain Control Circuit #1

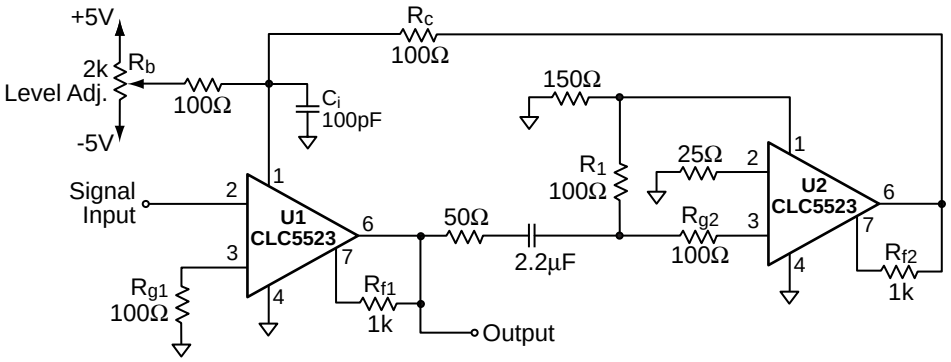


Figure 12: Automatic Gain Control Circuit #2

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