

CLC453

Single Supply, Low-Power, High Output, Programmable Buffer

General Description

The CLC453 is a low cost, high speed (110MHz) buffer that features user-programmable gains of +2, +1, and -1V/V. It has a new output stage that delivers high output drive current (100mA), but consumes minimal quiescent supply current (3.0mA) from a single 5V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a programmable range of gains and wide signal levels, and has a linear-phase response up to one half of the -3dB frequency. The CLC453's internal feedback network provides an excellent gain accuracy of 0.3%

The CLC453 offers superior dynamic performance with a 110MHz small-signal bandwidth, 370V/ μ s slew rate and 4.8ns rise/fall times ($2V_{step}$). The combination of the small SOT23-5 package, low quiescent power, high output current drive, and high-speed performance make the CLC453 well suited for many battery-powered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, makes the CLC453 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC453 will drive a 100 Ω load with only -72/-74dBc second/third harmonic distortion ($A_v = +2$, $V_{out} = 2V_{pp}$, $f = 1\text{MHz}$). With a 25 Ω load, and the same conditions, it produces only -65/-77dBc second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.

When driving the input of high-resolution A/D converters, the CLC453 provides excellent -65/-84dBc second/third harmonic distortion ($A_v = +2$, $V_{out} = 2V_{pp}$, $f = 1\text{MHz}$, $R_L = 1k\Omega$) and fast settling time.

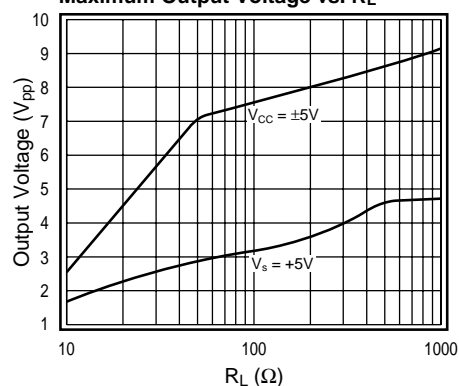
Features

- 100mA output current
- 3.0mA supply current
- 110MHz bandwidth ($A_v = +2$)
- -65/-84dBc HD2/HD3 (1MHz)
- 25ns settling to 0.05%
- 370V/ μ s slew rate
- Stable for capacitive loads up to 1000pF
- Single 5V to $\pm 5\text{V}$ supplies
- Available in Tiny SOT23-5 package

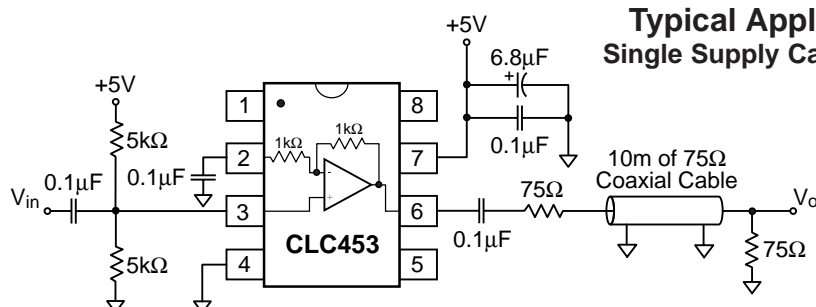
Applications

- Coaxial cable driver
- Twisted pair driver
- Transformer/Coil Driver
- High capacitive load driver
- Video line driver
- Portable/battery-powered applications
- A/D driver

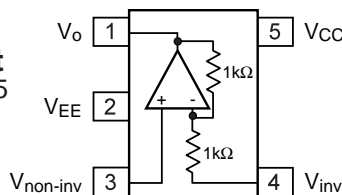
Maximum Output Voltage vs. R_L



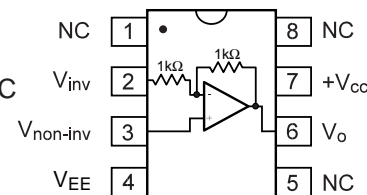
Typical Application Single Supply Cable Driver



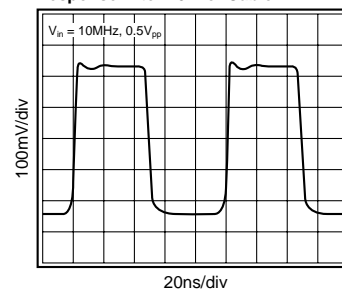
Pinout
SOT23-5



Pinout
DIP & SOIC



Response After 10m of Cable



+5V Electrical Characteristics (A_v = +2, R_L = 100Ω, V_s = +5V¹, V_{cm} = V_{EE} + (V_s/2), R_L tied to V_{cm}, unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS				UNITS	NOTES
Ambient Temperature	CLC453AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C			
FREQUENCY DOMAIN RESPONSE								
-3dB bandwidth	V _o = 0.5V _{pp}	110	80	75	70		MHz	
	V _o = 2.0V _{pp}	90	75	72	70		MHz	
-0.1dB bandwidth	V _o = 0.5V _{pp}	25	22	22	18		MHz	
gain peaking	<200MHz, V _o = 0.5V _{pp}	0	0.5	0.9	1.0		dB	
gain rolloff	<30MHz, V _o = 0.5V _{pp}	0.2	0.5	0.6	0.6		dB	
linear phase deviation	<30MHz, V _o = 0.5V _{pp}	0.1	2	3	3		deg	
TIME DOMAIN RESPONSE								
rise and fall time	2V step	4.8	6.4	6.8	7.3		ns	
settling time to 0.05%	1V step	25	—	—	—		ns	
overshoot	2V step	9	13	16	16		%	
slew rate	2V step	370	280	250	240		V/μs	
DISTORTION AND NOISE RESPONSE								
2 nd harmonic distortion	2V _{pp} , 1MHz	-72	-66	-64	-64		dBc	
	2V _{pp} , 1MHz; R _L = 1kΩ	-65	-59	-57	-57		dBc	
	2V _{pp} , 5MHz	-65	-56	-54	-54		dBc	
3 rd harmonic distortion	2V _{pp} , 1MHz	-74	-70	-68	-68		dBc	
	2V _{pp} , 1MHz; R _L = 1kΩ	-84	-76	-74	-74		dBc	
	2V _{pp} , 5MHz	-60	-55	-53	-53		dBc	
equivalent input noise								
voltage (e _{ni})	>1MHz	2.8	3.5	3.8	3.8		nV/√Hz	
non-inverting current (i _{bn})	>1MHz	7.5	10	11	11		pA/√Hz	
inverting current (i _{bi})	>1MHz	10.5	14	15	15		pA/√Hz	
STATIC DC PERFORMANCE								
input offset voltage		13	30	35	35		mV	A
average drift		80	—	—	—		μV/°C	
input bias current (non-inverting)		5	18	22	24		μA	A
average drift		30	—	—	—		nA/°C	
gain accuracy		±0.3	±1.5	±2.0	±2.0		%	A
internal resistors (R _f , R _g)		1000	±20%	±26%	±30%		Ω	
power supply rejection ratio	DC	48	43	43	43		dB	
common-mode rejection ratio	DC	51	48	46	46		dB	
supply current	R _L = ∞	3.0	3.4	3.6	3.6		mA	A
MISCELLANEOUS PERFORMANCE								
input resistance (non-inverting)		0.39	0.28	0.25	0.25		MΩ	
input capacitance (non-inverting)		1.5	2.3	2.3	2.3		pF	
input voltage range, High		4.2	4.1	4.0	4.0		V	
input voltage range, Low		0.8	0.9	1.0	1.0		V	
output voltage range, High	R _L = 100Ω	4.0	3.9	3.8	3.8		V	
output voltage range, Low	R _L = 100Ω	1.0	1.1	1.2	1.2		V	
output voltage range, High	R _L = ∞	4.1	4.0	4.0	3.9		V	
output voltage range, Low	R _L = ∞	0.9	1.0	1.0	1.1		V	
output current		100	80	65	40		mA	B
output resistance, closed loop	DC	400	600	600	600		mΩ	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes

- A) J-level: spec is 100% tested at +25°C.
 B) The short circuit current can exceed the maximum safe output current.
 1) V_s = V_{CC} - V_{EE}

Absolute Maximum Ratings

supply voltage (V _{CC} - V _{EE})	+14V
output current (see note C)	140mA
common-mode input voltage	V _{EE} to V _{CC}
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C
ESD rating (human body model)	500V

Reliability Information

Transistor Count	49
MTBF (based on limited test data)	31Mhr

±5V Electrical Characteristics ($A_v = +2$, $R_L = 100\Omega$, $V_{CC} = \pm 5V$, unless specified)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC453AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	$V_o = 1.0V_{pp}$	130	105	95	90	MHz	
	$V_o = 4.0V_{pp}$	70	55	52	50	MHz	
-0.1dB bandwidth	$V_o = 1.0V_{pp}$	30	25	25	20	MHz	
gain peaking	<200MHz, $V_o = 1.0V_{pp}$	0	0.5	0.9	1.0	dB	
gain rolloff	<30MHz, $V_o = 1.0V_{pp}$	0.2	0.7	0.8	0.8	dB	
linear phase deviation	<30MHz, $V_o = 1.0V_{pp}$	0.1	0.2	0.3	0.3	deg	
differential gain	NTSC, $R_L = 150\Omega$	0.3	—	—	—	%	
differential phase	NTSC, $R_L = 150\Omega$	0.1	—	—	—	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	3.8	4.8	5.1	5.6	ns	
settling time to 0.05%	2V step	20	—	—	—	ns	
overshoot	2V step	6	10	13	13	%	
slew rate	2V step	460	340	315	300	V/ μ s	
DISTORTION AND NOISE RESPONSE							
2 nd harmonic distortion	$2V_{pp}$, 1MHz	-82	-74	-72	-72	dBc	
	$2V_{pp}$, 1MHz; $R_L = 1k\Omega$	-69	-63	-61	-61	dBc	
	$2V_{pp}$, 5MHz	-65	-59	-57	-57	dBc	
3 rd harmonic distortion	$2V_{pp}$, 1MHz	-73	-69	-67	-67	dBc	
	$2V_{pp}$, 1MHz; $R_L = 1k\Omega$	-90	-80	-78	-78	dBc	
	$2V_{pp}$, 5MHz	-60	-56	-54	-54	dBc	
equivalent input noise voltage (e_{ni})	>1MHz	2.8	3.5	3.8	3.8	nV/ \sqrt{Hz}	
non-inverting current (i_{bn})	>1MHz	7.5	10	11	11	pA/ \sqrt{Hz}	
inverting current (i_{bi})	>1MHz	10.5	14	15	15	pA/ \sqrt{Hz}	
STATIC DC PERFORMANCE							
output offset voltage		7	30	35	35	mV	
average drift		80	—	—	—	μ V/°C	
input bias current (non-inverting)		3	18	23	25	μ A	
average drift		40	—	—	—	nA/°C	
gain accuracy		± 0.3	± 1.5	± 2.0	± 2.0	%	
internal resistors (R_f , R_g)		1000	$\pm 20\%$	$\pm 26\%$	$\pm 30\%$	Ω	
power supply rejection ratio	DC	48	45	43	43	dB	
common-mode rejection ratio	DC	53	50	48	48	dB	
supply current	$R_L = \infty$	3.2	3.8	4.0	4.0	mA	
MISCELLANEOUS PERFORMANCE							
input resistance (non-inverting)		0.52	0.35	0.30	0.30	M Ω	
input capacitance (non-inverting)		1.2	1.8	1.8	1.8	pF	
common-mode input range		± 4.2	± 4.1	± 4.1	± 4.0	V	
output voltage range	$R_L = 100\Omega$	± 3.8	± 3.6	± 3.6	± 3.5	V	
output voltage range	$R_L = \infty$	± 4.0	± 3.8	± 3.8	± 3.7	V	
output current		130	100	80	50	mA	
output resistance, closed loop	DC	400	600	600	600	m Ω	B

Notes

B) The short circuit current can exceed the maximum safe output current.

Package Thermal Resistance

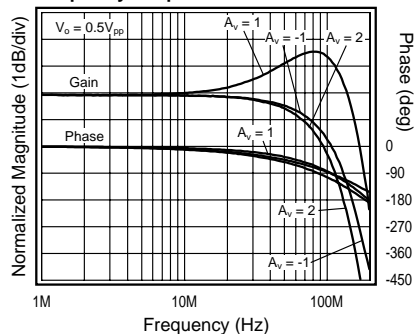
Package	θ_{JC}	θ_{JA}
Plastic (AJP)	115°C/W	125°C/W
Surface Mount (AJE)	130°C/W	150°C/W
Surface Mount (AJM5)	140°C/W	210°C/W
Dice (ALC)	25°C/W	—

Ordering Information

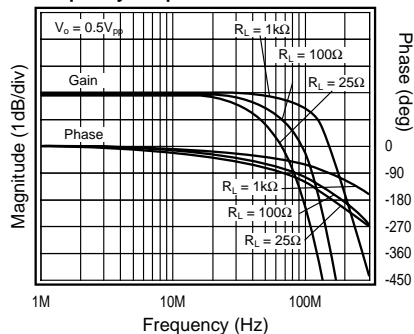
Model	Temperature Range	Description
CLC453AJP	-40°C to +85°C	8-pin PDIP
CLC453AJE	-40°C to +85°C	8-pin SOIC
CLC453AJM5	-40°C to +85°C	5-pin SOT
CLC453ALC	-40°C to +85°C	dice

+5V Typical Performance ($A_v = +2$, $R_L = 100\Omega$, $V_s = +5V^1$, $V_{cm} = V_{EE} + (V_s/2)$, R_L tied to V_{cm} , unless specified)

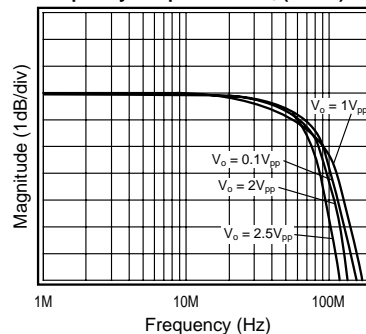
Frequency Response



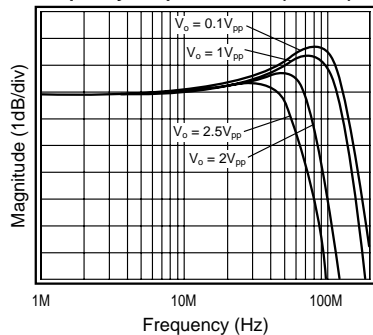
Frequency Response vs. R_L



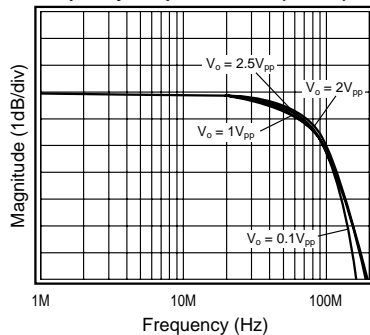
Frequency Response vs. V_o ($A_v = 2$)



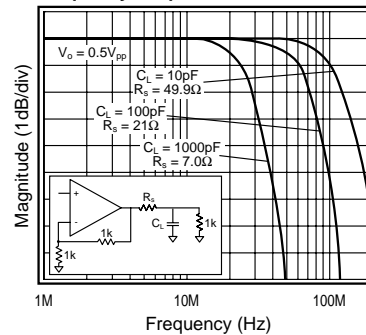
Frequency Response vs. V_o ($A_v = +1$)



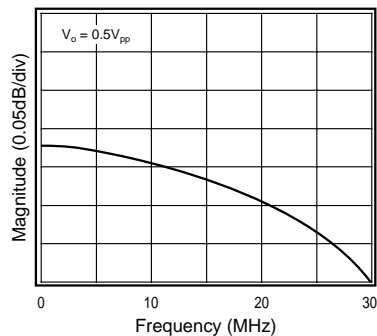
Frequency Response vs. V_o ($A_v = -1$)



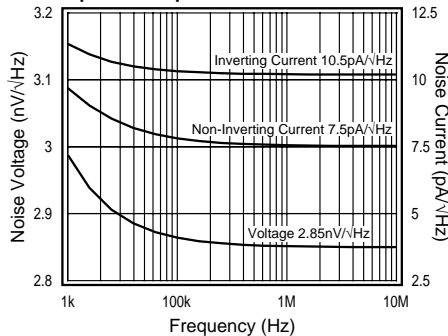
Frequency Response vs. C_L



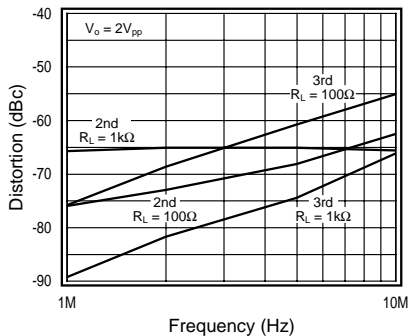
Gain Flatness



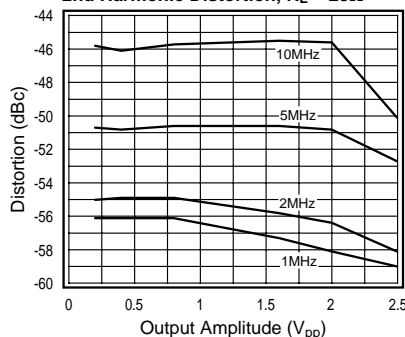
Equivalent Input Noise



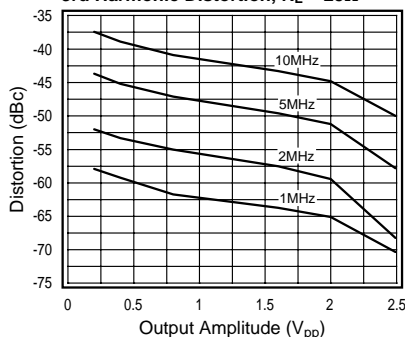
2nd & 3rd Harmonic Distortion



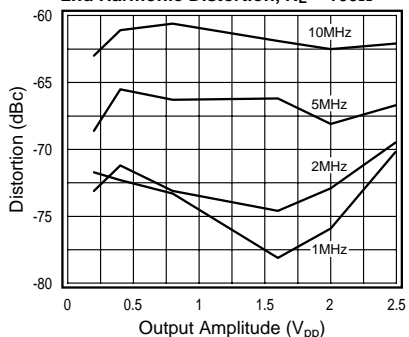
2nd Harmonic Distortion, $R_L = 25\Omega$



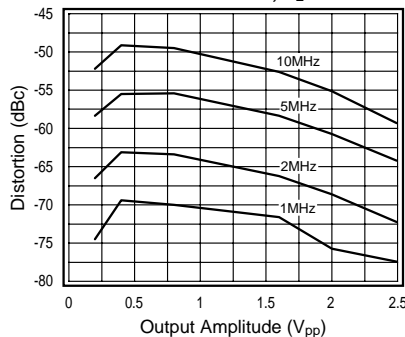
3rd Harmonic Distortion, $R_L = 25\Omega$



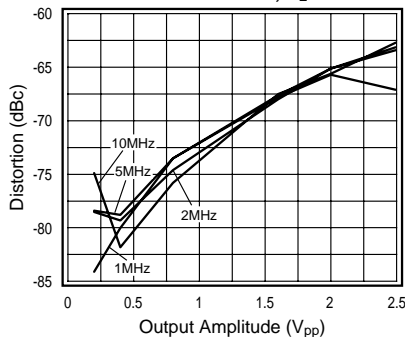
2nd Harmonic Distortion, $R_L = 100\Omega$



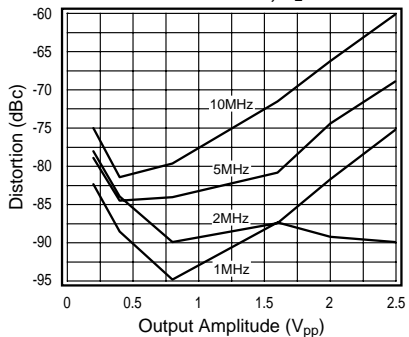
3rd Harmonic Distortion, $R_L = 100\Omega$



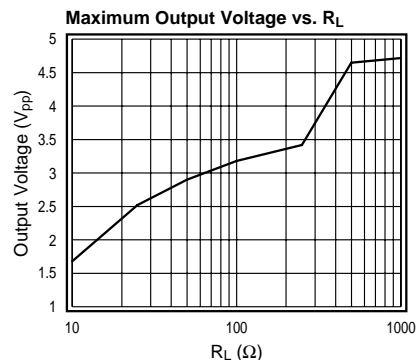
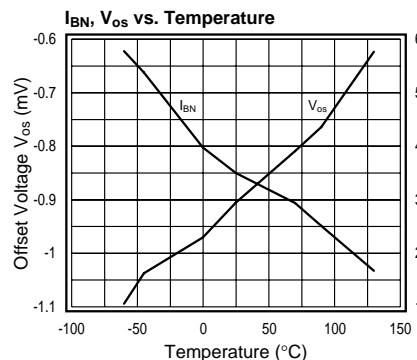
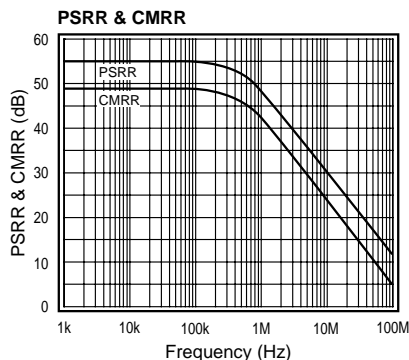
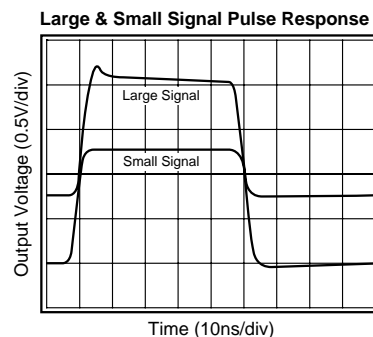
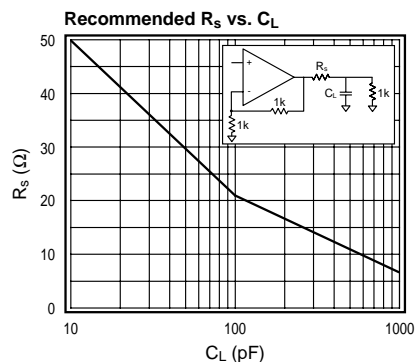
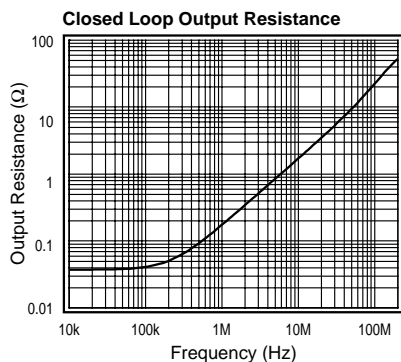
2nd Harmonic Distortion, $R_L = 1k\Omega$



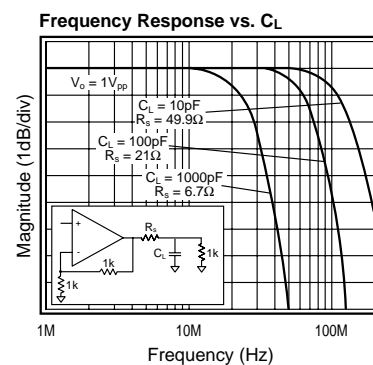
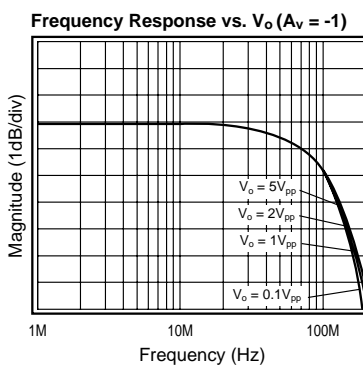
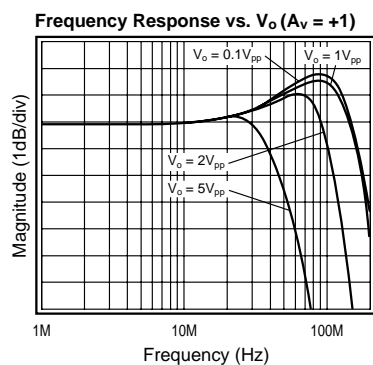
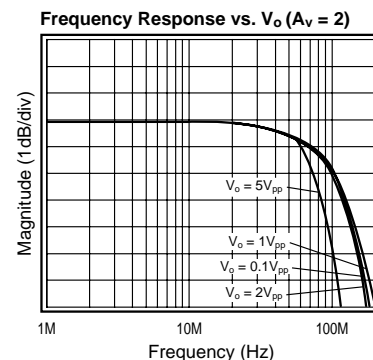
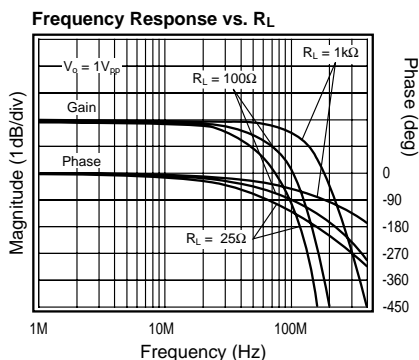
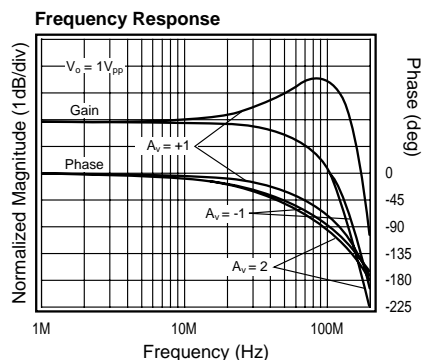
3rd Harmonic Distortion, $R_L = 1k\Omega$



+5V Typical Performance ($A_v = +2$, $R_L = 100\Omega$, $V_s = +5V$, $V_{cm} = V_{EE} + (V_s/2)$, R_L tied to V_{cm} , unless specified)

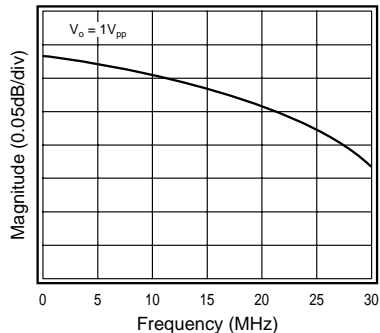


±5V Typical Performance ($A_v = +2$, $R_L = 100\Omega$, $V_{CC} = \pm 5V$, unless specified)

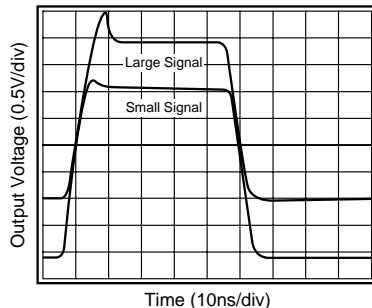


±5V Typical Performance ($A_v = +2$, $R_L = 100\Omega$, $V_{CC} = \pm 5V$, unless specified)

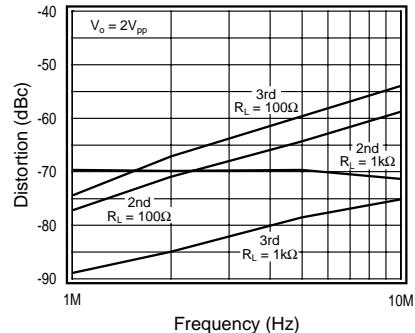
Gain Flatness



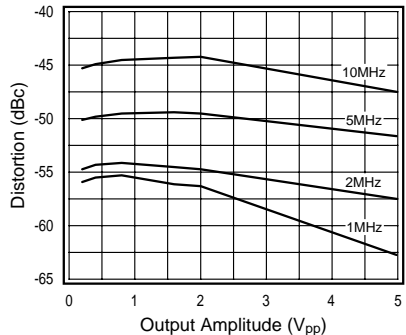
Large & Small Signal Pulse Response



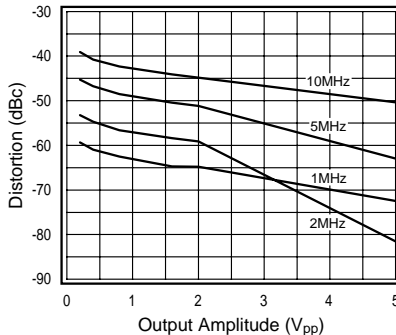
2nd & 3rd Harmonic Distortion



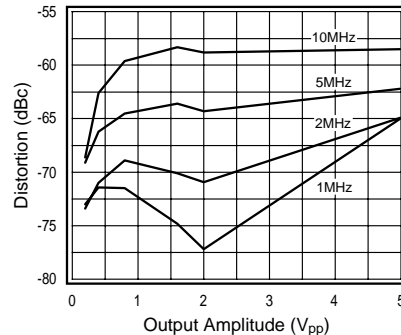
2nd Harmonic Distortion, $R_L = 25\Omega$



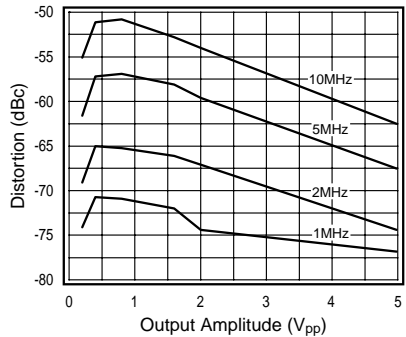
3rd Harmonic Distortion, $R_L = 25\Omega$



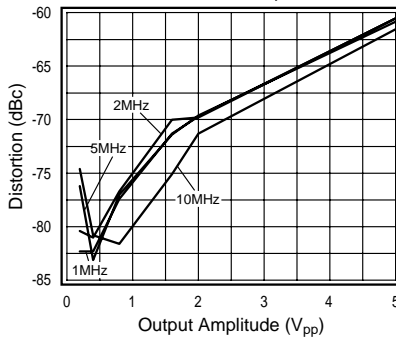
2nd Harmonic Distortion, $R_L = 100\Omega$



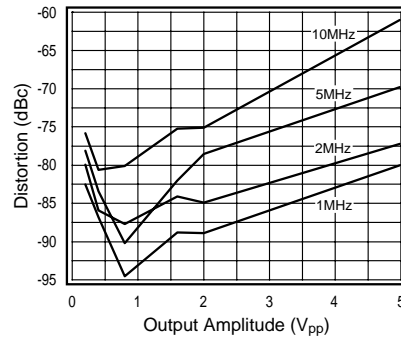
3rd Harmonic Distortion, $R_L = 100\Omega$



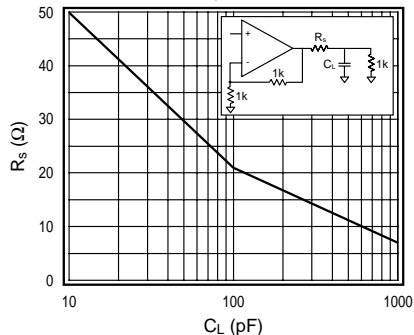
2nd Harmonic Distortion, $R_L = 1k\Omega$



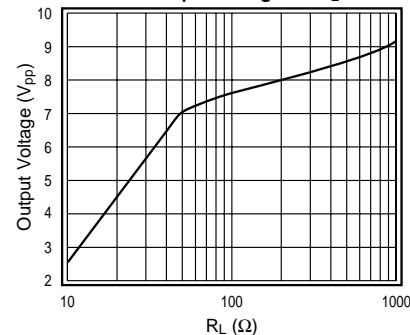
3rd Harmonic Distortion, $R_L = 1k\Omega$



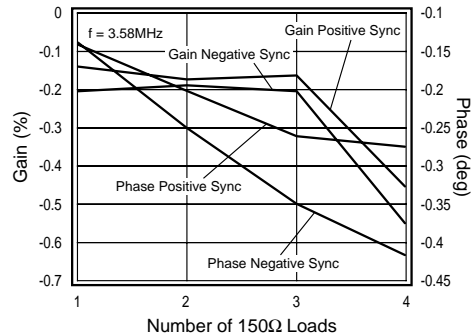
Recommended R_s vs. C_L



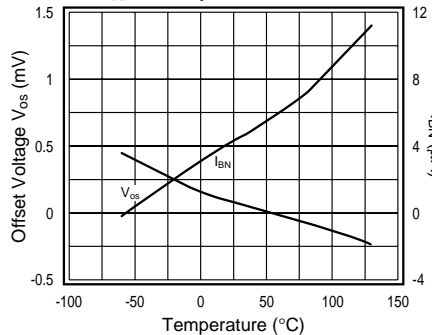
Maximum Output Voltage vs. R_L



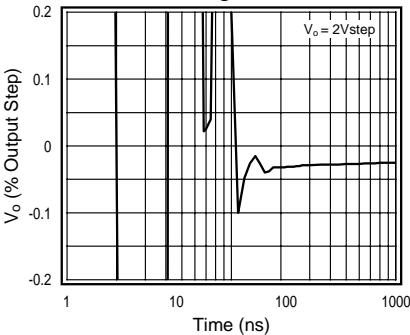
Differential Gain & Phase



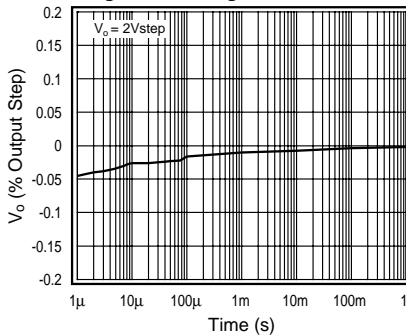
I_{BN} , V_{OS} vs. Temperature



Short Term Settling Time



Long Term Settling Time



CLC453 Operation

The CLC453 is a current feedback buffer built in an advanced complementary bipolar process. The CLC453 operates from a single 5V supply or dual $\pm 5V$ supplies. Operating from a single 5V supply, the CLC453 has the following features:

- Gains of +1, -1, and 2V/V are achievable without external resistors
- Provides 100mA of output current while consuming only 15mW of power
- Offers low -65/-84dBc 2nd and 3rd harmonic distortion
- Provides BW > 80MHz and 1MHz distortion < -70dBc at $V_o = 2V_{pp}$

The CLC453 performance is further enhanced in $\pm 5V$ supply applications as indicated in the ***$\pm 5V$ Electrical Characteristics*** table and ***$\pm 5V$ Typical Performance*** plots.

If gains other than +1, -1, or +2V/V are required, then the CLC452 can be used. The CLC452 is a current feedback amplifier with near identical performance and allows for external feedback and gain setting resistors.

Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with feedback resistor
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$\frac{V_o}{V_{in}} = \frac{A_v}{1 + \frac{R_f}{Z(j\omega)}} \quad \text{Equation 1}$$

where:

- A_v is the closed loop DC voltage gain
- R_f is the feedback resistor
- $Z(j\omega)$ is the CLC453's open loop transimpedance gain
- $\frac{Z(j\omega)}{R_f}$ is the loop gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the -3dB corner frequency, the interaction between R_f and $Z(j\omega)$ dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing R_f has the following affects:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

CLC453 Design Information

Closed Loop Gain Selection

The CLC453 is a current feedback op amp with $R_f = R_g = 1k\Omega$ on chip (in the package). Select from three closed loop gains without using any external gain or feedback resistors. Implement gains of +2, +1, and -1V/V by connecting pins 2 and 3 as described in the chart below.

Gain A_v	Input Connections	
	Non-Inverting (pin3)	Inverting (pin2)
-1V/V	ground	input signal
+1V/V	input signal	NC (open)
+2V/V	input signal	ground

The gain accuracy of the CLC453 is excellent and stable over temperature change. The internal gain setting resistors, R_f and R_g are diffused silicon resistors with a process variation of $\pm 20\%$ and a temperature coefficient of $\sim 2000\text{ppm}/^\circ\text{C}$. Although their absolute values change with processing and temperature, their ratio (R_f/R_g) remains constant. If an external resistor is used in series with R_g , gain accuracy over temperature will suffer.

Single Supply Operation ($V_{CC} = +5V$, $V_{EE} = \text{GND}$)

The specifications given in the ***$\pm 5V$ Electrical Characteristics*** table for single supply operation are measured with a common mode voltage (V_{cm}) of 2.5V. V_{cm} is the voltage around which the inputs are applied and the output voltages are specified.

Operating from a single +5V supply, the Common Mode Input Range (CMIR) of the CLC453 is typically +0.8V to +4.2V. The typical output range with $R_L = 100\Omega$ is +1.0V to +4.0V.

For single supply DC coupled operation, keep input signal levels above 0.8V DC. For input signals that drop below 0.8V DC, AC coupling and level shifting the signal are recommended. The non-inverting and inverting configurations for both input conditions are illustrated in the following 2 sections.

DC Coupled Single Supply Operation

Figures 1, 2, and 3 on the following page, show the recommended configurations for input signals that remain above 0.8V DC.

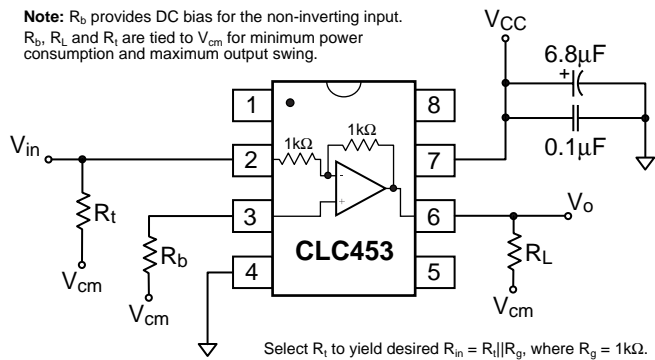


Figure 1: DC Coupled, $A_v = -1V/V$ Configuration

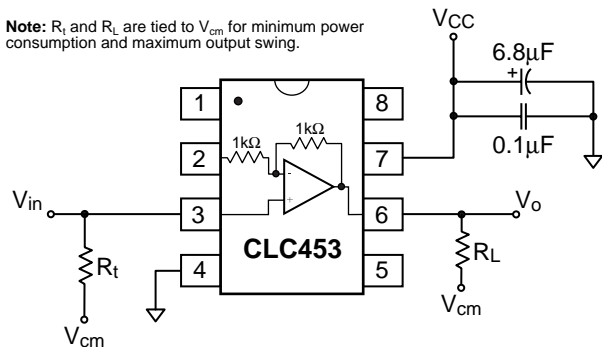


Figure 2: DC Coupled, $A_v = +1V/V$ Configuration

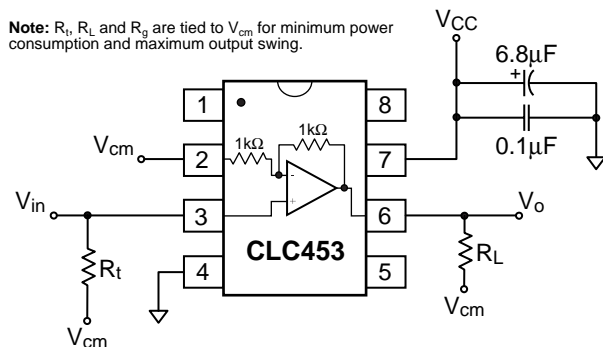


Figure 3: DC Coupled, $A_v = +2V/V$ Configuration

AC Coupled Single Supply Operation

Figures 4, 5, and 6 show possible non-inverting and inverting configurations for input signals that go below 0.8V DC.

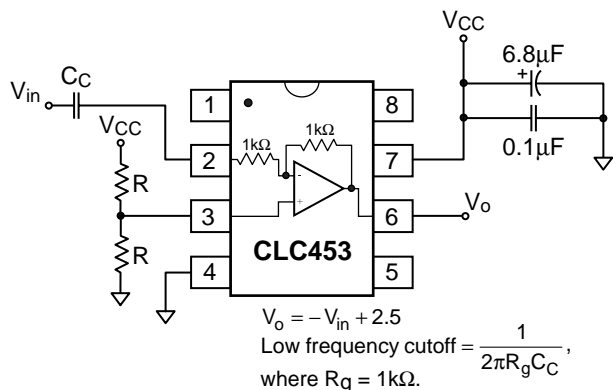


Figure 4: AC Coupled, $A_v = -1V/V$ Configuration

The input is AC coupled to prevent the need for level shifting the input signal at the source. The resistive voltage divider biases the non-inverting input to $V_{CC} \div 2 = 2.5V$ (For $V_{CC} = +5V$).

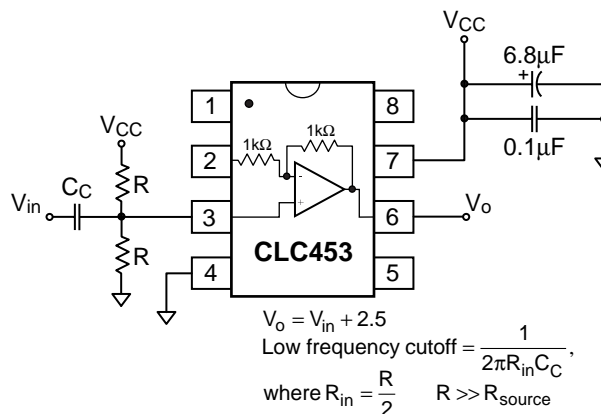


Figure 5: AC Coupled, $A_v = +1V/V$ Configuration

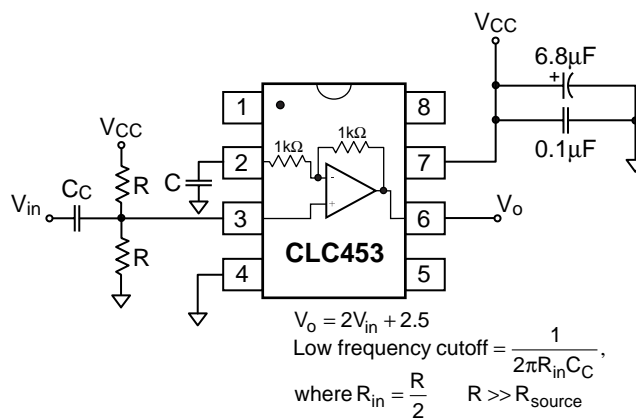


Figure 6: AC Coupled, $A_v = +2V/V$ Configuration

Dual Supply Operation

The CLC453 operates on dual supplies as well as single supplies. The non-inverting and inverting configurations are shown in Figures 7, 8 and 9.

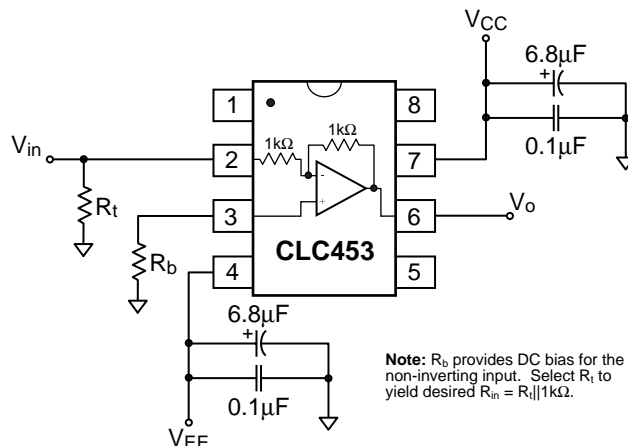


Figure 7: Dual Supply, $A_v = -1V/V$ Configuration

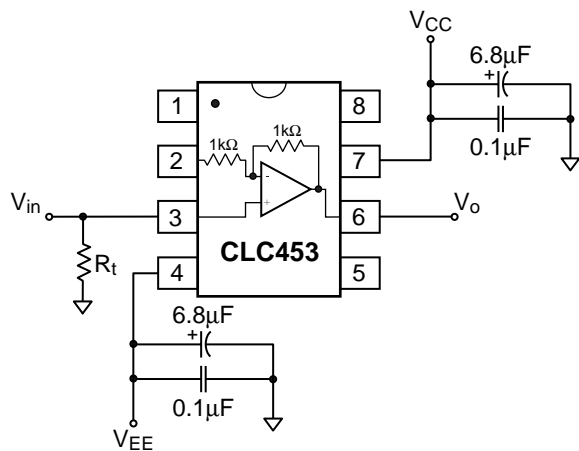


Figure 8: Dual Supply, $A_v = +1V/V$ Configuration

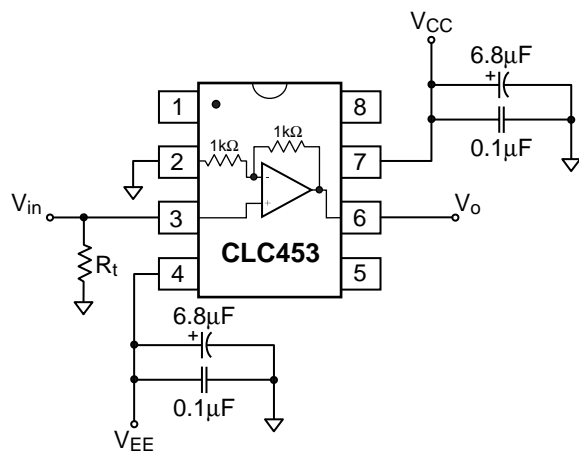


Figure 9: Dual Supply, $A_v = +2V/V$ Configuration

Bandwidth vs. Output Amplitude

The bandwidth of the CLC453 is at a maximum for output voltages near $1V_{pp}$. The bandwidth decreases for smaller and larger output amplitudes. Refer to the **Frequency Response vs. V_o** plots.

Load Termination

The CLC453 can source and sink near equal amounts of current. For optimum performance, the load should be tied to V_{cm} .

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC453 will improve stability and settling performance. The **Frequency Response vs. C_L** and **Recommended R_s vs. C_L** plots, in the typical performance section, give the recommended series resistance value for optimum flatness at various capacitive loads.

Transmission Line Matching

One method for matching the characteristic impedance (Z_0) of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier.

Figure 10 shows typical inverting and non-inverting circuit configurations for matching transmission lines.

Non-inverting gain applications:

- Connect pin 2 as indicated in the table in the **Closed Loop Gain Selection** section.
- Make R_1 , R_2 , R_6 , and R_7 equal to Z_0 .
- Use R_3 to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

Inverting gain applications:

- Connect R_3 directly to ground.
- Make the resistors R_4 , R_6 , and R_7 equal to Z_0 .
- Make $R_5 \parallel R_g = Z_0$.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C_6 to match the output transmission line over a greater frequency range. C_6 compensates for the increase of the amplifier's output impedance with frequency.

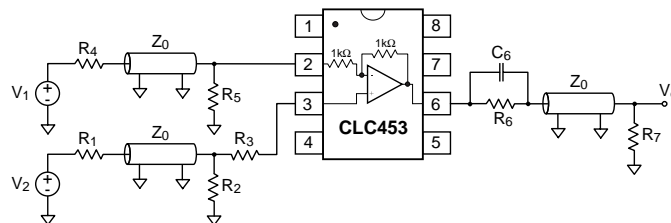


Figure 10: Transmission Line Matching

Power Dissipation

Follow these steps to determine the power consumption of the CLC453:

1. Calculate the quiescent (no-load) power:
 $P_{amp} = I_{CC} (V_{CC} - V_{EE})$
2. Calculate the RMS power at the output stage:
 $P_o = (V_{CC} - V_{load}) (I_{load})$, where V_{load} and I_{load} are the RMS voltage and current across the external load.
3. Calculate the total RMS power:
 $P_t = P_{amp} + P_o$

The maximum power that the DIP, SOIC, and SOT packages can dissipate at a given temperature is illustrated in Figure 11. The power derating curve for any CLC453 package can be derived by utilizing the following equation:

$$\frac{(175^\circ - T_{amb})}{\theta_{JA}}$$

where

T_{amb} = Ambient temperature ($^\circ C$)

θ_{JA} = Thermal resistance, from junction to ambient, for a given package ($^\circ C/W$)

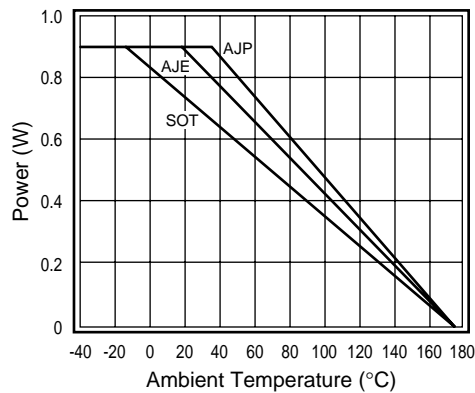


Figure 11: Power Derating Curve

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. Comlinear provides evaluation boards for the CLC453 (CLC730013-DIP, CLC730027-SOIC, CLC730068-SOT) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF tantalum and 0.1μF ceramic capacitors on both supplies.
- Place the 6.8μF capacitors within 0.75 inches of the power pins.
- Place the 0.1μF capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.

Evaluation Board Information

Data sheets are available for the CLC730013/CLC730027 and CLC730068 evaluation boards. The evaluation board data sheets provide:

- Evaluation board schematics
- Evaluation board layouts
- General information about the boards

The CLC730013/CLC730027 data sheet also contains tables of recommended components to evaluate several of National's high speed amplifiers. This table for the CLC453 is illustrated below. Refer to the evaluation board data sheet for schematics and further information.

Components Needed to Evaluate the CLC453 on the Evaluation Board:

- R_{in} , R_{out} - Typically 50Ω (Refer to the **Basic Operation** section of the evaluation board data sheet for details)

- R_t - Optional resistor for inverting gain configurations (Select R_t to yield desired input impedance = $R_g \parallel R_t$)
- C_1 , C_2 - 0.1μF ceramic capacitors
- C_3 , C_4 - 6.8μF tantalum capacitors

Components not used:

- C_5 , C_6 , C_7 , C_8
- R_1 thru R_8

The evaluation boards are designed to accommodate dual supplies. The boards can be modified to provide single supply operation. For best performance; 1) do not connect the unused supply, 2) ground the unused supply pin.

Special Evaluation Board

Considerations for the CLC453

To optimize off-isolation of the CLC453, cut the R_t trace on both the CLC730013 and the CLC730027 evaluation boards. This cut minimizes capacitive feedthrough between the input and the output. Figure 12 shows where to cut both evaluation boards for improved off-isolation.

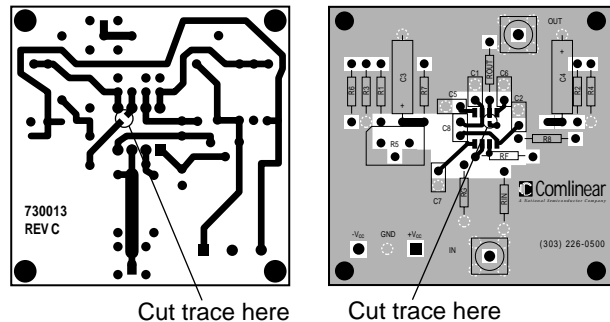


Figure 12: Evaluation Board Changes

SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for National's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The **readme** file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for National's Op Amps, contains schematics and a reproduction of the readme file.

Application Circuits

Single Supply Cable Driver

The typical application shown on the front page shows the CLC453 driving 10m of 75Ω coaxial cable. The CLC453 is set for a gain of +2V/V to compensate for the divide-by-two voltage drop at V_o .

Twisted Pair Driver

The high output current and low distortion, of the CLC453, make it well suited for driving transformers. Figure 13 illustrates a typical twisted pair driver utilizing the CLC453 and a transformer. The transformer provides the signal and its inversion for the twisted pair.

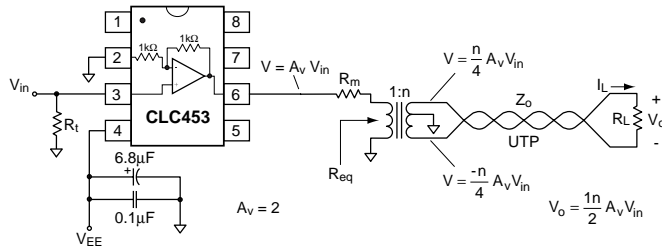


Figure 13: Twisted Pair Driver

To match the line's characteristic impedance (Z_0) set:

- $R_L = Z_0$
- $R_m = R_{eq}$

Where R_{eq} is the transformed value of the load impedance, (R_L), and is approximated by:

$$R_{eq} = \frac{R_L}{n^2}$$

Select the transformer so that it loads the line with a value close to Z_0 , over the desired frequency range. The output impedance, R_o , of the CLC453 varies with frequency and can also affect the return loss. The return loss, shown below, takes into account an ideal transformer and the value of R_o .

$$\text{Return Loss (dB)} \approx -20 \log_{10} \left| n^2 \cdot \frac{R_o}{Z_0} \right|$$

The load current (I_L) and voltage (V_o) are related to the CLC453's maximum output voltage and current by:

$$\begin{aligned} |V_o| &\leq n \cdot V_{\max} \\ |I_L| &\leq \frac{I_{\max}}{n} \end{aligned}$$

From the above current relationship, it is obvious that an amplifier with high output drive capability is required.

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