National Semiconductor

CLC409
Very Wideband, Low Distortion Monolithic Op Amp

General Description

The CLC409 is a very wideband, DC coupled monolithic operational amplifier designed specifically for wide dynamic range systems requiring exceptional signal fidelity. Benefitting from National's current feedback architecture, the CLC409 offers a gain range of ±1 to ±10 while providing stable, oscillation free operation without external compensation, even at unity gain.

With its 350MHz small signal bandwidth (V_{out}=2V_{pp}), 10-bit distortion levels through 20MHz (R_L=100Ω), 8-bit distortion levels through 60MHz, 2.2nV/$\sqrt{Hz}$ input referred noise and 13.5mA supply current, the CLC409 is the ideal driver or buffer for high speed flash A/D and D/A converters.

Wide dynamic range systems such as radar and communication receivers requiring a wideband amplifier offering exceptional signal purity will find the CLC409's low input referred noise and low harmonic and intermodulation distortion make it an attractive high speed solution.

Constructed using an advanced, complimentary biploar process and National's proven current feedback architecture, the CLC409 is available in several versions to meet a variety of requirements.

CLC409AJP	-40°C to +85°C	8-pin plastic DIP
CLC409AJE	-40°C to +85°C	8-pin plastic SOIC
CLC409ALC	-40°C to +85°C	dice
CLC409AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B
CLC409AJM5	-40°C to +85°C	5-pin SOT

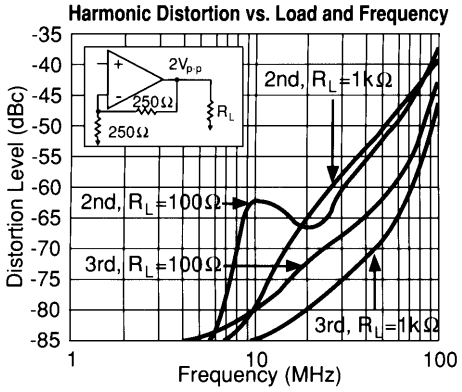
DESC SMD number: 5962-92034

Features

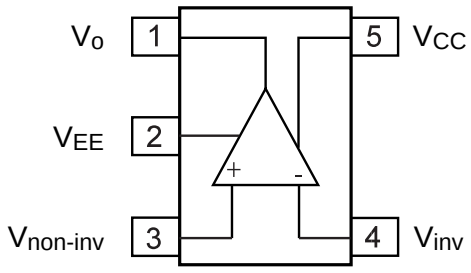
- 350MHz small signal bandwidth
- -65/-72dBc 2nd/3rd harmonics (20MHz)
- Low noise
- 8ns settling to 0.1%
- 1200V/µs slew rate
- 13.5mA supply current (±5V)
- 70mA output current

Applications

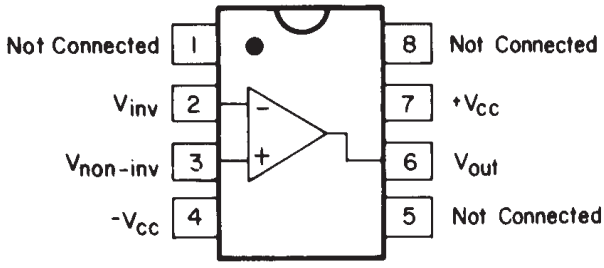
- Flash A/D driver
- D/A transimpedance buffer
- Wide dynamic range IF amp
- Radar/communication receivers
- DDS post-amps
- Wideband inverting summer
- Line driver



Pinout
SOT23-5



Pinout
DIP & SOIC



CLC409 Electrical Characteristics (A_V = +2, V_{cc} = ±5V, R_L = 100Ω, R_f = 250Ω; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC409AJ	+25°C	−40°C	+25°C	+ 85°C		
FREQUENCY DOMAIN PERFORMANCE							
−3dB bandwidth	V_{out}<2V_{pp}	350	>250	>250	>200	MHz	SSBW
	V_{out}<5V_{pp}	110	>90	>90	>80	MHz	LSBW
gain flatness	V_{out}<0.5V_{pp}						
peaking	DC to 75MHz	0	<0.4	<0.4	<0.4	dB	GFPL
peaking	>75MHz	0	<0.8	<0.8	<0.8	dB	GFPH
rolloff	DC to 125MHz	0.2	<1.0	<1.0	<1.0	dB	GFR1
rolloff	@ 200MHz	1.0	<2.0	<2.2	<3.0	dB	GFR2
linear phase deviation	DC to 100MHz	0.3	<0.8	<0.8	<1.0	°	LPD
differential gain	150Ω load, 3.58MHz	0.03	<0.07	<0.06	<0.06	%	DG1
	4.43MHz	0.03	<0.07	<0.06	<0.06	%	DG2
differential phase	150Ω load, 3.58MHz	0.01	<0.02	<0.02	<0.02	°	DP1
	4.43MHz	0.01	<0.02	<0.02	<0.02	°	DP2
TIME DOMAIN RESPONSE							
rise and fall time	2V step	1.3	<1.6	<1.6	<1.6	ns	TRS
	5V step	3.5	<4.2	<4.2	<4.6	ns	TRL
settling time to 0.1%	2Vstep	8	<12	<12	<12	ns	TS
overshoot	2V step	5	<15	<18	<18	%	OS
slew rate		1200	>1000	>1000	>1000	V/μs	SR
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 5MHz	−86	<−78	<−81	<−81	dBc	HD2L
	2V_{pp}, 20MHz	−65	<−56	<−56	<−56	dBc	HD2
	2V_{pp}, 60MHz	−49	<−41	<−44	<−44	dBc	HD2H
3rd harmonic distortion	2V_{pp}, 5MHz	−84	<−76	<−76	<−76	dBc	HD3L
	2V_{pp}, 20MHz	−72	<−65	<−65	<−65	dBc	HD3
	2V_{pp}, 60MHz	−59	<−52	<−52	<−52	dBc	HD3H
equivalent input noise							
non-inverting voltage	>1MHZ	2.2	<2.8	<2.8	<3.1	nV/√Hz	VN
inverting current	>1MHZ	14.3	<18	<18	<20	pA/√Hz	ICN
non-inverting current	>1MHZ	3.2	<4.0	<4.0	<4.5	pA/√Hz	NCN
total noise floor	>1MHZ	−157	<−155	<−155	<−154	dBm_{1Hz}	SNF
total integrated noise	1MHZ to 150MHz	38	<47	<47	<52	μV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		0.5	<8.5	<4.5	<9.5	mV	VIO
average temperature coefficient		25	<50	—	<50	μV/°C	DVIO
*input bias current	non-inverting	10	<44	<22	<22	μA	IBN
average temperature coefficient		100	<275	—	<125	nA/°C	DIBN
*input bias current	inverting	10	<36	<20	<30	μA	IBI
average temperature coefficient		100	<200	—	<100	nA/°C	DIBI
power supply rejection ratio		50	>45	>45	>45	dB	PSRR
common mode rejection ratio		50	>45	>45	>45	dB	CMRR
*supply current	no load	13.5	<14.2	<14.2	<14.2	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		1000	>250	>500	>1000	kΩ	RIN
non-inverting input capacitance		1	<2	<2	<2	pF	CIN
output impedance	DC	0.1	<0.3	<0.2	<0.2	Ω	RO
output voltage range	R_L = 100Ω	±3.5	>±3.0	>±3.2	>±3.2	V	VO
common mode input range		±2.2	±1.5	±2.0	±2.0	V	CMIR
output current		70	36	50	50	mA	IO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{cc} ±7V

I_{out} output is short circuit protected to ground, but, maximum reliability will be maintained if I_{out} does not exceed... 70mA

common mode input voltage $\pm V_{cc}$

differential input voltage 10V

junction temperature +175°C

operating temperature range

AJ: −40°C to +85°C

storage temperature range −65°C to +150°C

lead solder duration (+300°C) 10 sec

EDS rating (human body model) 1000V

Miscellaneous Ratings

recommended gain range: ±1 to ±10

Notes: * AJ 100% tested at +25°C.

Package Thermal Resistance

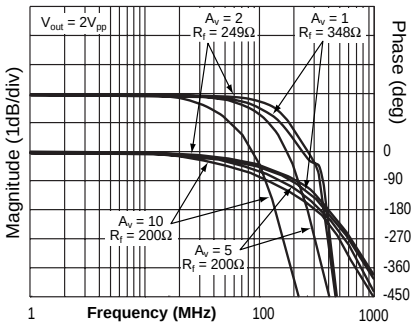
Package	θ_{JC}	θ_{JA}
AJP	95°C/W	155°C/W
AJE	75°C/W	160°C/W
AJM5	115°C/W	185°C/W

Reliability Information

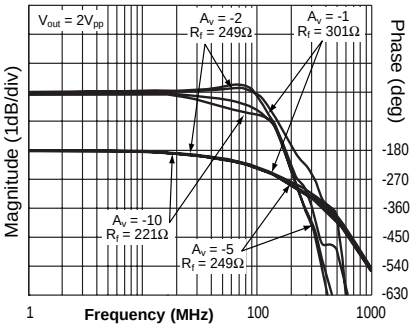
Transistor count 28

CLC409 Typical Performance Characteristics (T_A = 25°, A_V = +6, V_{CC} = ±5V, R_L = 100Ω, R_f = 500Ω)

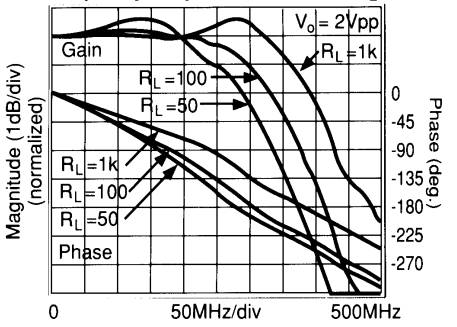
Non-Inverting Frequency Response



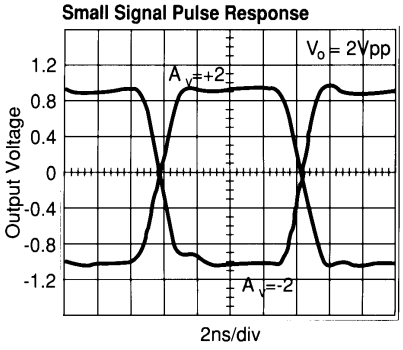
Inverting Frequency Response



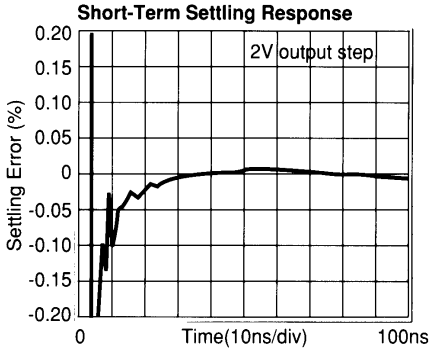
Frequency Response for Various R_Ls



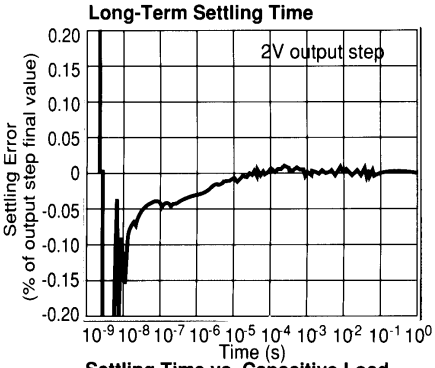
Small Signal Pulse Response



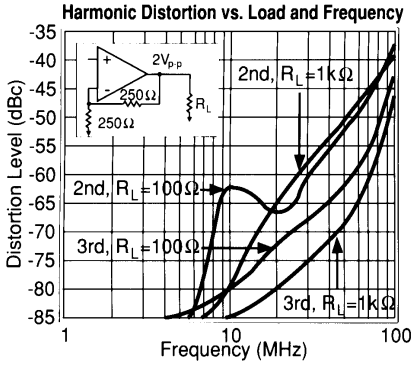
Short-Term Settling Response



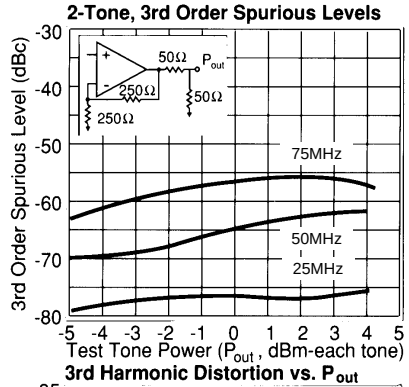
Long-Term Settling Time



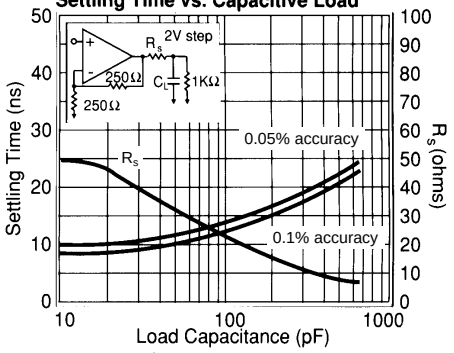
Harmonic Distortion vs. Load and Frequency



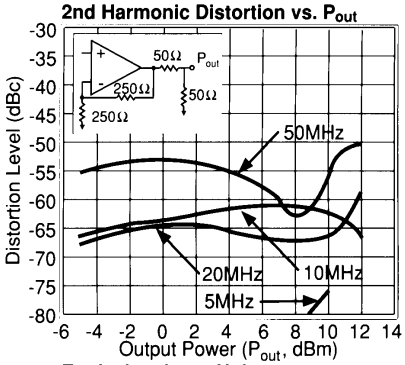
2-Tone, 3rd Order Spurious Levels



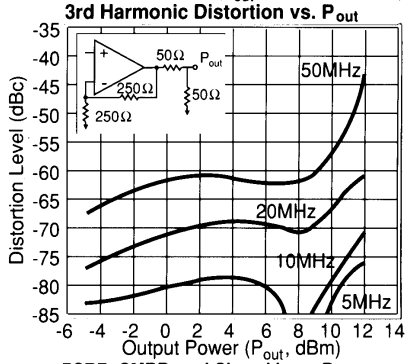
Settling Time vs. Capacitive Load



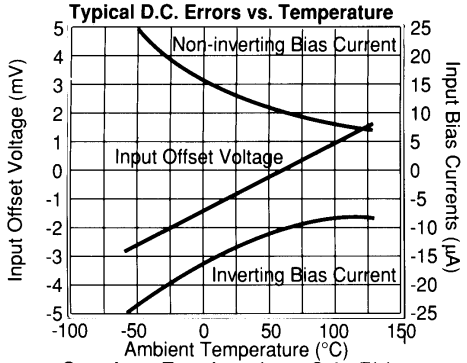
2nd Harmonic Distortion vs. P_{out}



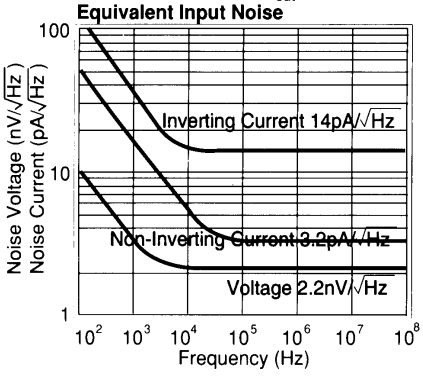
3rd Harmonic Distortion vs. P_{out}



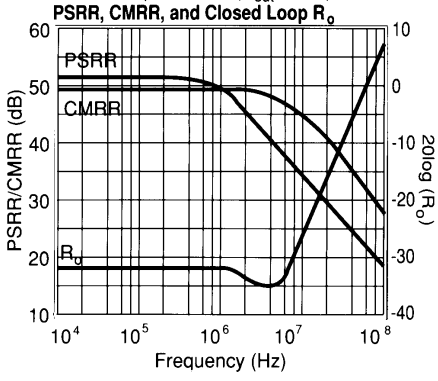
Typical D.C. Errors vs. Temperature



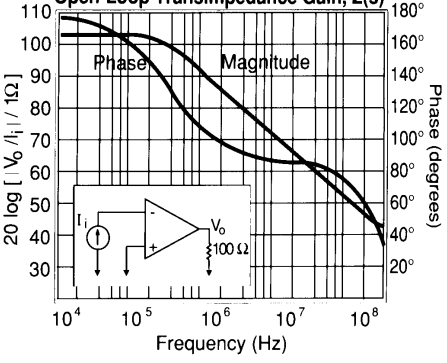
Equivalent Input Noise



PSRR, CMRR, and Closed Loop R_o



Open-Loop Transimpedance Gain, Z(s)



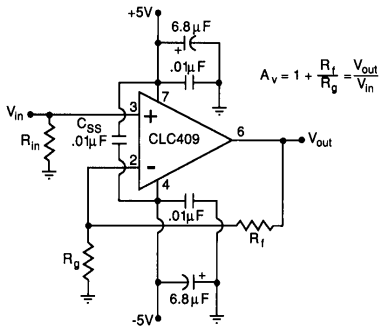
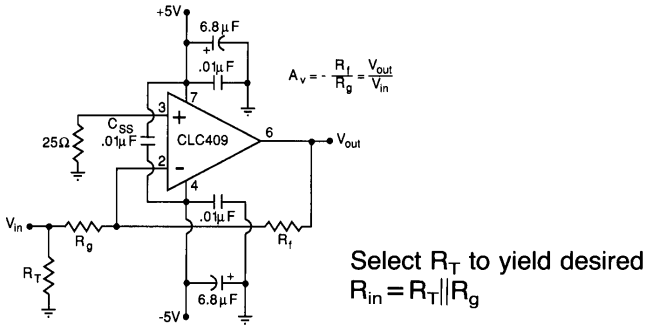


Figure 1: recommended non-inverting gain circuit



Select R_T to yield desired $R_{in} = R_T || R_g$

Figure 2: recommended inverting gain circuit

Feedback Resistor

The CLC409 achieves its excellent pulse and distortion performance by using the current feedback topology pioneered by Comlinear Corporation. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The CLC409 is optimized for use with a 250Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 discusses this in detail along with the occasions where a different R_f might be advantageous.

Harmonic Distortion

The CLC409 has been optimized for exceptionally low harmonic distortion while driving very demanding resistive or capacitive loads. Generally, when used as the input amplifier to very high speed flash ADCs, the distortions introduced by the converter will dominate over the low CLC409 distortions shown on the plots on the previous page. The 0.01µF capacitor (C_{SS}) shown across the supplies in Figures 1 and 2 is critical to achieving the lowest 2nd harmonic distortion.

The 2-tone, 3rd-order spurious plot shows a relatively constant difference between the test power level and the spurious level with that difference depending on frequency. The CLC409 does not show an intercept type performance, (where the relative spurious levels change at a 2X rate vs. the test tone powers), due to an internal full power bandwidth enhancement circuit that boosts the performance as the output swing increases while dissipating negligible quiescent power under low output power conditions. This feature enhances the distortion performance and full power bandwidth to match that of much higher quiescent supply current parts.

Figure 3 shows a typical application using the CLC409 to drive an ADC. The series resistor, R_s, between the amplifier output and the ADC input is critical to achieving best system performance. This load capacitance, if applied directly to the output pin, can quickly lead to unacceptable levels of ringing in the pulse response. The plot of R_s and settling time vs. C_L on the previous page is an excellent starting point for setting R_s. The value derived in that plot minimizes the step settling time into a fixed discrete capacitive load. Several additional constraints should be considered, however, in driving the capacitive input of an ADC.

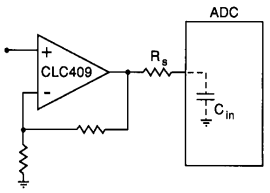


Figure 3: input amplifier to ADC

There is an option to increase R_s, bandlimiting at the ADC input for either noise or Nyquist bandlimiting purposes. Increasing R_s too much, however, can induce an unacceptably large input glitch due to switching transients coupling through from the convert signal. Also, C_{in} is oftentimes a voltage dependent capacitance. This input impedance non-linearity will induce distortion terms that will increase as R_s is increased. Only slight adjustments up or down from the recommended R_s value should therefore be attempted in optimizing system performance.

DC Accuracy and Noise

The CLC409 offers an improved offset voltage over the pin compatible CLC400 low gain amplifier. The offset adjustment available on the CLC400 was therefore not included in this part. Figure 4 shows the output offset computation equation for the non-inverting configuration with an example using the typical bias current and offset specifications for $A_v = +2$.

Output Offset

$$V_o = (\pm I_{bn} R_{in} \pm V_{io})\ (1 + R_f/R_g) \pm I_{bi} R_f$$

Example Computation for $A_v = +2$, $R_f = 250\Omega$, $R_{in} = 25\Omega$:

$V_o = (\pm 10\mu A(25\Omega) \pm 0.5mV)2 \pm 10\mu A(250\Omega) = \pm 3.25mV$

Figure 4: Output DC Offset Calculation

This low output offset voltage is a marked improvement over earlier very high speed amplifiers. Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA-7.

The two input bias currents are physically unrelated in both magnitude and polarity for the current feedback topology. It is not possible, therefore, to cancel their effects by matching the source impedance for the two inputs (as is commonly done for matched input bias current devices).

The total output noise is computed in a similar fashion to output offset voltage. Using the input noise voltage and two input noise currents, the output noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. See Application Note OA-12 for a full discussion of noise calculations for current feedback amplifiers.

Printed Circuit Layout

As with any high speed component, a careful attention to the board layout is necessary for optimum performance. Evaluation PC boards (CLC730013-DIP, CLC730027-SOIC, and CLC730068-SOT) for the CLC409 are available. This additional supply bypassing capacitor, C_{SS}, can easily be added to the board if desired. Further layout suggestions can be found in Application Note OA-15.

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