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National Semiconductor

CLC111
Ultra-High Slew Rate, Closed-Loop Buffer

General Description

The CLC111 is a high-performance, closed-loop, monolithic buffer designed for applications requiring very high-frequency signals. The CLC111's high performance includes an extremely fast 800MHz small signal bandwidth (0.5V_{pp}) and an ultra high (3500V/µs) slew rate while requiring only 10.5mA quiescent current. Signal fidelity is maintained with low harmonic distortion (-62dBc 2nd and 3rd harmonics at 20MHz). These performance characteristics are for a demanding 100Ω load.

Featuring a patented closed-loop design, the CLC111 offers nearly ideal unity-gain (0.996) with very low (1.4Ω) output impedance. The CLC111 is ideally suited for buffering video signals with its 0.15%/0.04° differential gain and phase performance at 4.43MHz. Power sensitive applications will benefit from the CLC111's excellent performance on reduced or single supply voltages.

Constructed using an advanced, complementary bipolar process and Comlinear's proven high-performance architectures, the CLC111 is available in several versions to meet a variety of requirements.

CLC111AJP	-40°C to +85°C	8-pin Plastic DIP
CLC111AJE	-40°C to +85°C	8-pin Plastic SOIC
CLC111ALC	-40°C to +85°C	dice
CLC111AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B

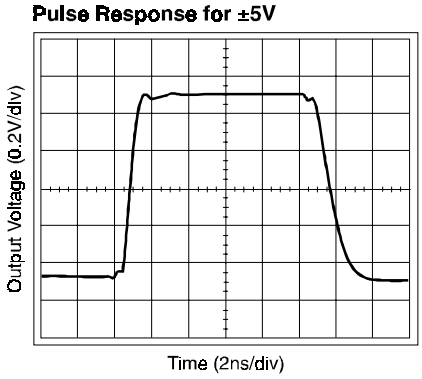
Contact factory for other packages and DESC SMD number.

Features

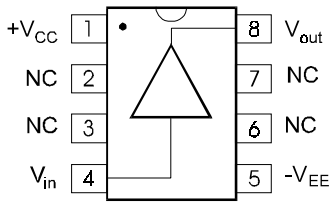
- Very wideband (800MHz)
- Ultra-high (3500V/µs) slew rate
- Very low output impedance (1.4Ω)
- Low (-62dBc) 2nd/3rd harmonics @ 20MHz
- 60mA output current (±5 supplies)
- Single supply operation (0 to 3V supply min.)
- Evaluation boards and Spice models

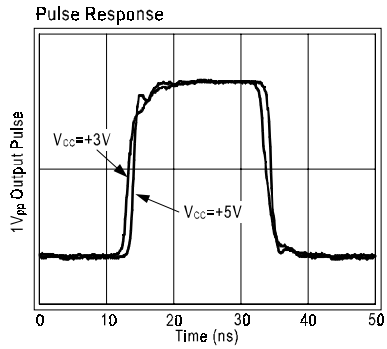
Applications

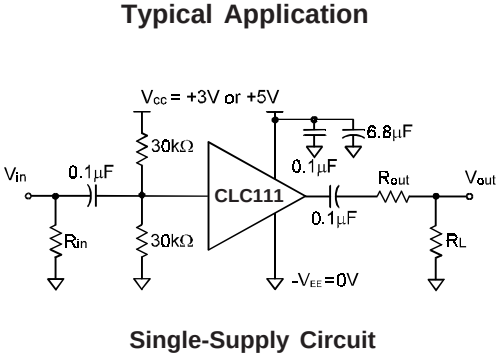
- Video switch buffers
- Test point drivers
- High frequency active filters
- Wideband DC clamping buffer
- High-speed peak detector circuits

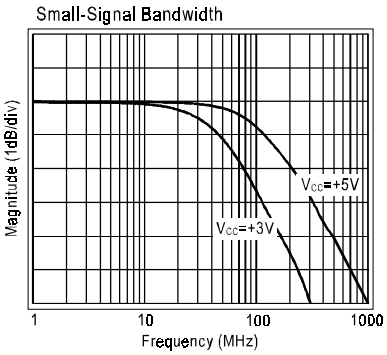


Pinout
DIP & SOIC









CLC111 Electrical Characteristics ($\pm V_{cc}$ = ± 5V, R_L = 100Ω unless specified)

PARAMETER	CONDITIONS	TYP	MIN AND MAX RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC109AJ	+25°C	-40°C	+25°C	+85°C		
FREQUENCY RESPONSE							
small signal bandwidth	V_{out} < 0.5V_{pp}	800	400	400	300	MHz	SSBW
	V_{out} < 4.0V_{pp}	450	250	250	200	MHz	LSBW
gain flatness	V_{out} < 0.5V_{pp}						
flatness	DC-50MHz	0.02	±0.1	±0.1	±0.2	dB	GFL
peaking	DC-200MHz	0.1	1.0	0.5	0.5	dB	GFPH
rolloff	DC-200MHz	0.1	0.8	0.8	1.2	dB	GFRH
differential gain	4.43MHz, 150Ω load	0.15	0.4	0.25	0.25	%	DG
differential phase	4.43MHz, 150Ω load	0.04	0.08	0.08	0.08	°	DP
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	0.6	0.8	0.8	1.1	ns	TRS
	4.0V step	1.0	1.4	1.4	1.7	ns	TRL
settling time to ±0.1%	2.0V step	16	20	20	20	ns	TS
overshoot	4V step	0	8	5	5	%	OS1
slew rate	4V step	3500	2700	2700	2300	V/µsec	SR
DISTORTION AND NOISE PERFORMANCE							
2nd harmonic distortion	2V_{pp}, 20MHz	-62	-47	-50	-50	dBc	HD2
3rd harmonic distortion	2V_{pp}, 20MHz	-62	-55	-55	-52	dBc	HD3
equivalent output noise							
voltage	>1MHz	4.0	4.8	4.8	5.3	nV/√Hz	VN
current	>1MHz	1.6	4.0	3.0	3.0	pA/√Hz	ICN
STATIC DC PERFORMANCE							
small signal gain	no load	0.996	0.994	0.994	0.992	V/V	GA1
	100Ω load	0.98	0.96	0.97	0.97	V/V	GA2
output resistance	DC	1.4	3.0	2.0	2.0	Ω	RO
*output offset voltage		2	17	9	9	mV	VIO
average temperature coefficient		±30	±100		±50	µV/°C	DVIO
*input bias current		5	30	15	15	µA	IBN
average temperature coefficient		50	±187		±100	nA/°C	DIBN
power supply rejection ratio		-52	-48	-48	-46	dB	PSRR
*supply current	no load	10.5	12	12	12	mA	ICC
MISCELLANEOUS PERFORMANCE							
integral endpoint linearity	±2V, full scale	0.2	1.0	0.5	0.5	%	ILIN
input resistance		1	0.3	0.7	1	MΩ	RIN
input capacitance	CERDIP	2.5	3.5	3.5	3.5	pF	CIN
	Plastic DIP	1.25	2.0	2.0	2.0	pF	CIN
output voltage range	no load	3.9	3.5	3.6	3.6	V	VO
	R_L=100Ω	3.5	+3.1,-2.5	3.2	3.2	V	VOL
	R_L=100Ω, 0°C		±3.1			V	VOL
output current		60	50,25	50	40	mA	IO
	0° - 70°C		50,35	50	50	mA	IO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{cc}	±7.0V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	96mA
input voltage	±V_{cc}
maximum junction temperature	+175°C
operating temperature range	
AJ	-40°C to +85°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C
ESD rating	1000V

Miscellaneous Ratings

Notes:

* AJ : 100% tested at +25°C.

Package Thermal Resistance

Package	θ_{JC}	θ_{JA}
Plastic(AJP)	70°C/W	125°C/W
Surface Mount (AJE)	65°C/W	145°C/W

Reliability Information

Transistor count	17

Electrical Characteristics (V_{CC} = +3V or V_{CC} = +5V, $-V_{EE}$ = 0V, T_A = +25°C, R_L = 100Ω, unless noted)

PARAMETERS	CONDITIONS	V_{CC} = 3V	V_{CC} = 5V	UNITS
FREQUENCY DOMAIN RESPONSE				
-3dB bandwidth	$V_{out} < 0.5V_{pp}$	120	300	MHz
	$V_{out} < 2.0V_{pp}$		210	MHz
gain flatness	$V_{out} < 0.5V_{pp}$			
flatness	DC to 30MHz	0.5	0.1	dB
peaking	DC to 200MHz	0	0	dB
rolloff	DC to 60MHz	1.5	0.25	dB
TIME DOMAIN RESPONSE				
rise and fall time	0.5V step	3.9	1.2	ns
	2.0V step		1.5	ns
overshoot	1.0V step	3	3	%
slew rate	0.5V step	260	425	V/µs
DISTORTION AND NOISE RESPONSE				
2nd harmonic distortion	$0.5V_{pp}$,20MHz	-46		dBc
	$1.0V_{pp}$,20MHz		-55	dBc
3rd harmonic distortion	$0.5V_{pp}$,20MHz	-44		dBc
	$1.0V_{pp}$,20MHz		-64	dBc
STATIC DC PERFORMANCE				
small-signal gain	AC-coupled	0.96	0.97	V/V
supply current	$R_L = \infty$	2.0	4.5	mA
MISCELLANEOUS PERFORMANCE				
output voltage range	$R_L = \infty$	1.5	3.4	V_{pp}
	R_L=100Ω	1.1	2.6	V_{pp}

Operation

The CLC111 is a low-power, very high-speed unity-gain buffer. It uses a closed-loop topology which allows for accuracy not usually found in high-speed open-loop buffers. A slew enhanced front end allows for low quiescent power while not sacrificing ac performance.

Single Supply Operation

Although the CLC111 is specified to operate from split ±5V power supplies, there is no internal ground reference that prevents operation from a single voltage power supply. For single supply operation the input signal should be biased at a DC value of ½V_{CC}. This can be accomplished by AC coupling and rebiasing as shown in Figure 1.

The above electrical specifications provide typical performance specifications for the CLC111 at 25°C while operating from a single +3V or a single +5V power supply.

Printed Circuit Layout and Supply Bypassing

As with any high-frequency device, a good PCB layout is required for optimum performance. This is especially important for a device as fast as the CLC111.

To minimize capacitive feedthrough, pins 2, 3, 6, and 7 should be connected to the ground plane, as shown in Figure 1. Input and output traces should be laid out as transmission lines with the appropriate termination resistors very near the CLC111. On a 0.065 inch epoxy PCB material, a 50Ω transmission line (commonly called stripline) can be constructed by using a trace width of 0.1" over a complete ground plane.

Figure 1 shows recommended power supply bypassing.

The ferrite beads are optional and are recommended only where additional isolation is needed from high-frequency (>400MHz) resonances in the power supply.

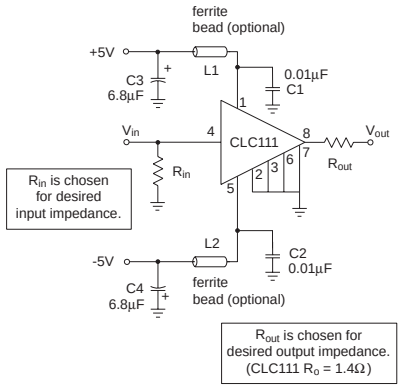


Figure 1: Recommended circuit & evaluation board schematic

Parasitic or load capacitance directly on the output of the CLC111 will introduce additional phase shift in the device. This phase shift can decrease phase margin and increase frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the following page illustrate the required resistor value and the resulting performance vs. capacitance.

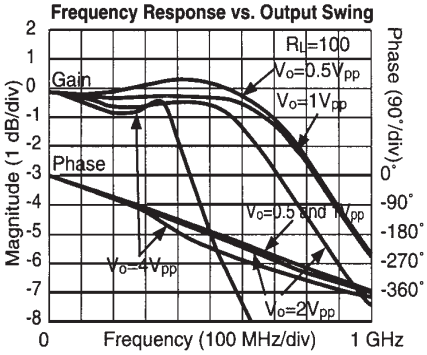
Precision buffed resistors (PRP8351 series from Precision Resistive Products), which have low parasitic reactances, were used to develop the data sheet specifications. Precision carbon composition resistors or standard spirally-trimmed RN55D metal film resistors will work, though they will cause a slight degradation of ac performance due to their reactive nature at high frequencies.

Evaluation Boards

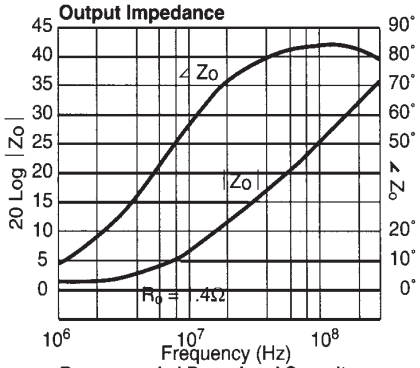
Evaluation boards are available from National as part numbers CLC730012 (DIP) and CLC730045 (SOIC). This board was used in the characterization of the device and provides optimal performance. Designers are encouraged to copy these printed circuit board layouts for their applications.

Typical Performance Characteristics (T_A = +25°C, V_{cc} = ± 5V, R_L = 100Ω unless specified)

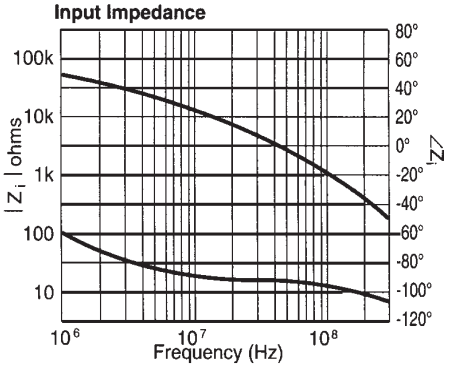
Frequency Response vs. Output Swing



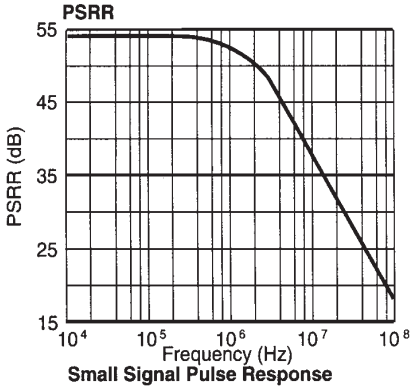
Output Impedance



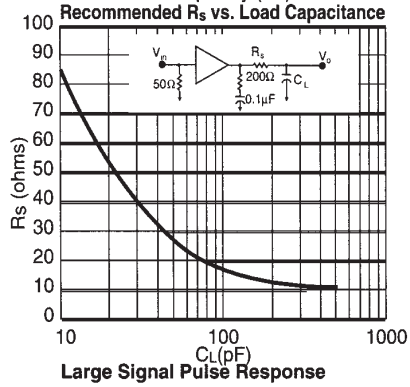
Input Impedance



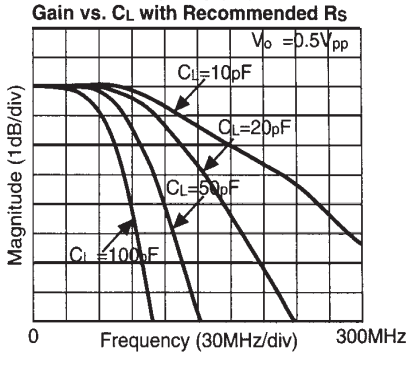
PSRR



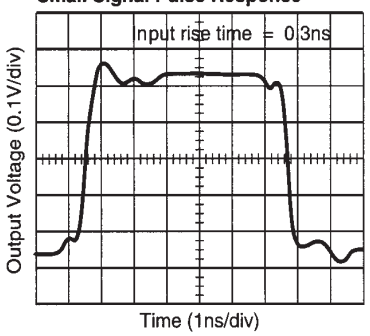
Recommended R_S vs. Load Capacitance



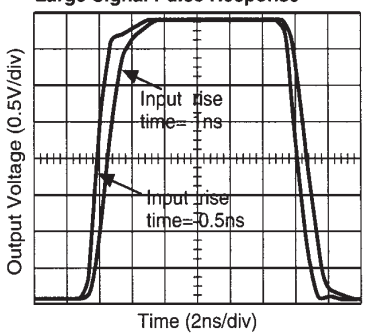
Gain vs. C_L with Recommended R_S



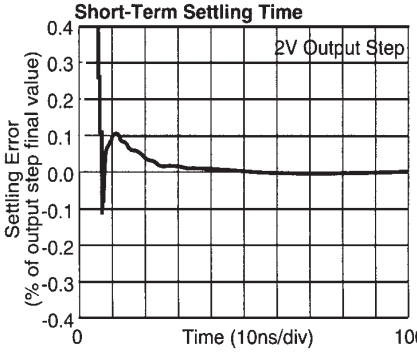
Small Signal Pulse Response



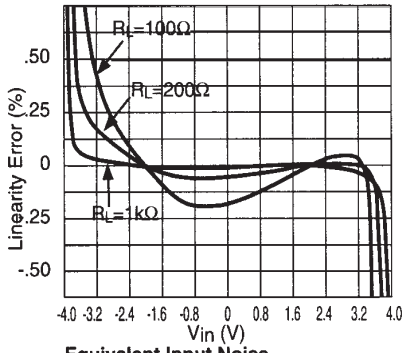
Large Signal Pulse Response



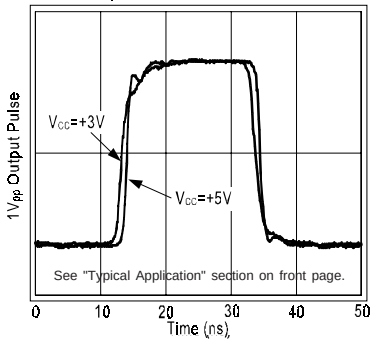
Short-Term Settling Time



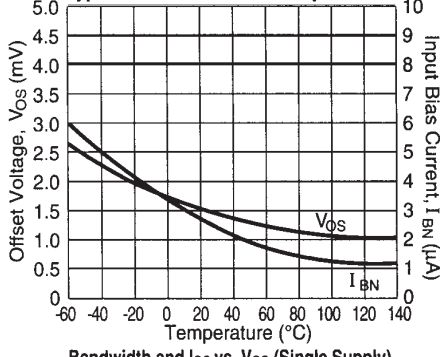
Integral Linearity Error



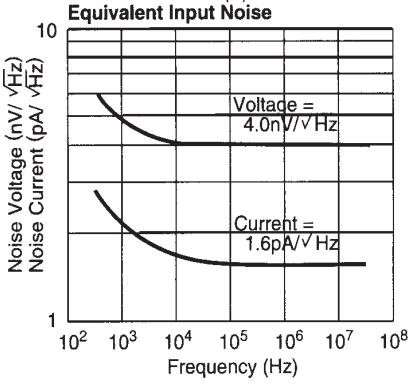
Pulse Response



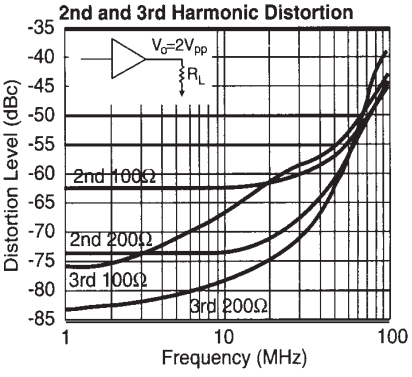
Typical D.C. Errors vs. Temperature



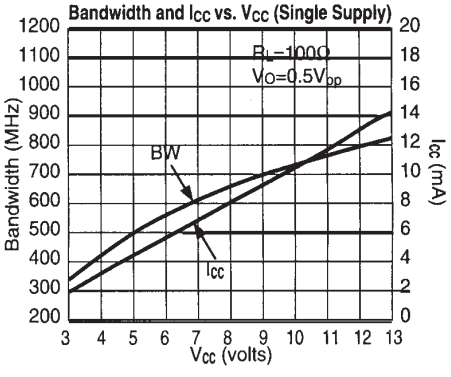
Equivalent Input Noise



2nd and 3rd Harmonic Distortion



Bandwidth and I_{CC} vs. V_{CC} (Single Supply)



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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