

54F/74F545 Octal Bidirectional Transceiver with TRI-STATE® Outputs

General Description

The 'F545 is an 8-bit, TRI-STATE, high-speed transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24 mA (20 mA Mil) bus drive capability on the A ports and 64 mA (48 mA Mil) bus drive capability on the B ports.

One input, Transmit/Receive (T/ $\bar{R}$) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Output Enable input disables both A and B ports by placing them in a TRI-STATE condition.

Features

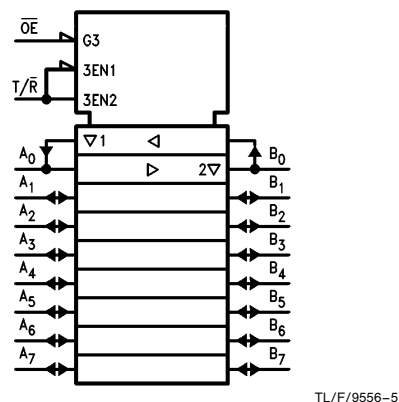
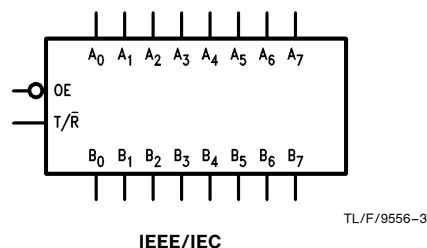
- Higher drive than 8304
- 8-bit bidirectional data flow reduces system package count
- TRI-STATE inputs/outputs for interfacing with bus-oriented systems
- 24 mA (20 mA Mil) and 64 mA (48 mA Mil) bus drive capability on A and B ports, respectively
- Transmit/Receive and Output Enable simplify control logic
- Guaranteed 4000V minimum ESD protection
- Pin for Pin compatible with Intel 8286

Commercial	Military	Package Number	Package Description
74F545PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F545DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F545SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F545SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F545FM (Note 2)	W20A	20-Lead Cerpack
	54F545LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

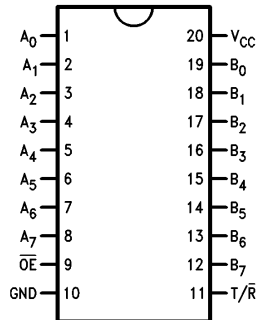
Logic Symbols



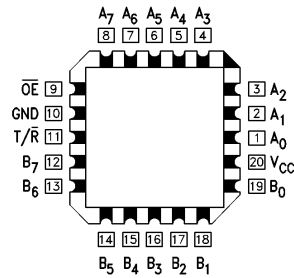
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Connection Diagrams

Pin Assignment for
DIP, SOIC and Flatpak



Pin Assignment
for LCC



TL/F/9556-2

TL/F/9556-1

Truth Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/2.0	20 μA / - 1.2 mA
$T/\overline{R}$	Transmit/Receive Input	1.0/2.0	20 μA / - 1.2 mA
A_0-A_7	Side A TRI-STATE Inputs or TRI-STATE Outputs	3.5/1.083 150/40 (33.3)	70 μA / - 650 μA - 3 mA/24 mA (20 mA)
B_0-B_7	Side B TRI-STATE Inputs or TRI-STATE Outputs	3.5/1.083 600/106.6 (80)	70 μA / - 650 μA - 12 mA/64 mA (48 mA)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA ($\overline{OE}$, T/ $\overline{R}$)
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.0 2.5 2.4 2.0 2.7 2.7		V	Min	I _{OH} = −1 mA (A _n) I _{OH} = −3 mA (A _n) I _{OH} = −12 mA (B _n) I _{OH} = −1 mA (A _n) I _{OH} = −3 mA (A _n) I _{OH} = −15 mA (B _n) I _{OH} = −1 mA (A _n) I _{OH} = −3 mA (A _n)
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC}		0.5 0.55 0.5 0.55	V	Min	I _{OL} = 20 mA (A _n) I _{OL} = 48 mA (B _n) I _{OL} = 24 mA (A _n) I _{OL} = 64 mA (B _n)
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V ($\overline{OE}$, T/ $\overline{R}$)
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V ($\overline{OE}$, T/ $\overline{R}$)
I _{BVIT}	Input HIGH Current Breakdown (I/O)	54F 74F		1.0 0.5	mA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{ID} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−1.2	mA	Max	V _{IN} = 0.5V ($\overline{OE}$, T/ $\overline{R}$)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (A _n , B _n)
I _{IL} + I _{OZL}	Output Leakage Current			−650	μA	Max	V _{OUT} = 0.5V (A _n , B _n)
I _{OS}	Output Short-Circuit Current			−60 −100	mA	Max	V _{OUT} = 0V (A _n) V _{OUT} = 0V (B _n)

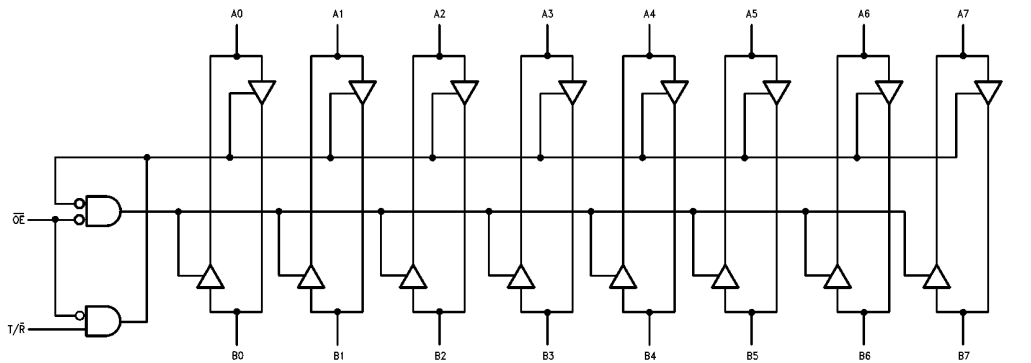
DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCH}	Power Supply Current		70	90	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		95	120	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		85	110	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	2.5	4.2	6.0	2.0	7.5	2.5	7.0	ns
t _{PHL}	A _n to B _n or B _n to A _n	2.5	4.6	6.0	2.0	7.5	2.5	7.0	
t _{PZH}	Output Enable Time	3.0	5.3	7.0	2.5	9.0	3.0	8.0	ns
t _{PZL}		3.5	6.0	8.0	3.0	10.0	3.5	9.0	
t _{PHZ}	Output Disable Time	3.0	5.0	6.5	2.5	9.0	3.0	7.5	
t _{PLZ}		2.0	5.0	6.5	2.0	10.0	2.0	7.5	

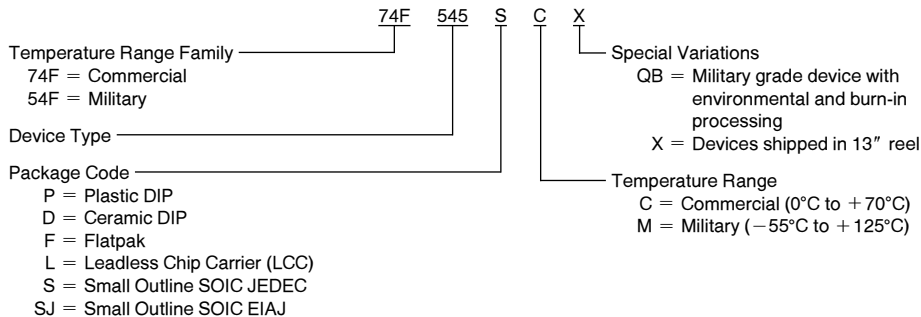
Logic Diagram



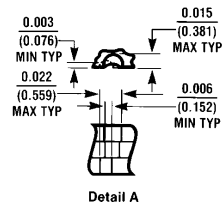
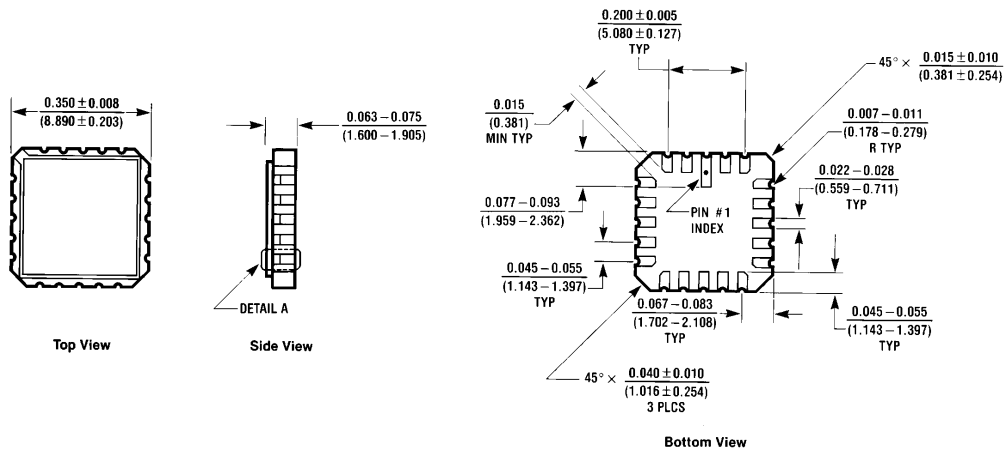
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

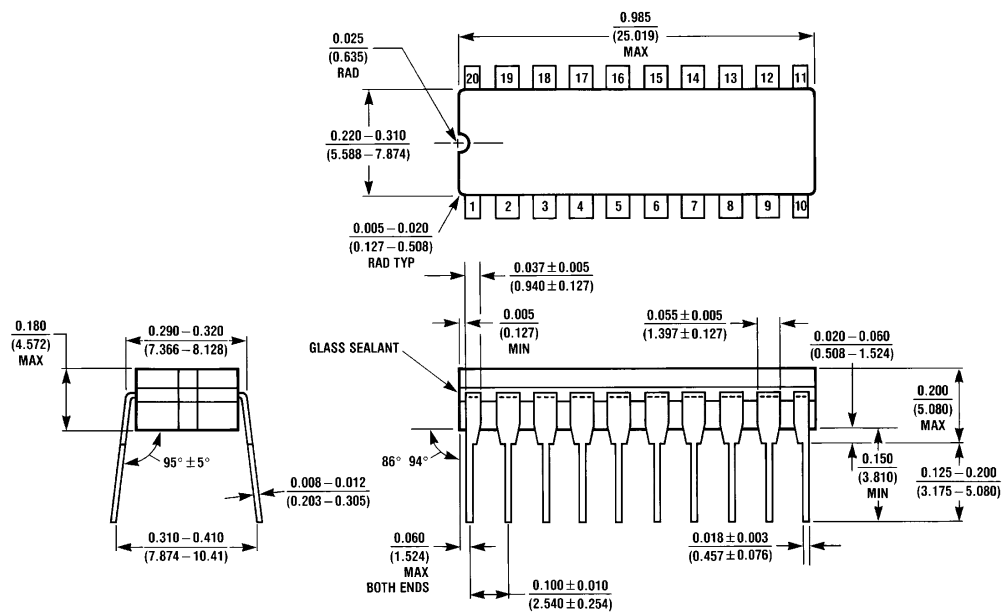


Physical Dimensions inches (millimeters)



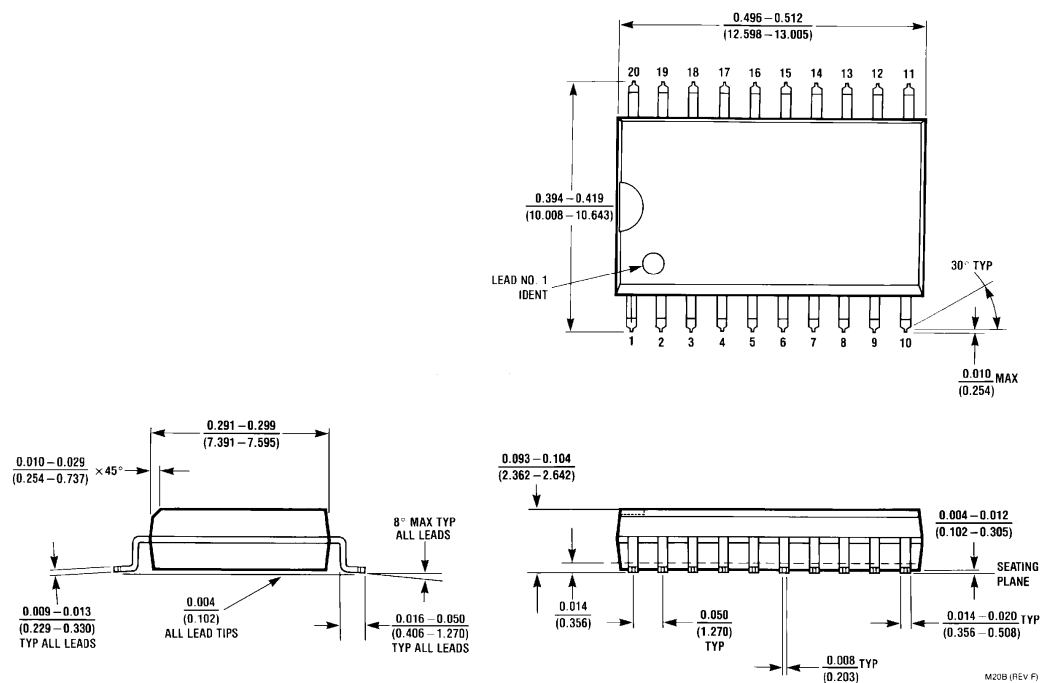
20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

E20A (REV D)

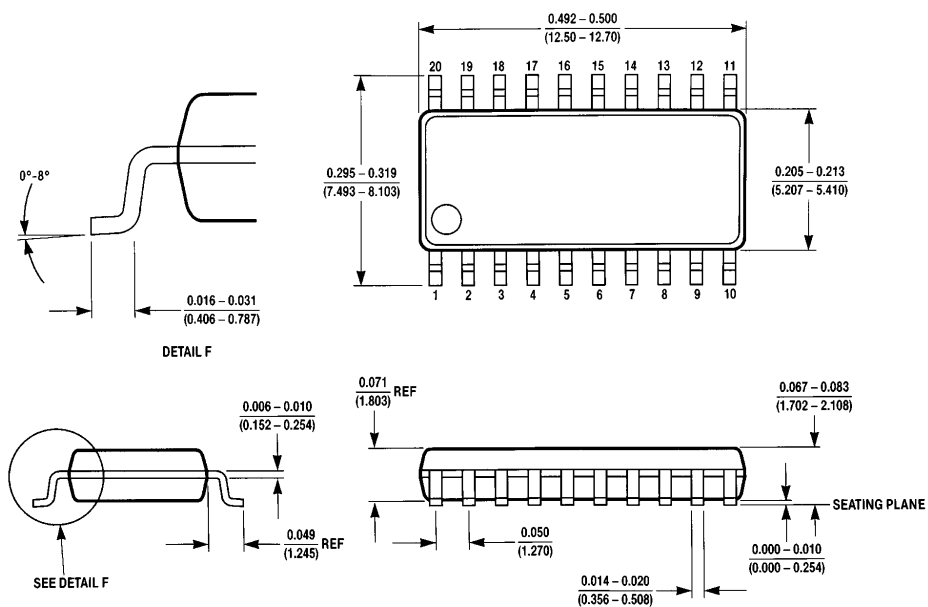


20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

J20A (REV M)

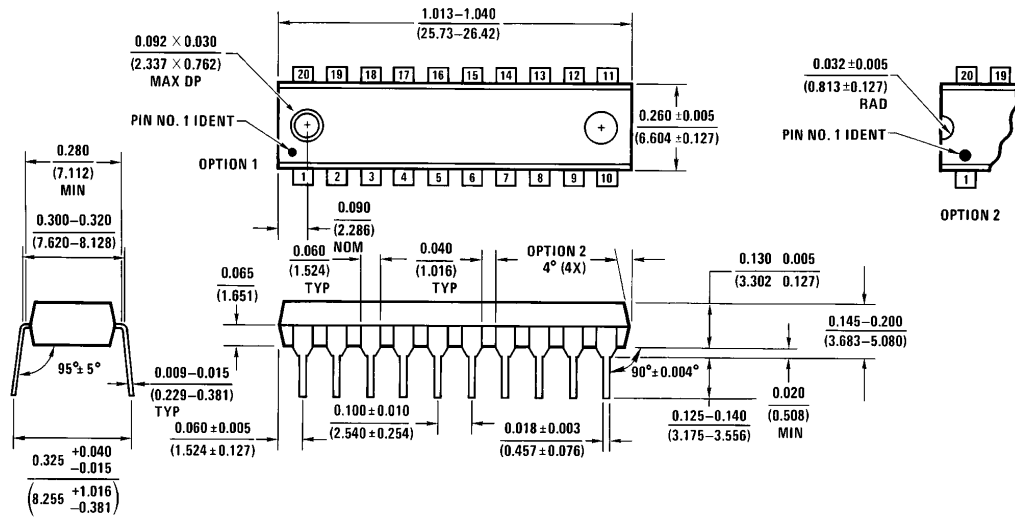
Physical Dimensions inches (millimeters) (Continued)

**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B**



**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ
NS Package Number M20D**

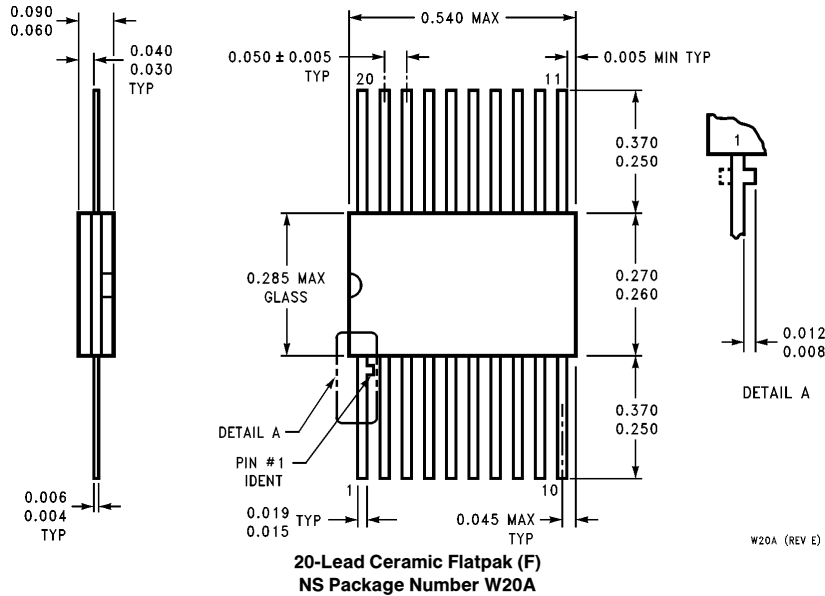
Physical Dimensions inches (millimeters) (Continued)



20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A

N20A (REV G)

Physical Dimensions inches (millimeters) (Continued)



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