

## 54F/74F413 64 x 4 First-In First-Out Buffer Memory with Parallel I/O

### General Description

The 'F413 is an expandable fall-through type high-speed First-In First-Out (FIFO) buffer memory organized as 64 words by four bits. The 4-bit input and output registers record and transmit, respectively, asynchronous data in parallel form. Control pins on the input and output allow for handshaking and expansion. The 4-bit wide, 62-bit deep fall-through stack has self-contained control logic.

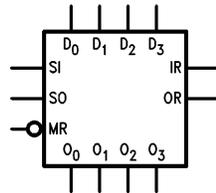
### Features

- Separate input and output clocks
- Parallel input and output
- Expandable without external logic
- 15 MHz data rate
- Supply current 160 mA max
- Available in SOIC, (300 mil only)

Commercial	Military	Package Number	Package Description
74F413PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F413DM (Note 1)	J16A	16-Lead Ceramic Dual-In-Line

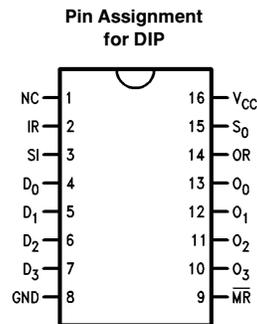
**Note 1:** Military grade device with environmental and burn-in processing. Use suffix = DMQB.

### Logic Symbol



TL/F/9541-1

### Connection Diagram



TL/F/9541-2

## Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0-D_3$	Data Inputs	1.0/0.667	20 $\mu A$ / -0.4 mA
$O_0-O_3$	Data Outputs	50/13.3	-1 mA/8 mA
IR	Input Ready	1.0/0.667	20 $\mu A$ / -0.4 mA
SI	Shift In	1.0/0.667	20 $\mu A$ / -0.4 mA
SO	Shift Out	1.0/0.667	20 $\mu A$ / -0.4 mA
OR	Output Ready	1.0/0.667	20 $\mu A$ / -0.4 mA
$\overline{MR}$	Master Reset	1.0/0.667	20 $\mu A$ / -0.4 mA

## Functional Description

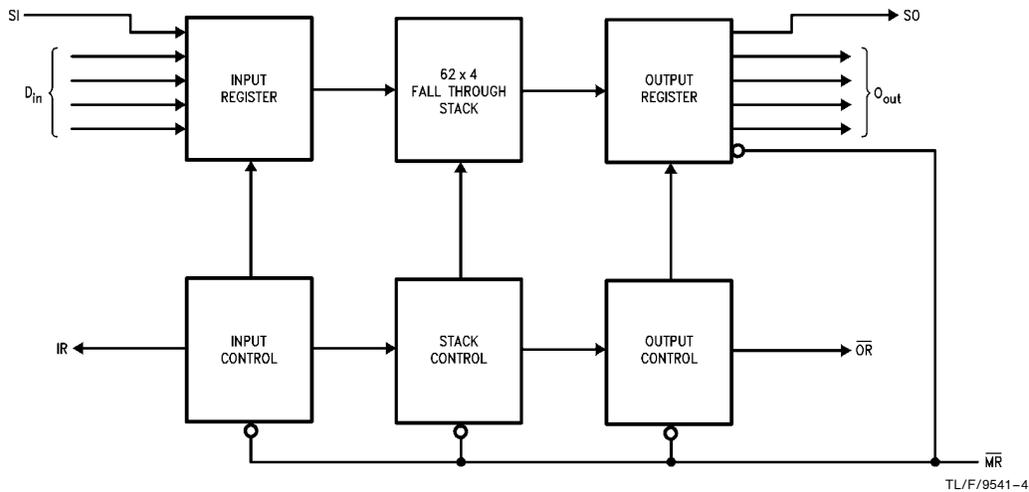
**Data Input**—Data is entered into the FIFO on  $D_0-D_3$  inputs. To enter data the Input Ready (IR) should be HIGH, indicating that the first location is ready to accept data. Data then present at the four data inputs is entered into the first location when the Shift In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, IR will remain LOW.

**Data Transfer**—Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will “bubble” to the front. The  $t_{PT}$  parameter defines the time required for the first data to travel from input to the output of a previously empty device.

**Data Output**—Data is read from the  $O_0-O_3$  outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW, the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and  $O_0-O_3$  remains as before, i.e., data does not change if FIFO is empty.

**Input Ready and Output Ready** may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least  $t_{PT}$ ) or completely empty (Output Ready stays LOW for at least  $t_{PT}$ ).

## Block Diagram



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.5	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.4 2.4 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 8 mA I <sub>OL</sub> = 8 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.4	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current			-20 -130	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		115 160		mA	Max	V <sub>O</sub> = HIGH

## AC Electrical Characteristics

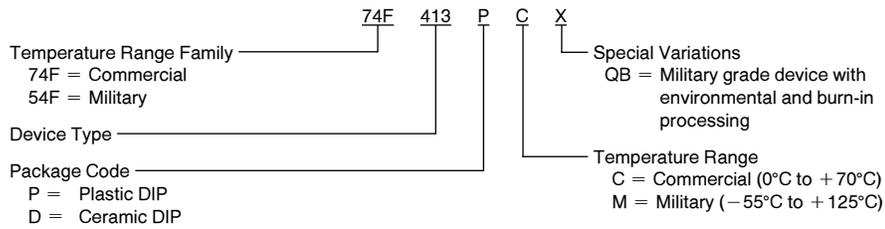
Symbol	Parameter	74F			54F		74F		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f <sub>max</sub>	Shift In Rate	10			8.0		10		MHz
f <sub>max</sub>	Shift Out Rate	10			8.0		10		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Shift In to IR	1.5		44.0	1.5	50.0	1.5	48.0	ns
		1.5		31.0	1.5	37.0	1.5	35.0	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Shift Out to OR	1.5		52.0	1.5	57.0	1.5	55.0	ns
		1.5		31.0	1.5	37.0	1.5	35.0	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Output Data Delay	1.5		46.0	1.5	52.0	1.5	50.0	ns
		1.5		34.0	1.5	39.0	1.5	37.0	
t <sub>PLH</sub>	Propagation Delay Master Reset to IR	1.5		27.0	1.5	33.0	1.5	31.0	ns
t <sub>PLH</sub>	Propagation Delay Master Reset to OR	1.5		30.0	1.5	34.0	1.5	32.0	ns

## AC Operating Requirements

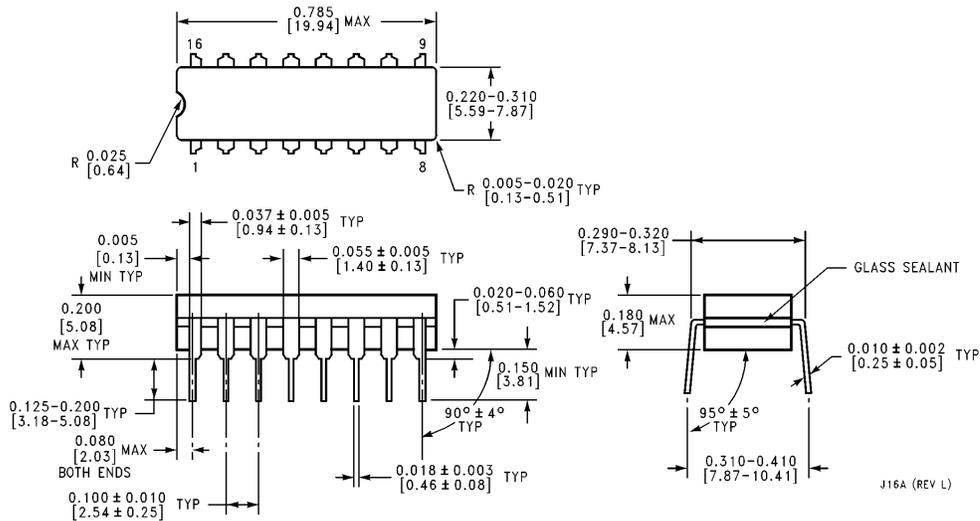
Symbol	Parameter	74F		54F		74F		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com		
		Min	Max	Min	Max	Min	Max	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW D <sub>n</sub> to SI	1.0		1.0		1.0		ns
		1.0		1.0		1.0		
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW D <sub>n</sub> to SI	10.0		10.0		10.0		ns
		10.0		10.0		10.0		
t <sub>w</sub> (H) t <sub>w</sub> (L)	Shift In Pulse Width HIGH or LOW	5.0		5.0		5.0		ns
		10.0		10.0		10.0		
t <sub>w</sub> (H) t <sub>w</sub> (L)	Shift Out Pulse Width HIGH or LOW	7.5		8.5		7.5		ns
		10.0		10.0		10.0		
t <sub>w</sub> (H)	Input Ready Pulse Width, HIGH	7.5		8.5		7.5		ns
t <sub>w</sub> (L)	Output Ready Pulse Width, LOW	5.0		5.0		5.0		ns
t <sub>w</sub> (L)	Master Reset Pulse Width, LOW	10.0		10.0		10.0		ns
t <sub>rec</sub>	Recovery Time, MR to SI	32.0		35.0		35.0		ns
t <sub>PT</sub>	Data Throughput Time		0.9		1.0		1.0	μs

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

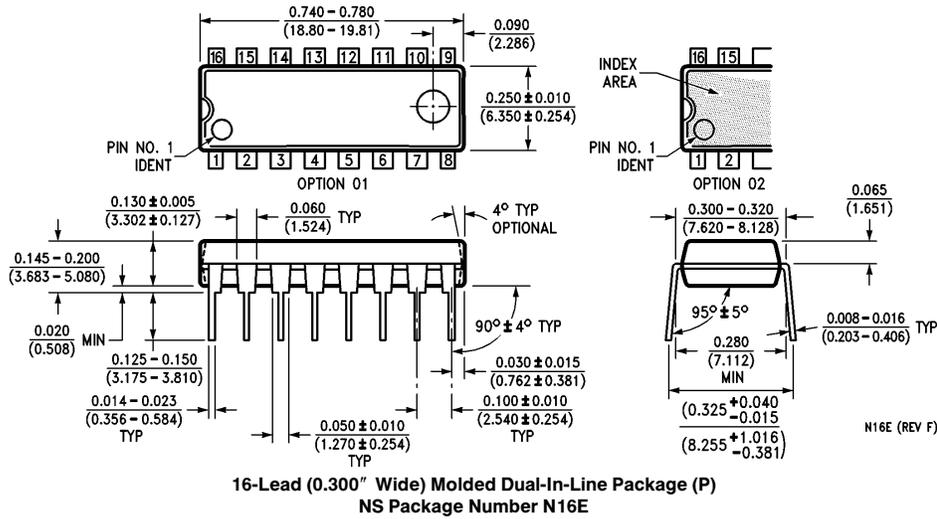


## Physical Dimensions inches (millimeters)



**16-Lead Ceramic Dual-In-Line Package (D)**  
**NS Package Number J16A**

**Physical Dimensions** inches (millimeters) (Continued)



**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

 <p><b>National Semiconductor Corporation</b> 1111 West Bardin Road Arlington, TX 76017 Tel: 1(800) 272-9959 Fax: 1(800) 737-7018</p>	<p><b>National Semiconductor Europe</b></p> <p>Fax: (+49) 0-180-530 85 86 Email: cnjwge@tevm2.nsc.com Deutsch Tel: (+49) 0-180-530 85 85 English Tel: (+49) 0-180-532 78 32 Français Tel: (+49) 0-180-532 93 58 Italiano Tel: (+49) 0-180-534 16 80</p>	<p><b>National Semiconductor Hong Kong Ltd.</b> 19th Floor, Straight Block, Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong Tel: (852) 2737-1600 Fax: (852) 2736-9960</p>	<p><b>National Semiconductor Japan Ltd.</b> Tel: 81-043-299-2309 Fax: 81-043-299-2408</p>
--	---	---	---

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.