National Semiconductor

November 1994

54F/74F219
64-Bit Random Access Memory with TRI-STATE® Outputs

General Description

The 'F219 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are TRI-STATE and are in the high-impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode. This device is similar to the 'F189 but features non-inverting, rather than inverting, data outputs.

Features

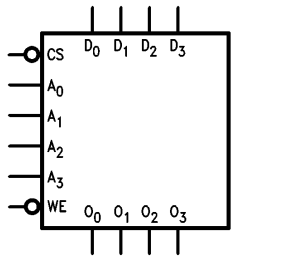
- TRI-STATE outputs for data bus applications
- Buffered inputs minimize loading
- Address decoding on-chip
- Diode clamped inputs minimize ringing
- Available in SOIC (300 mil only)

Commercial	Military	Package Number	Package Description
74F219PC		N16E	16-Lead (0.300″ Wide) Molded Dual-In-Line
	54F219DL (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F219SC (Note 1)		M16B	16-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F219SJ (Note 1)		M16D	16-Lead (0.300″ Wide) Molded Small Outline, EIAJ
	54F219FL (Note 2)	W16A	16-Lead Cerpack
	54F219LL (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DLQB, FLQB and LLQB.

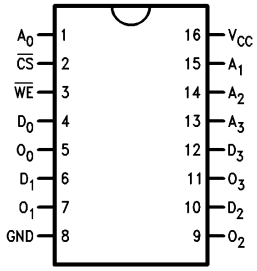
Logic Symbol



TL/F/9500–1

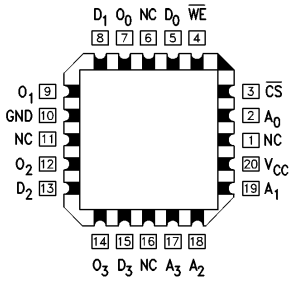
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9500–2

Pin Assignment for LCC



TL/F/9500–3

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

RRD-B30M105/Printed in U. S. A.

Unit Loading/Fan Out

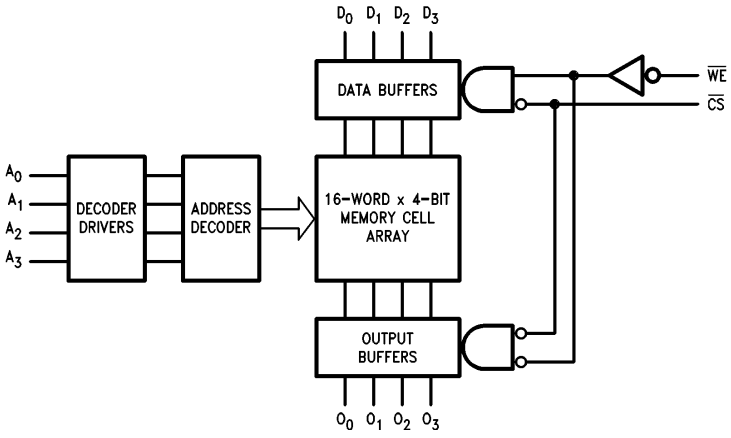
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0-A_3	Address Inputs	1.0/1.0	20 μA/$-$0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/2.0	20 μA/$-$1.2 mA
$\overline{WE}$	Write Enable Input (Active LOW)	1.0/1.0	20 μA/$-$0.6 mA
D_0-D_3	Data Inputs	1.0/1.0	20 μA/$-$0.6 mA
O_0-O_3	TRI-STATE Data Outputs	150/40 (33.3)	$-$3 mA/24 mA (20 mA)

Function Table

Inputs		Operation	Condition of Outputs
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	True Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



TL/F/9500–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +100°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (A_n, $\overline{WE}$, D_n)
					−1.2			V_{IN} = 0.5V ($\overline{CS}$)
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CC}	Power Supply Current			37	55	mA	Max	

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			54F $T_A = +100°C$ $V_{CC} = Mil$ $C_L = 50$ pF		74F $T_A, V_{CC} = Com$ $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Access Time, HIGH or LOW	10.0	18.5	26.0	9.0	32.0	10.0	27.0	ns
t_{PHL}	A_n to O_n	8.0	13.5	19.0	8.0	23.0	8.0	20.0	
t_{PZH}	Access Time, HIGH or LOW	3.5	6.0	8.5	3.5	10.5	3.5	9.5	ns
t_{PZL}	$\overline{CS}$ to O_n	5.0	9.0	13.0	5.0	15.0	5.0	14.0	
t_{PHZ}	Disable Time, HIGH or LOW	2.0	4.0	6.0	2.0	8.0	2.0	7.0	
t_{PLZ}	$\overline{CS}$ to O_n	3.0	5.5	8.0	2.5	10.0	3.0	9.0	
t_{PZH}	Write Recovery Time	6.5	20.0	28.0	6.5	37.5	6.5	29.0	ns
t_{PZL}	HIGH or LOW, $\overline{WE}$ to O_n	6.5	11.0	15.5	6.5	17.5	6.5	16.5	
t_{PHZ}	Disable Time, HIGH or LOW	4.0	7.0	10.0	3.5	12.0	4.0	11.0	
t_{PLZ}	$\overline{WE}$ to O_n	5.0	9.0	13.0	5.0	15.0	5.0	14.0	

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A = +100°C$ $V_{CC} = Mil$		74F $T_A, V_{CC} = Com$		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$	Setup Time, HIGH or LOW	0		0		0		ns
$t_s(L)$	A_n to $\overline{WE}$	0		0		0		
$t_h(H)$	Hold Time, HIGH or LOW	2.0		2.0		2.0		
$t_h(L)$	A_n to $\overline{WE}$	2.0		2.0		2.0		
$t_s(H)$	Setup Time, HIGH or LOW	10.0		11.0		10.0		ns
$t_s(L)$	D_n to $\overline{WE}$	10.0		11.0		10.0		
$t_h(H)$	Hold Time, HIGH or LOW	0		2.0		0		
$t_h(L)$	D_n to $\overline{WE}$	0		2.0		0		
$t_s(L)$	Setup Time, LOW $\overline{CS}$ to $\overline{WE}$	0		0		0		ns
$t_h(L)$	Hold Time, LOW $\overline{CS}$ to $\overline{WE}$	6.0		7.5		6.0		
$t_w(L)$	$\overline{WE}$ Pulse Width, LOW	6.0		15.0		6.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F 219 S C X

Temperature Range Family
- 74F = Commercial
- 54F = Military

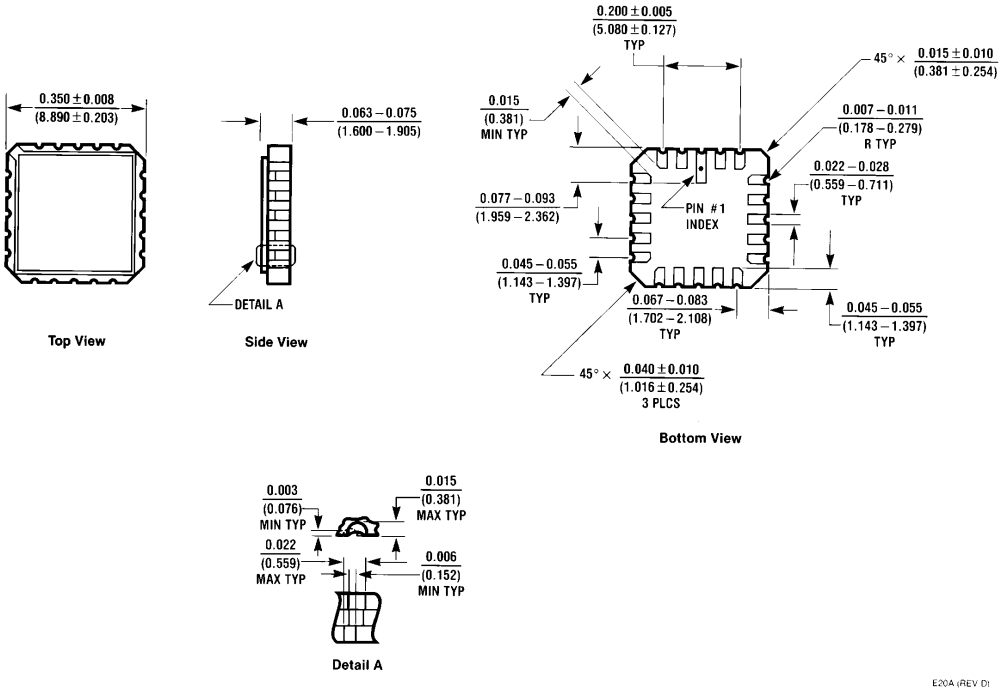
Device Type

Package Code
- P = Plastic DIP
- D = Ceramic DIP
- F = Flatpak
- L = Leadless Chip Carrier (LCC)
- S = Small Outline SOIC JEDEC
- SJ = Small Outline SOIC EIAJ

Special Variations
- QB = Military grade device with environmental and burn-in processing
- X = Devices shipped in 13″ reel

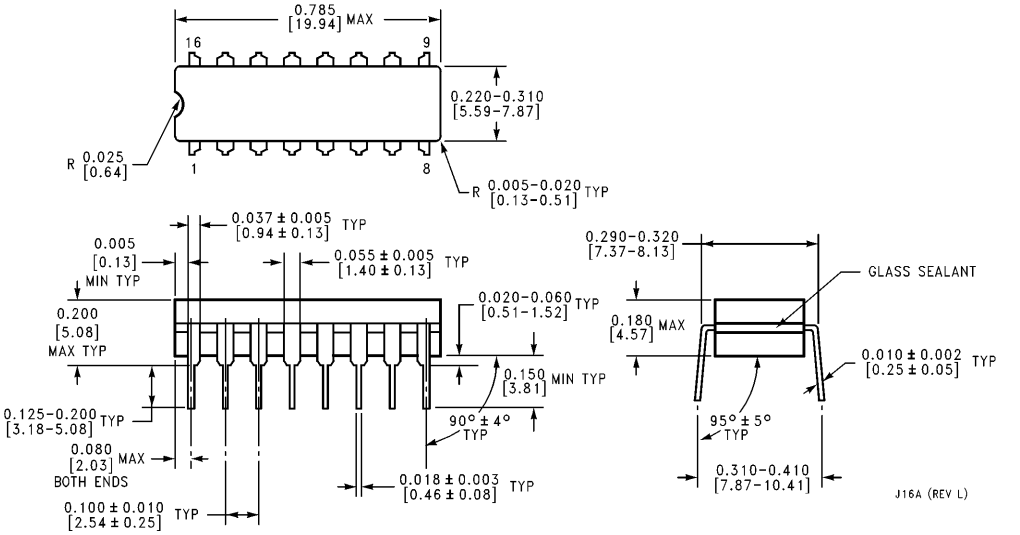
Temperature Range
- C = Commercial (0°C to +70°C)
- L = Military (−55°C to +100°C)

Physical Dimensions inches (millimeters)

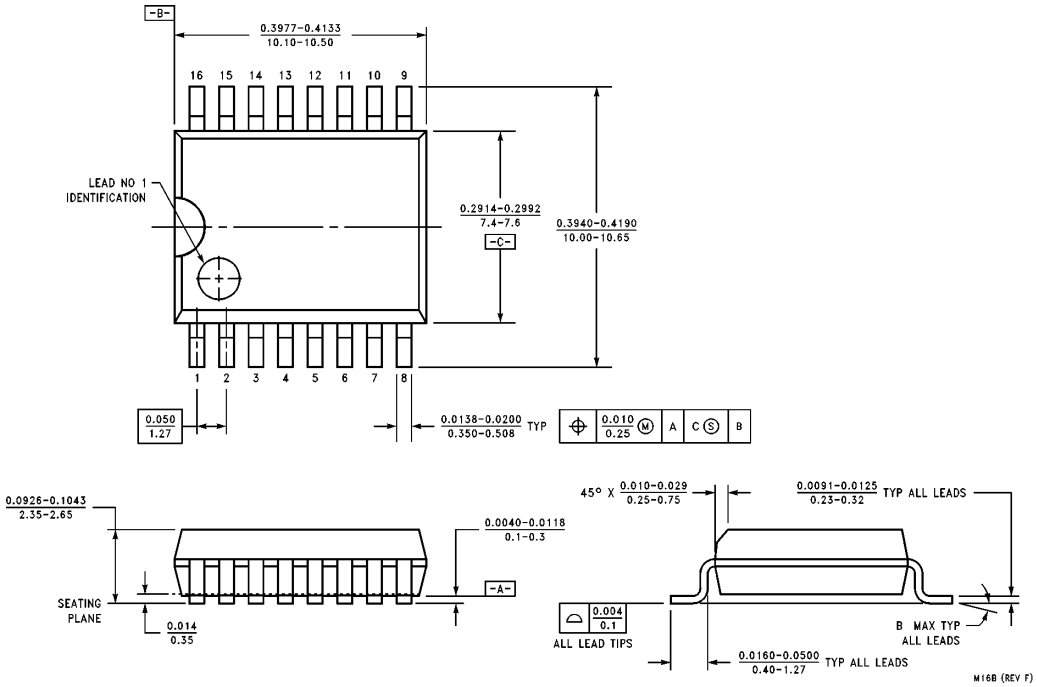


20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

Physical Dimensions inches (millimeters) (Continued)

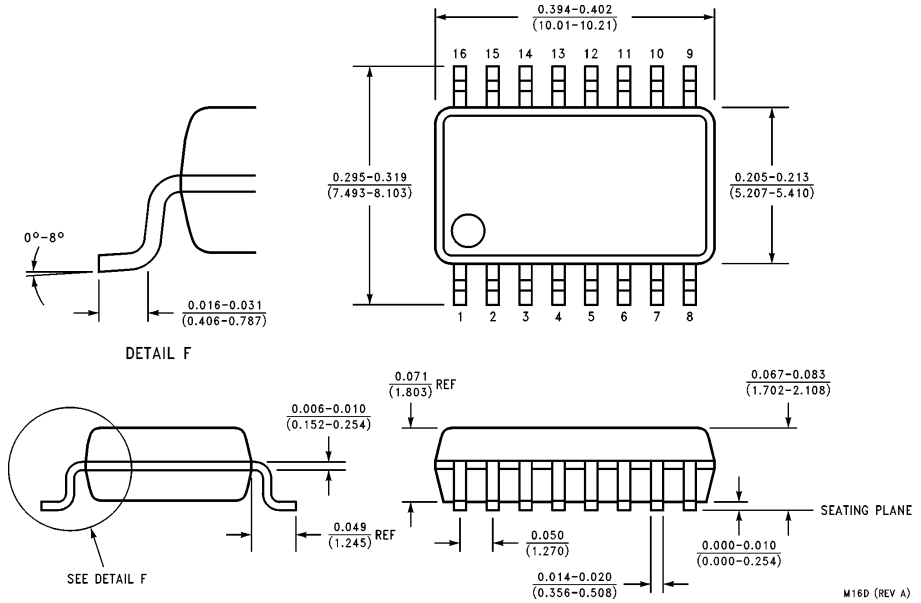


16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

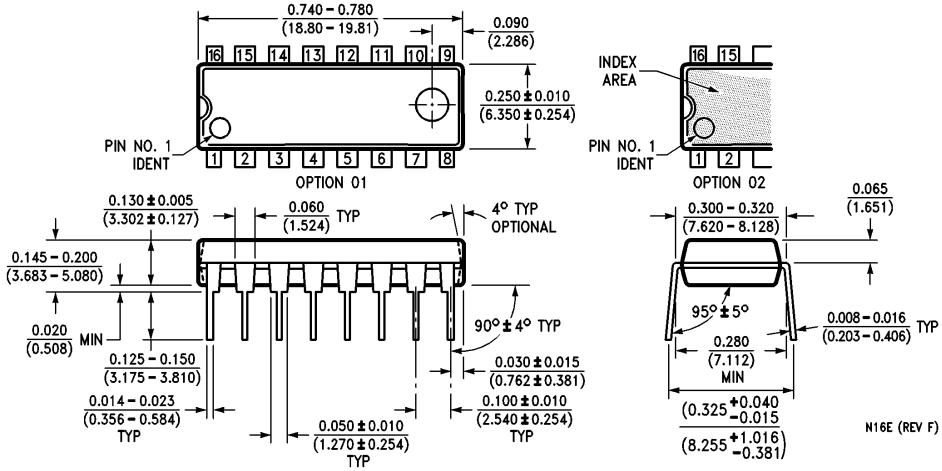


16-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16B

Physical Dimensions inches (millimeters) (Continued)

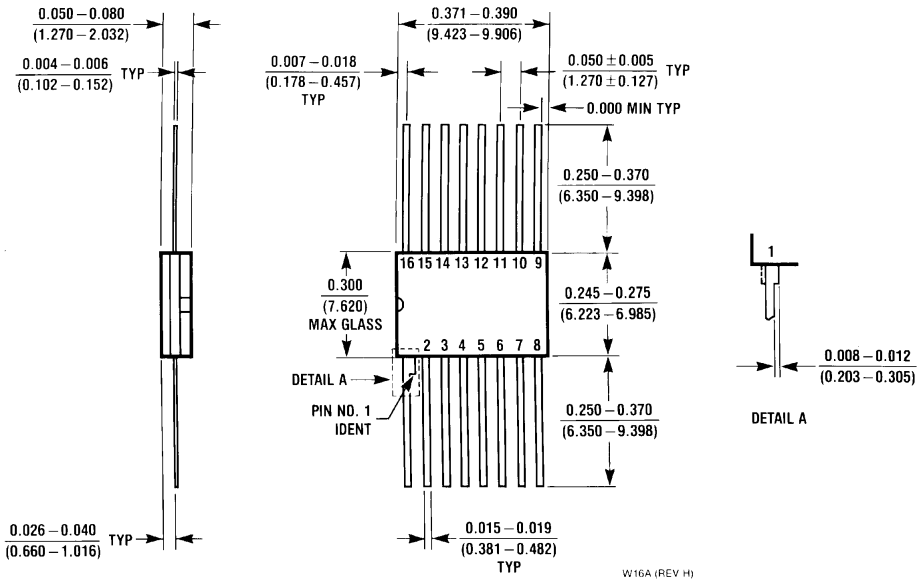


16-Lead (0.300″ Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D



16-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flatpak (F)
NS Package Number W16A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408