National Semiconductor

August 1998

# 54ACTQ533
# Quiet Series Octal Transparent Latch with TRI-STATE® Outputs

## General Description

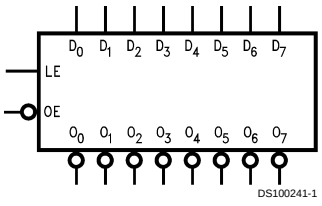
The ACTQ533 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

The ACTQ533 utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

## Features

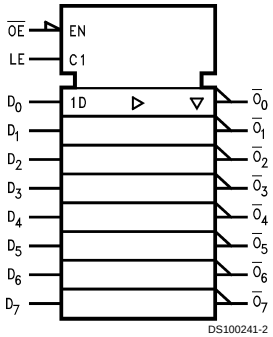
- $I_{CC}$ and $I_{OZ}$ reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch up immunity
- Eight latches in a single package
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Inverted version of the ACTQ373
- 4 kV minimum ESD immunity

## Logic Symbols




DS100241-1

IEEE/IEC




DS100241-2

| Pin Names | Description |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| LE | Latch Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{O}_0$–$\overline{O}_7$ | TRI-STATE Latch Outputs |

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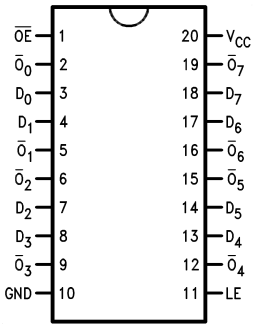
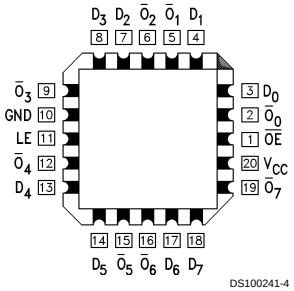
## Connection Diagrams

**Pin Assignment for DIP and Flatpak**




DS100241-3

**Pin Assignment for LCC**

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## Functional Description

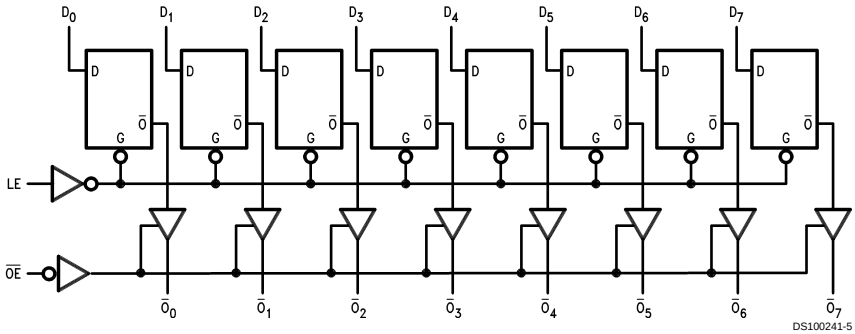
The ACTQ533 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the $D_n$ inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

## Truth Table

| Inputs | | | Outputs |
|---|---|---|---|
| **LE** | $\overline{\textbf{OE}}$ | $\mathbf{D_n}$ | $\overline{\mathbf{O}}_\mathbf{n}$ |
| X | H | X | Z |
| H | L | L | H |
| H | L | H | L |
| L | L | X | $\overline{O}_0$ |

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
$\overline{O}_0$ = Previous $\overline{O}_0$ before HIGH to Low transition of Latch Enable

## Logic Diagram

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Source or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current per Output Pin ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| Storage Temperature ($T_{STG}$) | −65˚C to +150˚C |
| DC Latchup Source or Sink Current | ±300 mA |
| Junction Temperature ($T_J$) | |
| CDIP | 175˚C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| 'ACTQ | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | |
| 54ACTQ | −55˚C to +125˚C |
| Minimum Input Edge Rate ΔV/Δt | |
| 'ACTQ Devices $V_{IN}$ from 0.8V to 2.0V $V_{CC}$ @ 4.5V, 5.5V | 125 mV/ns |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

**Note 2:** All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40˚C to +125˚C.

## DC Characteristics for 'ACTQ Family Devices

| Symbol | Parameter | $V_{CC}$ (V) | 54ACTQ $T_A$ = −55˚C to +125˚C Guaranteed Limits | Units | Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High Level Input Voltage | 4.5<br>5.5 | 2.0<br>2.0 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 4.5<br>5.5 | 0.8<br>0.8 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| $V_{OH}$ | Minimum High Level Output Voltage | 4.5<br>5.5 | 4.4<br>5.4 | V | $I_{OUT}$ = −50 μA |
| | | | | | (Note 3) $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 4.5<br>5.5 | 3.70<br>4.70 | V | $I_{OH}$ = −24 mA<br>$I_{OH}$ = −24 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 4.5<br>5.5 | 0.1<br>0.1 | V | $I_{OUT}$ = 50 μA |
| | | | | | (Note 3) $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 4.5<br>5.5 | 0.50<br>0.50 | V | $I_{OL}$ = 24 mA<br>$I_{OL}$ = 24 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OZ}$ | Maximum TRI-STATE Leakage Current | 5.5 | ±5.0 | μA | $V_I$ = $V_{IL}$, $V_{IH}$<br>$V_O$ = $V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 1.6 | mA | $V_I$ = $V_{CC}$ − 2.1V |

## DC Characteristics for 'ACTQ Family Devices (Continued)

| Symbol | Parameter | $V_{CC}$ (V) | 54ACTQ $T_A$ = −55°C to +125°C Guaranteed Limits | Units | Conditions |
|---|---|---|---|---|---|
| $I_{OLD}$ | Minimum Dynamic | 5.5 | 50 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | Output Current (Note 4) | 5.5 | −50 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | 80.0 | µA | $V_{IN}$ = $V_{CC}$ or GND (Note 5) |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 5.0 | 1.7 | V | (Notes 6, 7) |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 5.0 | −1.2 | V | (Notes 6, 7) |

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:** $I_{CC}$ for 54ACTQ @ 25°C is identical to 74ACQ @ 25°C.

**Note 6:** Plastic DIP package.

**Note 7:** Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) (Note 8) | 54ACTQ $T_A$ = −55°C to +125°C $C_L$ = 50 pF Min | 54ACTQ $T_A$ = −55°C to +125°C $C_L$ = 50 pF Max | Units | Fig. No. |
|---|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay $D_n$ to $O_n$ | 5.0 | 1.5 | 9.0 | ns | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay LE to $O_n$ | 5.0 | 1.5 | 10.5 | ns | |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time | 5.0 | 1.5 | 10.5 | ns | |
| $t_{PHZ}$, $t_{PLZ}$ | Output Disable Time | 5.0 | 1.5 | 10.5 | ns | |

**Note 8:** Voltage Range 5.0 is 5.0V ±0.5V.

**Note 9:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ($t_{OSHL}$) or LOW to HIGH ($t_{OSLH}$). Parameter guaranteed by design.

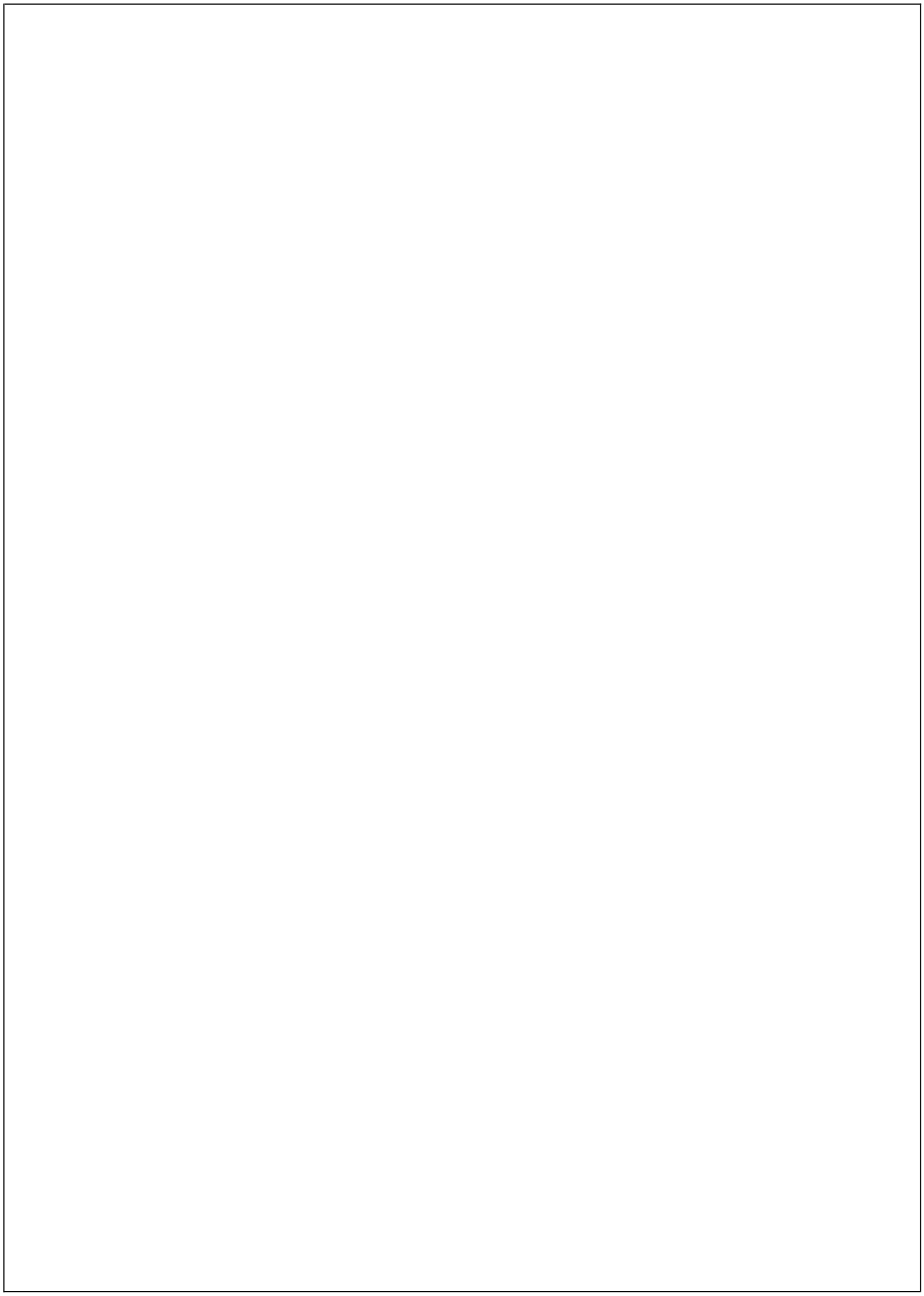
## AC Operating Requirements

| Symbol | Parameter | $V_{CC}$ (V) (Note 10) | 54ACTQ $T_A$ = −55°C to +125°C $C_L$ = 50 pF Guaranteed Minimum | Units | Fig. No. |
|---|---|---|---|---|---|
| $t_S$ | Setup Time, HIGH or LOW $D_n$ to LE | 5.0 | 3.0 | ns | |
| $t_H$ | Hold Time, HIGH or LOW $D_n$ to LE | 5.0 | 1.5 | ns | |
| $t_W$ | LE Pulse Width, HIGH | 5.0 | 5.0 | ns | |

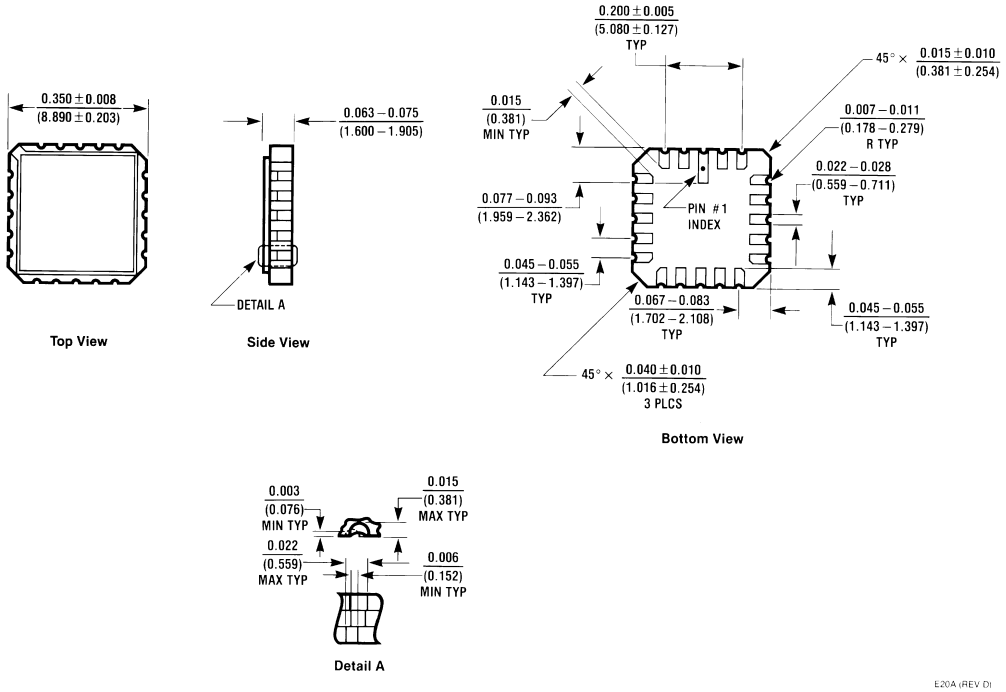
**Note 10:** Voltage Range 5.0 is 5.0V ±0.5V.

## Capacitance

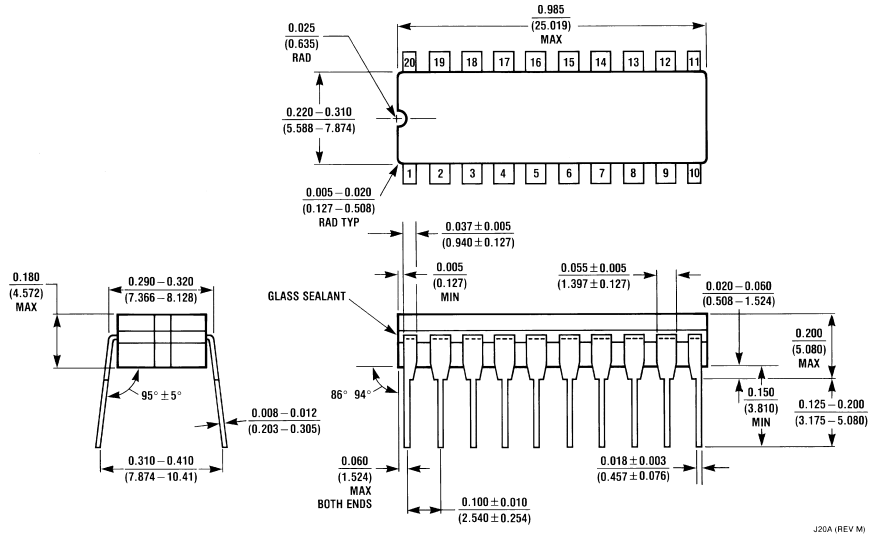
| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = OPEN |
| $C_{PD}$ | Power Dissipation Capacitance | 40 | pF | $V_{CC}$ = 5.0V |



## Physical Dimensions inches (millimeters) unless otherwise noted

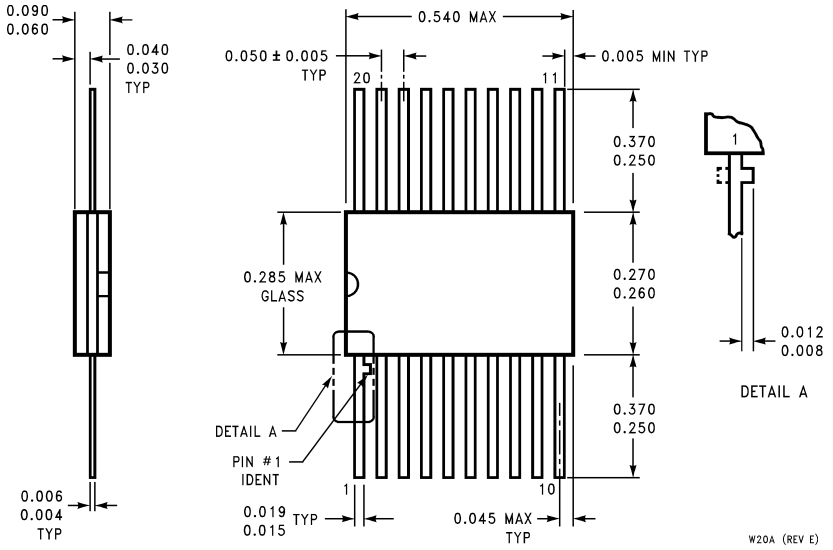



**20-Terminal Ceramic Leadless Chip Carrier (L)**
**NS Package Number E20A**




**20-Lead Ceramic Dual-In-Line Package (D)**
**NS Package Number J20A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead Ceramic Flatpak (F)**
**NS Package Number W20A**

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