National Semiconductor

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54ACTQ16373
16-Bit Transparent Latch with TRI-STATE®Outputs

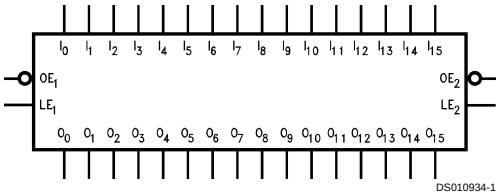
General Description

The 'ACTQ16373 contains sixteen non-inverting latches with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state. The 'ACTQ16373 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™output control for superior performance.

Features

- Utilizes NSC FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Separate control logic for each byte
- 16-bit version of the 'ACTQ373
- Outputs source/sink 24 mA
- Standard Microcircuit Drawing (SMD) 5962-9561801

Logic Symbol



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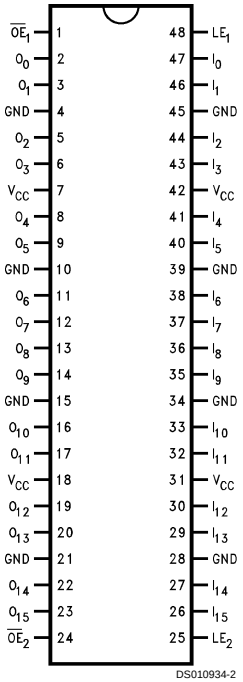
Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
LE_n	Latch Enable Input
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

Connection Diagram

Pin Assignment for CERPAK



DS010934-2

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Functional Description

The 'ACTQ16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

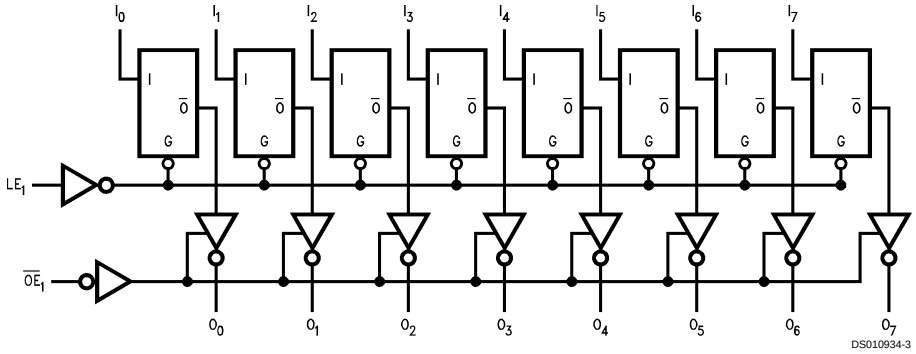
Truth Table

Inputs			Outputs
LE_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	(Previous)

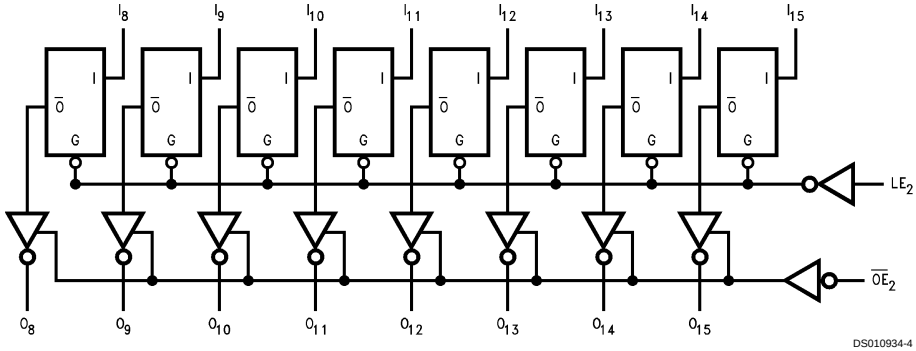
Inputs			Outputs
LE_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	(Previous)

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
Previous = previous output prior to HIGH to LOW transition of LE

Logic Diagrams



DS010934-3



DS010934-4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	+50 mA
DC V_{CC} or Ground Current per Output Pin	+50 mA
Junction Temperature	
CDIP	+175˚C
Storage Temperature	−65˚C to +150˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54ACTQ	−55˚C to +125˚C
Minimum Input Edge Rate (dV/dt)	
'ACTQ Devices	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	54ACTQ T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Input Voltage	4.5 5.5	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Input Voltage	4.5 5.5	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Output Voltage	4.5 5.5	4.4 5.4	V	I_{OUT} = −50 µA
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		4.5 5.5	3.70 4.70	V	I_{OH} = −24 mA I_{OH} = −24 mA
V_{OL}	Maximum Low Output Voltage	4.5 5.5	0.1 0.1	V	I_{OUT} = 50 µA
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		4.5 5.5	0.50 0.50	V	I_{OL} = 24 mA I_{OL} = 24 mA
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5	±10.0	µA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} − 2.1V
I_{CC}	Max Quiescent Supply Current	5.5	160.0	µA	V_{IN} = V_{CC} or GND (Note 7)
I_{OLD}	Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 3)		50	mA	V_{OHD} = 3.85V Min
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.8	V	(Notes 4, 5)

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54ACTQ T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	-0.8	V	(Notes 4, 5)

Note 2: All outputs loaded; thesholds associated with output unders test.

Note 3: Maximum test duration 2.0 ms; one output loaded at a time.

Note 4: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched LOW and one output held LOW.

Note 5: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched HIGH and one output held HIGH.

Note 6: Max number of data inputs (n) switching, (n − 1) input switching 0V to 3V ('ACTQ). Input under test switching 3V to threshold (V_{ILD})

Note 7: I_{CC} for 54ACTQ @ 25°C is indentical to 74ACTQ @ 25°C.

AC Electrical Characteristics:

Symbol	Parameter	V_{CC} (V) (Note 8)	54ACTQ T_A = −55°C to+125°C C_L = 50 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay	5.0	3.0	10.5	ns
t_{PHL}	D_n to O_n		3.0	10.0	
t_{PLH}	Propagation Delay	5.0	3.0	11.0	ns
t_{PHL}	LE to O_n		3.0	10.0	
t_{PZH}	Output Enable	5.0	2.5	10.0	ns
t_{PZL}	Delay		2.5	11.0	
t_{PHZ}	Output Disable	5.0	2.0	9.0	ns
t_{PLZ}	Delay		2.0	9.0	

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements:

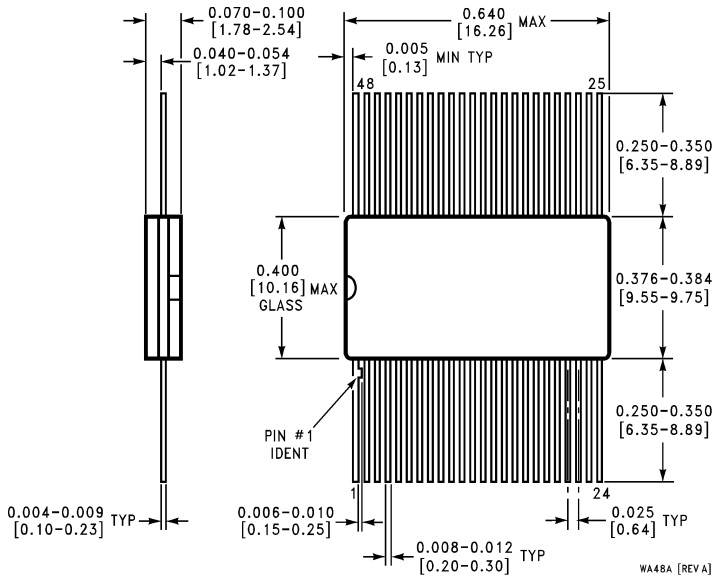
Symbol	Parameter	V_{CC} (V) (Note 9)	54ACTQ −55°C to +125°C 50 pF Guaranteed Minimum	Units
t_S	Setup Time, HIGH or LOW, Input to Clock	5.0	3.0	ns
t_h	Hold time, High or LOW, Input to Clock	5.0	1.5	ns
t_w	CS Pulse Width, HIGH or LOW	5.0	4.0	ns

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation	95	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead CERPAK
NS Package Number WA48A

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