

# 54ACTQ16244

## 16-Bit Buffer/Line Driver with TRI-STATE® Outputs

### General Description

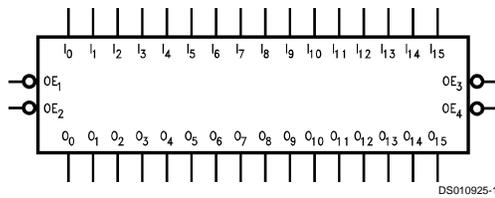
The 'ACTQ16244 contains sixteen non-inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation.

The 'ACTQ16244 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series® features GTO® output control for superior performance.

### Features

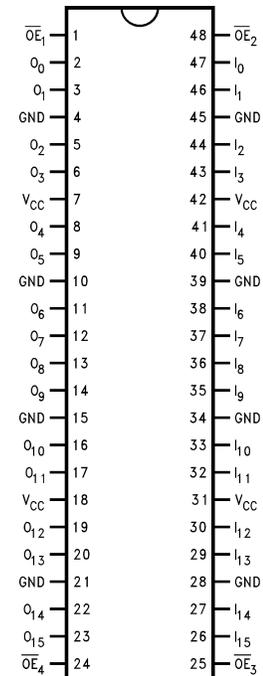
- Utilizes NSC FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Separate control logic for each byte and nibble
- 16-bit version of the 'ACTQ244
- Outputs source/sink 24 mA
- Standard Microcircuit Drawing (SMD) 5962-9561901

### Logic Symbol



### Connection Diagram

Pin Assignment for CERPAK



### Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	Outputs

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 TRI-STATE® is a registered trademark of National Semiconductor Corporation.  
 FACT™ and FACT Quiet Series™ are trademarks of Fairchild Semiconductor Corporation.

## Functional Description

The 'ACTQ16244 contains sixteen non-inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable ( $\overline{OE}_n$ ) input for each nibble. When  $\overline{OE}_n$  is LOW, the outputs are in 2-state mode. When  $\overline{OE}_n$  is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

## Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I <sub>0</sub> -I <sub>3</sub>	O <sub>0</sub> -O <sub>3</sub>
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I <sub>8</sub> -I <sub>11</sub>	O <sub>8</sub> -O <sub>11</sub>
L	L	L
L	H	H

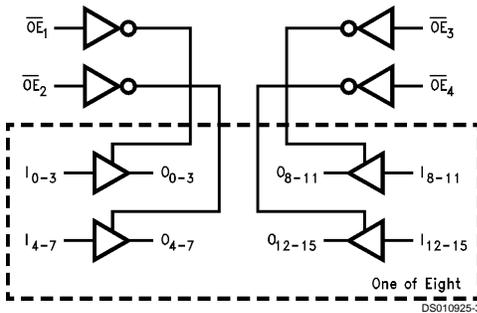
Inputs		Outputs
$\overline{OE}_3$	I <sub>8</sub> -I <sub>11</sub>	O <sub>8</sub> -O <sub>11</sub>
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I <sub>4</sub> -I <sub>7</sub>	O <sub>4</sub> -O <sub>7</sub>
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I <sub>12</sub> -I <sub>15</sub>	O <sub>12</sub> -O <sub>15</sub>
L	L	L
L	H	H
H	X	Z

H = High Voltage Level  
 L = Low Voltage Level  
 X = Immaterial  
 Z = High Impedance

## Logic Diagram



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source/Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin	±50 mA
Junction Temperature C-DIP	+175°C
Storage Temperature	-65°C to +150°C

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ ) 'ACTQ	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ ) 54ACTQ	-55°C to +125°C
Minimum Input Edge Rate (dV/dt) 'ACTQ Devices	125 mV/ns
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	$V_{CC}$ (V)	54ACTQ	Units	Conditions
			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		
			Guaranteed Limits		
$V_{IH}$	Minimum High Input Voltage	4.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	2.0		
$V_{IL}$	Maximum Low Input Voltage	4.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	0.8		
$V_{OH}$	Minimum High Output Voltage	4.5	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.4		
		4.5	3.70	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
		5.5	4.70		
$V_{OL}$	Maximum Low Output Voltage	4.5	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.1		
		4.5	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = 24 \text{ mA}$ $I_{OH} = 24 \text{ mA}$
		5.5	0.50		
$I_{OZ}$	Maximum TRI-STATE Leakage Current	5.5	±10.0	µA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{GND}$
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}, \text{GND}$
$I_{CCT}$	Maximum $I_{CC}$ /Input	5.5	1.6	mA	$V_I = V_{CC} - 2.1V$
$I_{CC}$	Max Quiescent Supply Current	5.5	160.0	µA	$V_{IN} = V_{CC}$ or GND (Note 5)
$I_{OLD}$	Minimum Dynamic Output Current (Note 3)	5.5	50	mA	$V_{OLD} = 1.65V$ Max
$I_{OHD}$			50	mA	$V_{OHD} = 3.85V$ Min
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	5.0	0.8	V	(Notes 4, 5)
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	5.0	-0.8	V	(Notes 4, 5)

**Note 2:** All outputs loaded; thresholds associated with output under test.

## DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

**Note 3:** Maximum test duration 2.0 ms; one output loaded at a time.

**Note 4:** Maximum number of outputs that can switch simultaneously is n. (n - 1) outputs are switched LOW and one output held LOW.

**Note 5:** Maximum number of outputs that can switch simultaneously is n. (n - 1) outputs are switched HIGH and one output held HIGH.

**Note 6:** Max number of data inputs (n) switching. (n - 1) input switching 0V to 3V ('ACTQ) input under test switching 3V to threshold ( $V_{ILD}$ )

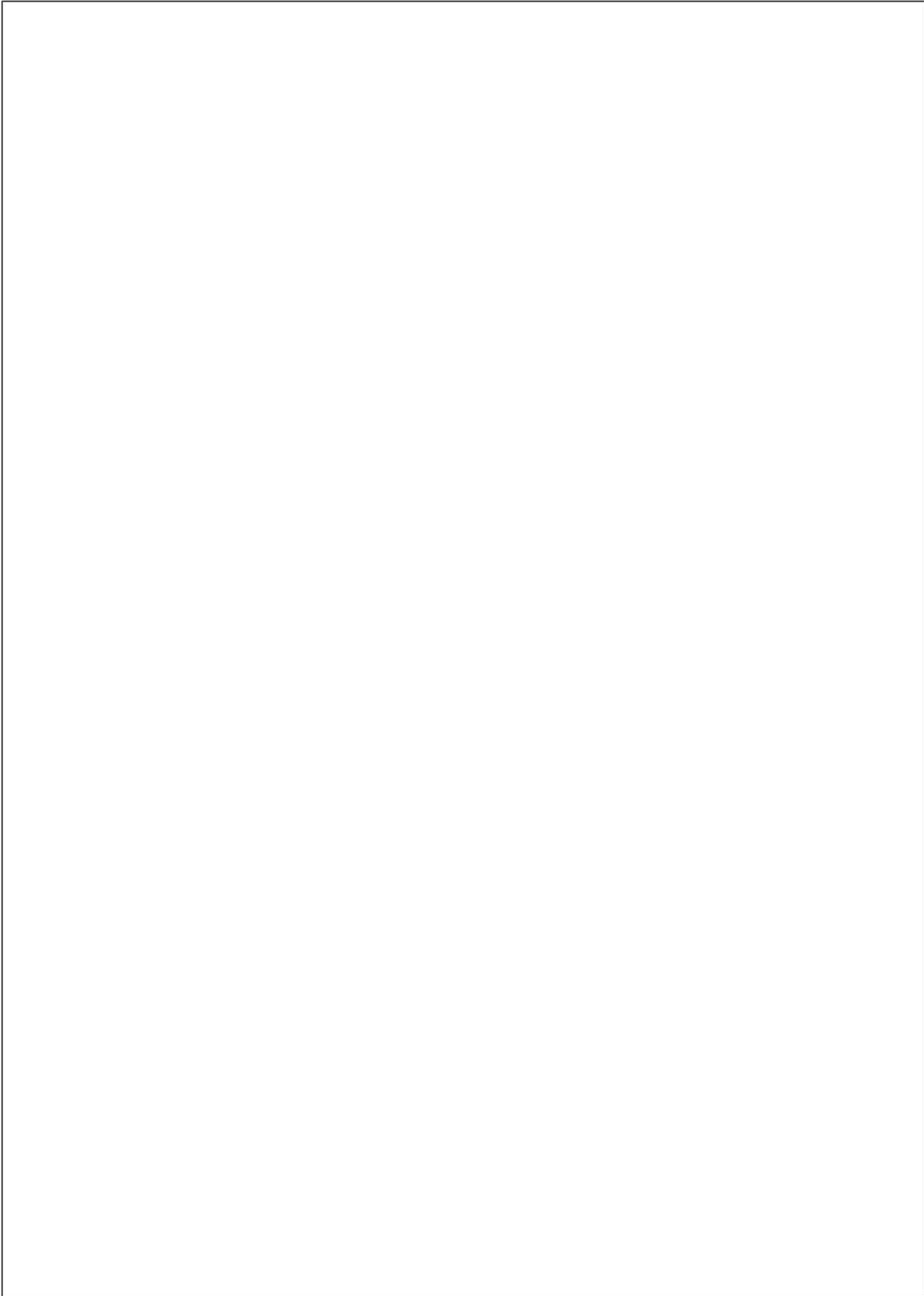
## AC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V) (Note 7)	54ACTQ		Units
			$T_A =$ -55°C to +125°C $C_L = 50$ pF		
			Min	Max	
$t_{PLH}$	Propagation Delay	5.0	2.5	10.0	ns
$t_{PHL}$	$A_n, B_n$ to $B_n, A_n$		2.5	9.5	
$t_{PZH}$	Output Enable	5.0	2.5	9.5	ns
$t_{PZL}$	Time		2.5	10.5	
$t_{PHZ}$	Output Disable	5.0	2.0	9.5	ns
$t_{PLZ}$	Time		2.0	9.5	

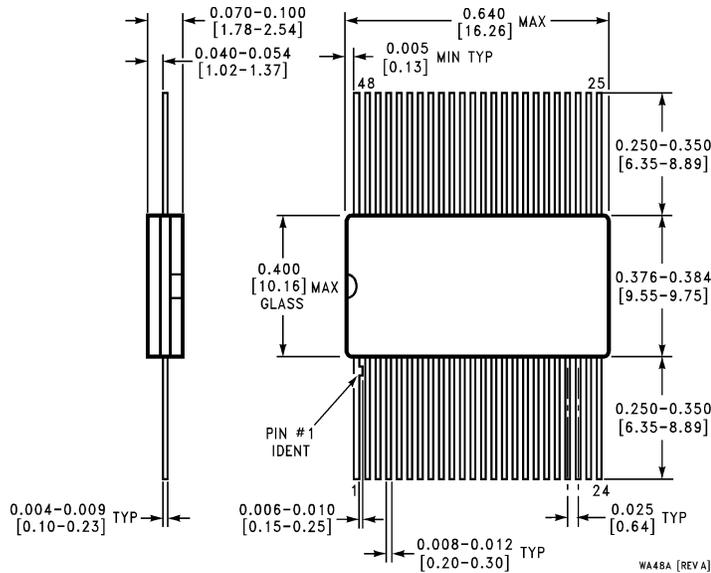
**Note 7:** Voltage Range 5.0 is 5.0V  $\pm$ 0.5V.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Pin Capacitance	4.5	pF	$V_{CC} = 5.0V$
$C_{PD}$	Power Dissipation Capacitance	95	pF	$V_{CC} = 5.0V$



**Physical Dimensions** inches (millimeters) unless otherwise noted



**48-Lead CERPAK (F)  
NS Package Number WA48A**

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