National *Semiconductor*

54ACT823
9-Bit D Flip-Flop

General Description

The ACT823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The ACT823 offers noninverting outputs and is fully compatible with AMD's Am29823.

Features

■ Outputs source/sink 24 mA

■ TRI-STATE outputs for bus interfacing
■ Inputs and outputs are on opposite sides
■ ACT823 has TTL-compatible inputs
■ Standard Microcircuit Drawing (SMD) 5962-9161001

Ordering Code

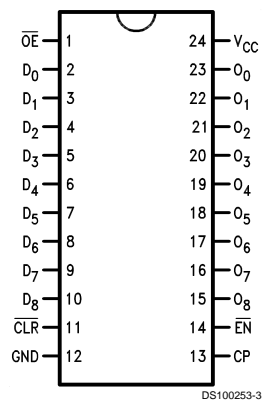| Order Number	Package Number	Package Description
54ACT823DMQB	J24A	24-Lead Ceramic Dual-in-line
54ACT823FMQB	W24C	24-Lead Cerpack
54ACT823LMQB	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C

Logic Symbols

DS100253-1

IEEE/IEC

DS100253-2
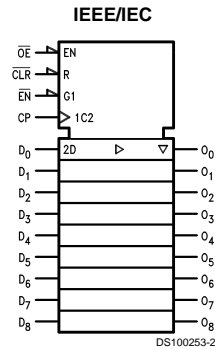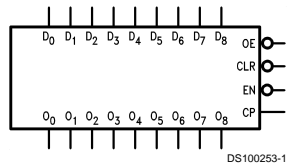
Pin Names	Description
D_0–D_8	Data Inputs
O_0–O_8	Data Outputs
$\overline{OE}$	Output Enable
$\overline{CLR}$	Clear
CP	Clock Input
$\overline{EN}$	Clock Enable

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TRI-STATE™ is a trademark of National Semiconductor Corporation.

Connection Diagrams

**Pin Assignment for DIP
and Cerpack**

$\overline{OE}$	1	24	V_{CC}
D_0	2	23	O_0
D_1	3	22	O_1
D_2	4	21	O_2
D_3	5	20	O_3
D_4	6	19	O_4
D_5	7	18	O_5
D_6	8	17	O_6
D_7	9	16	O_7
D_8	10	15	O_8
$\overline{CLR}$	11	14	$\overline{EN}$
GND	12	13	CP

DS100253-3

**Pin Assignment
for LCC**

D_7 D_6 D_5 NC D_4 D_3 D_2
11 10 9 8 7 6 5

D_8	12	4 D_1
$\overline{CLR}$	13	3 D_0
GND	14	2 $\overline{OE}$
NC	15	1 NC
CP	16	28 V_{CC}
$\overline{EN}$	17	27 O_0
O_8	18	26 O_1

19 20 21 22 23 24 25
O_7 O_6 O_5 NC O_4 O_3 O_2

DS100253-4
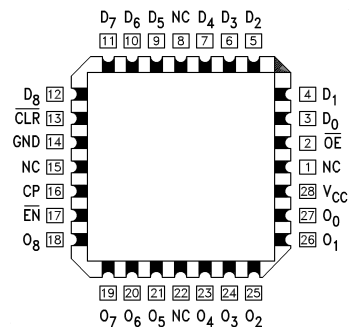
Functional Description

The ACT823 consists of nine D-type edge-triggered flip-flops. These have TRI-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}$ LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. In addition to the Clock and Output En-able pins, there are Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These devices are ideal for parity bus interfacing in high performance systems.

When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	Q	O	
H	X	L	N	L	L	Z	High Z
H	X	L	N	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	N	L	L	Z	Load
H	H	L	N	H	H	Z	Load
L	H	L	N	L	L	L	Load
L	H	L	N	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
N = LOW-to-HIGH Transition
NC = No Change

Logic Diagram

DS100253-5
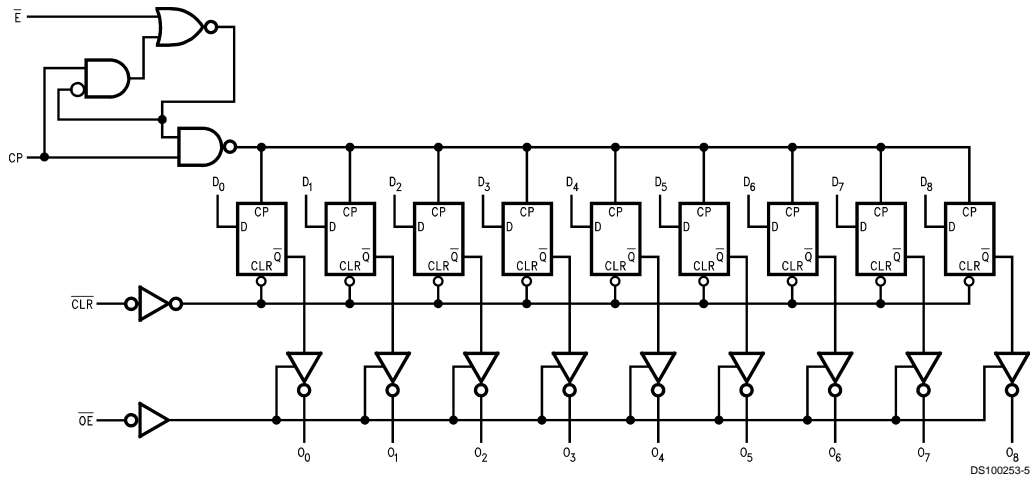
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current	
(I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Junction Temperature (T_J)	
CDIP	175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −55°C to +125°C	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		4.5	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	3.7	V	I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.5	V	I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5	±10.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} −2.1V
I_{OLD}	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	160	μA	V_{IN} = V_{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 4)	T_A = −55°C to +125°C C_L = 50 pF		Units
			Min	Max	
f_{max}	Maximum Clock Frequency	5.0	95		MHz
t_{PLH}	Propagation Delay CP to O_n	5.0	1.0	12.0	ns

AC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V) (Note 4)	T_A = −55°C to +125°C C_L = 50 pF		Units
			Min	**Max**	
t_{PHL}	Propagation Delay CP to O_n	5.0	1.0	12.0	ns
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0	1.0	18.0	ns
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	1.0	11.5	ns
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	1.0	12.0	ns
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.0	13.5	ns
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.0	12.0	ns

Note 4: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}(V) (Note 5)	T_A = −55°C to +125°C C_L = 50 pF Guaranteed Minimum	Units
t_s	Setup Time, HIGH or LOW D to CP	5.0	4.0	ns
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	3.0	ns
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	5.0	4.0	ns
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	5.0	3.0	ns
t_w	CP Pulse Width HIGH or LOW	5.0	6.0	ns
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	7.5	ns
t_{rec}	$\overline{CLR}$ to CP Recovery Time	5.0	4.5	ns

Note 5: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	4.4	pF	V_{CC} = 5.0V

## Physical Dimensions inches (millimeters) unless otherwise noted

1.290
(32.766)
MAX

0.600
(15.240)
MAX
GLASS

24 23 22 21 20 19 18 17 16 15 14 13

0.025
(0.635)
RAD

0.514−0.526
(13.06−13.36)

1 2 3 4 5 6 7 8 9 10 11 12

0.030−0.055
(0.762−1.397)
RAD TYP

0.590−0.620
(14.986−15.748)

0.005
(0.127)
MIN

GLASS
SEALANT

0.055 ±0.005
(1.397 ±0.127)

0.180
(4.572)
MAX

0.020−0.070
(0.508−1.778)

95° ±5°

0.008−0.012
(0.203−0.305)

0.685 +0.025
       −0.060

(17.40 +0.635
        −1.524)

0.098
(2.489)
MAX

0.100 ±0.010
(2.540 ±0.254)

0.018 ±0.003
(0.457 ±0.076)

86°
94°
TYP

0.125−0.200
(3.175−5.080)
MIN

0.150
(3.810)
MIN
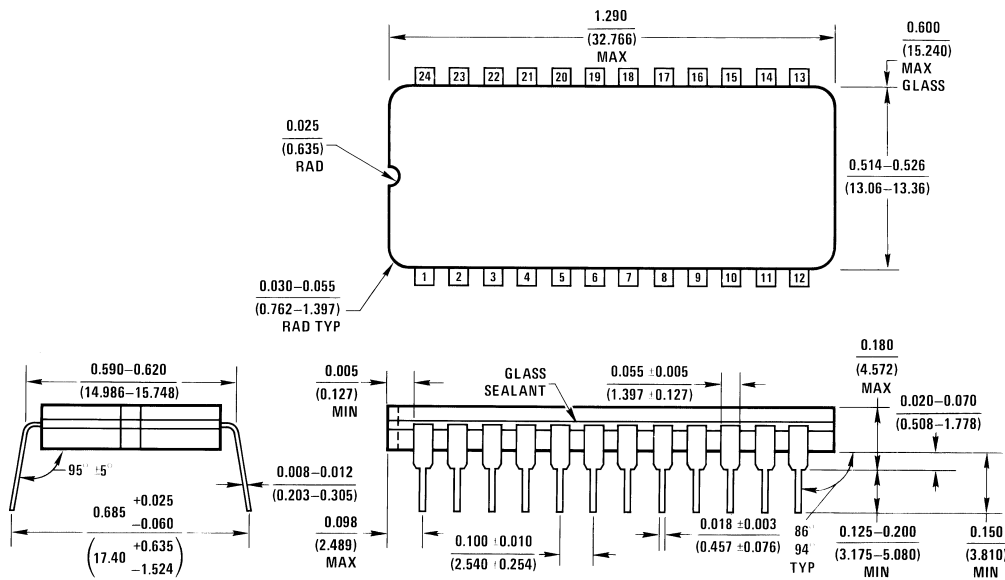
J24A (REV H)

24 Lead Ceramic Dual-in-line
Package Number J24A

0.090
0.060

0.040
0.030

0.625
0.590

0.050 ±0.005

0.005 MIN TYP

24

13

0.370
0.250

0.015
0.008

0.420 MAX

0.019
0.015 TYP

0.015
0.008

0.370
0.250

SEE
DETAIL A

1

12

0.006
0.004

0.045 MAX
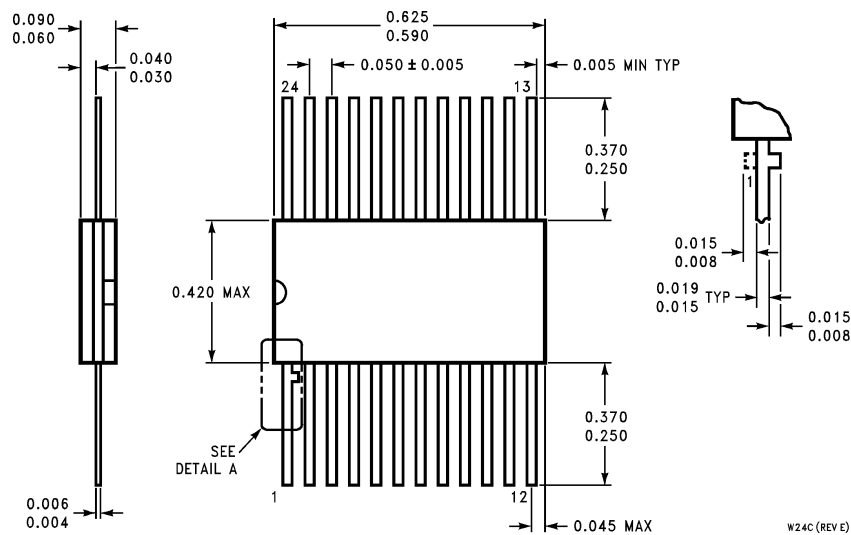
W24C (REV E)

24 Lead Cerpack
Package Number W24C

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
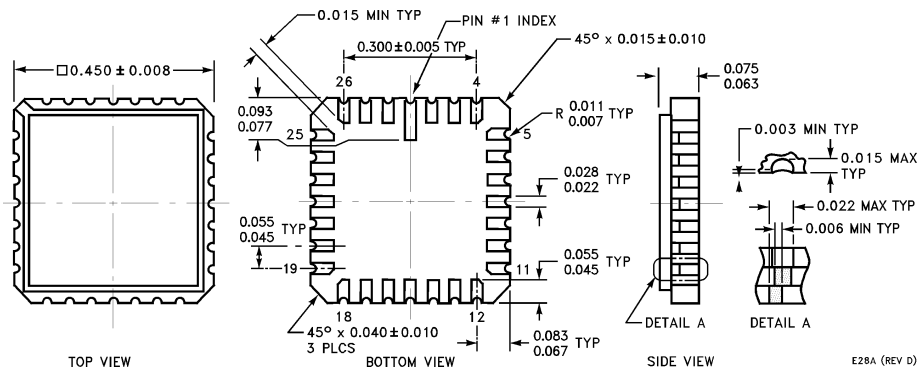
28 Lead Ceramic Leadless Chip Carrier
Package Number E28A

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