National Semiconductor

August 1998

54AC646
Octal Transceiver/Register with TRI-STATE® Outputs

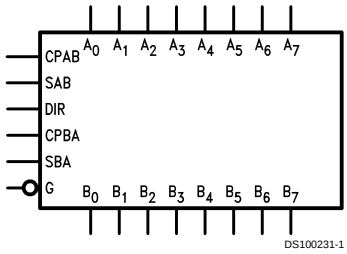
General Description

The 'AC646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in *Figures 1, 2, 3, 4*.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- TRI-STATE outputs
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- 'ACT646 has TTL compatible inputs
- Standard Microcircuit Drawing (SMD)
  — 'AC646: 5962-89682

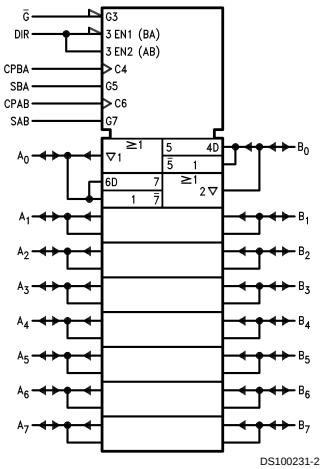
Logic Symbols



DS100231-1

Pin Names	Description
A_0–A_7	Data Register A Inputs
	Data Register A Outputs
B_0–B_7	Data Register B Inputs
	Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

IEEE/IEC



DS100231-2

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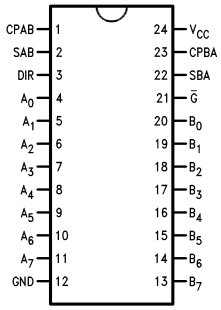
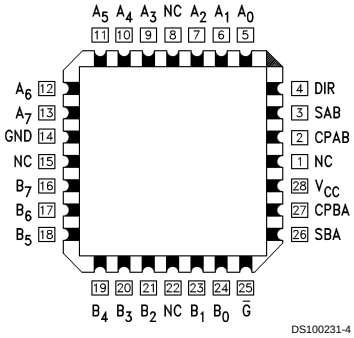
Connection Diagrams

Pin Assignment for DIP and Flatpak



DS100231-3

Pin Assignment for LCC



DS100231-4

Real Time Transfer A-Bus to B-Bus

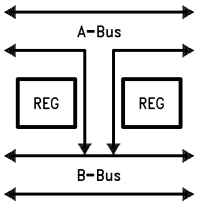


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FIGURE 1.

Real Time Transfer B-Bus to A-Bus

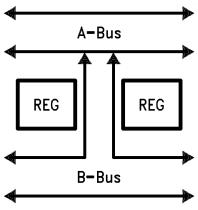

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FIGURE 2.

Storage from Bus to Register

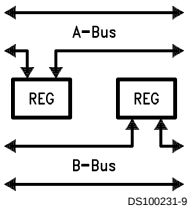

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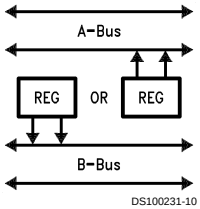
FIGURE 3.

Transfer from Register to Bus



DS100231-10

FIGURE 4.

Function Table

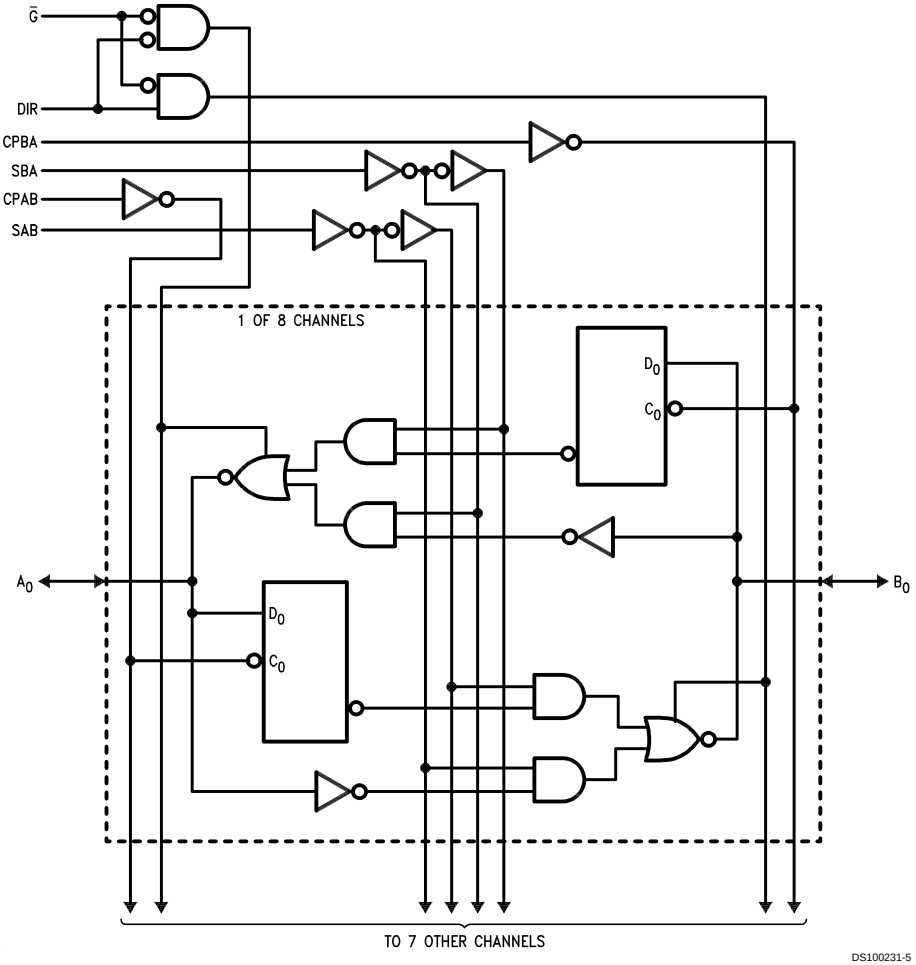
Inputs						Data I/O (Note 1)		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X			Isolation
H	X	⌐	X	X	X	Input	Input	Clock A_n Data into A Register
H	X	X	⌐	X	X			Clock B_n Data into B Register
L	H	X	X	L	X			A_n to B_n — Real Time (Transparent Mode)
L	H	⌐	X	L	X	Input	Output	Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	⌐	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L			B_n to A_n — Real Time (Transparent Mode)
L	L	X	⌐	X	L	Output	Input	Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	⌐	X	H			Clock B_n Data into B Register and Output to A_n

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

⌐ = LOW-to-HIGH Transition

Note 1: The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

Logic Diagram



DS100231-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC	−55˚C to +125˚C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	I_{OUT} = −50 µA
		4.5	4.4		
		5.5	5.4		
					(Note 3) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4	V	I_{OH} = −12 mA
		4.5	3.7		I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	I_{OUT} = 50 µA
		4.5	0.1		
		5.5	0.1		
					(Note 3) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50	V	I_{OH} = 12 mA
		4.5	0.50		I_{OL} = 24 mA
		5.5	0.50		I_{OH} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{OLD}	Minimum Dynamic Output Current (Note 4)	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	5.5	160.0	µA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	5.5	±10.0	µA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 6)	54AC T_A = −55°C to +125°C C_L = 50 pF Min	54AC Max	Units	Fig. No.
t_{PLH}	Propagation Delay	3.3	1.0	20.0	ns	
	Clock to Bus	5.0	1.5	14.0		
t_{PHL}	Propagation Delay	3.3	1.0	17.5	ns	
	Clock to Bus	5.0	1.5	12.0		
t_{PLH}	Propagation Delay	3.3	1.0	15.0	ns	
	Bus to Bus	5.0	1.5	10.0		
t_{PHL}	Propagation Delay	3.3	1.0	14.5	ns	
	Bus to Bus	5.0	1.5	9.5		
t_{PLH}	Propagation Delay	3.3	1.0	17.0		
	SBA or SAB to A_n or B_n	5.0	1.5	12.0	ns	
	(w/ A_n or B_n HIGH or LOW)					
t_{PHL}	Propagation Delay	3.3	1.0	17.0		
	SBA or SAB to A_n or B_n	5.0	1.5	12.0	ns	
	(w/ A_n or B_n HIGH or LOW)					
t_{PZH}	Enable Time	3.3	1.0	13.0	ns	
	$\overline{G}$ to A_n or B_n	5.0	1.5	9.5		
t_{PZL}	Enable Time	3.3	1.0	15.5	ns	
	$\overline{G}$ to A_n or B_n	5.0	1.5	11.0		
t_{PHZ}	Disable Time	3.3	1.0	14.0	ns	
	$\overline{G}$ to A_n or B_n	5.0	1.5	11.0		
t_{PLZ}	Disable Time	3.3	1.0	13.5	ns	
	$\overline{G}$ to A_n or B_n	5.0	1.5	11.0		
t_{PZH}	Enable Time	3.3	1.0	14.5	ns	
	DIR to A_n or B_n	5.0	1.5	10.5		
t_{PZL}	Enable Time	3.3	1.0	16.0	ns	
	DIR to A_n or B_n	5.0	1.5	12.5		
t_{PHZ}	Disable Time	3.3	1.0	14.5	ns	
	DIR to A_n or B_n	5.0	1.5	12.0		

AC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V) (Note 6)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
t_{PLZ}	Disable Time	3.3	1.0	16.5	ns	
	DIR to A_n or B_n	5.0	1.5	12.0		

Note 6: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

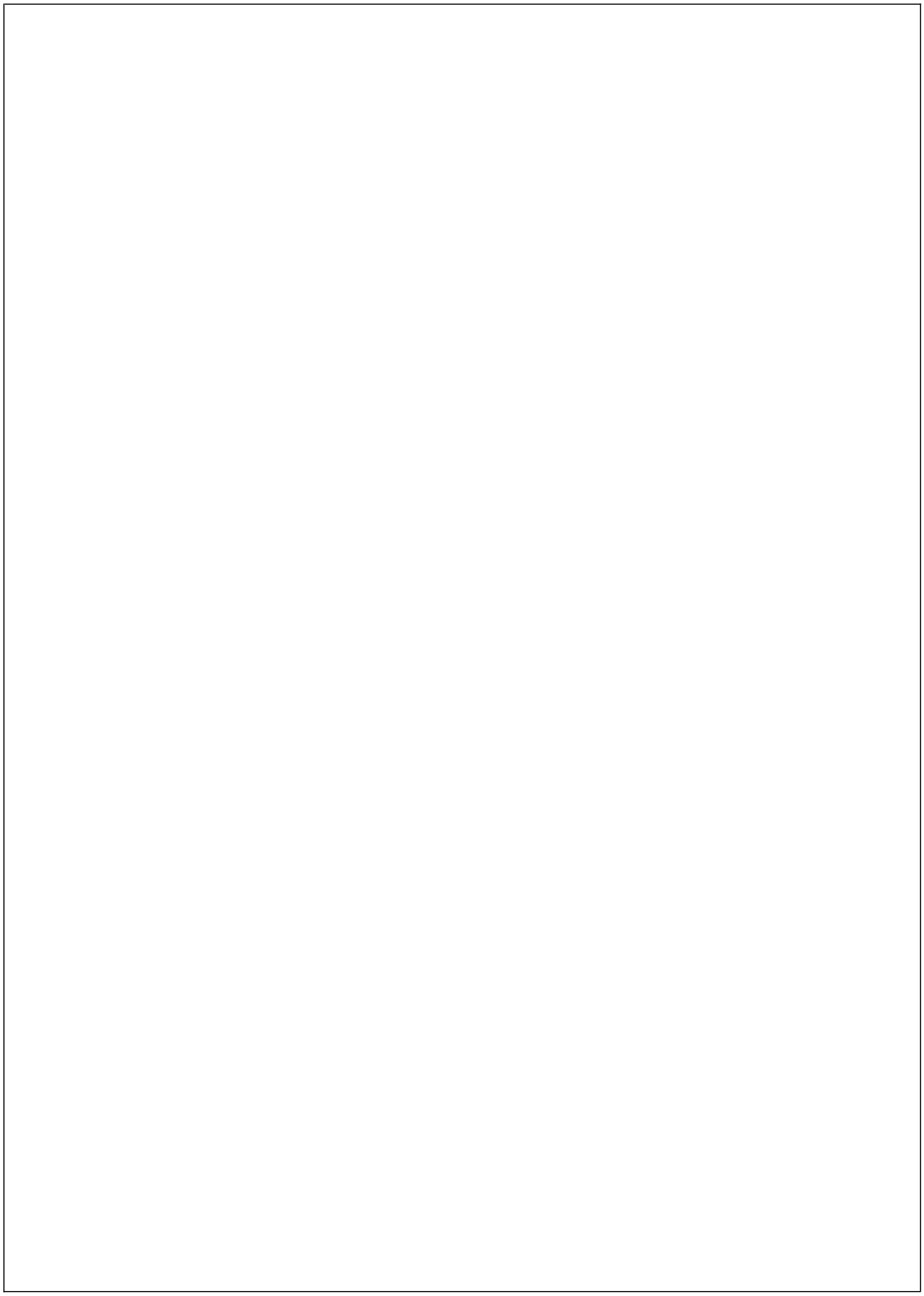
AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 7)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW	3.3	6.0	ns	
	Bus to Clock	5.0	4.5		
t_h	Hold Time, HIGH or LOW	3.3	1.5	ns	
	Bus to Clock	5.0	2.0		
t_w	Clock Pulse Width	3.3	5.0	ns	
	HIGH or LOW	5.0	5.0		

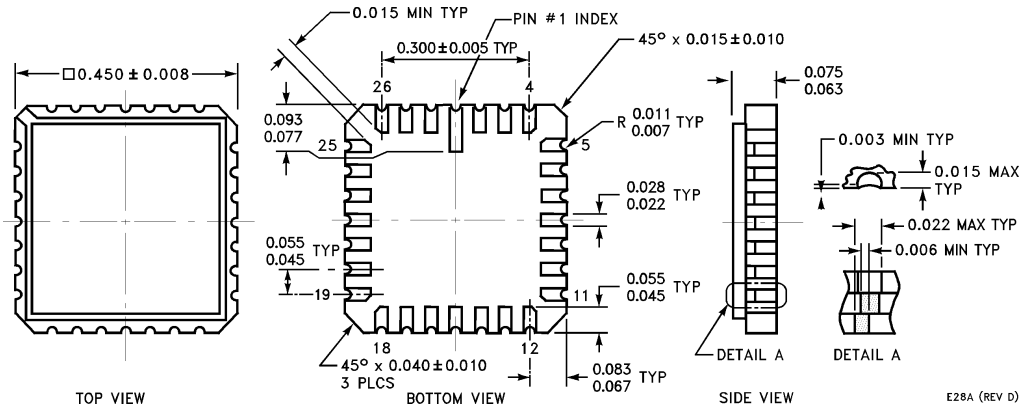
Note 7: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

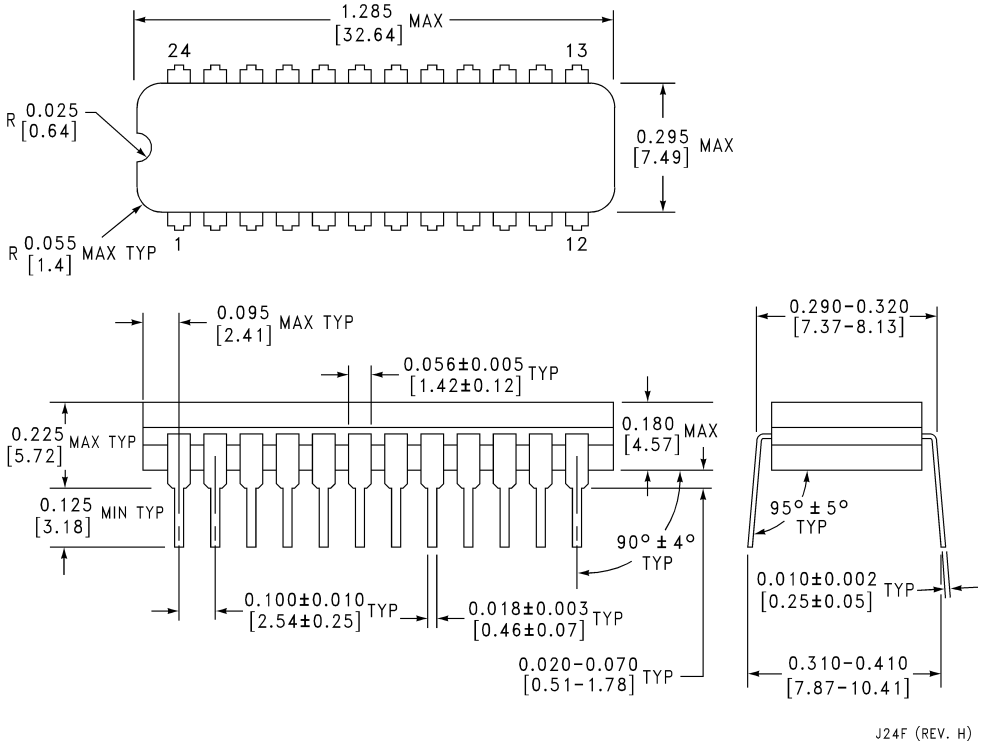
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
$C_{I/O}$	Input/Output Capacitance	15.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	60.0	pF	V_{CC} = 5.0V



Physical Dimensions inches (millimeters) unless otherwise noted

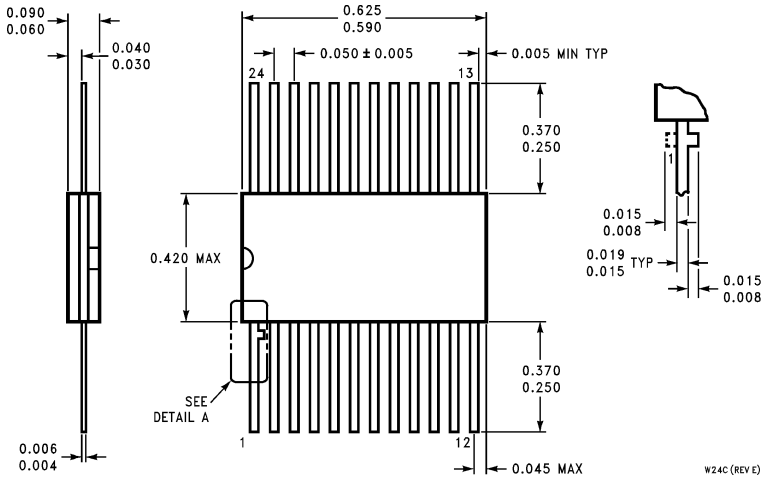


28-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E28A



24-Lead Slim (0.300" Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Ceramic Flatpak (F)
NS Package Number W24C

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