National Semiconductor

August 1998

54ABT543
Octal Registered Transceiver with TRI-STATE® Outputs

General Description

The 'ABT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

Features

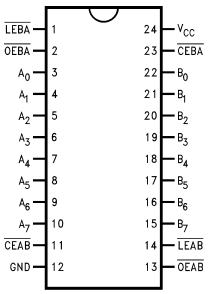
- Back-to-back registers for storage
- Bidirectional data path
- A and B outputs have current sourcing capability of 24 mA and current sinking capability of 48 mA
- Separate controls for data flow in each direction
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Standard Military Drawing (SMD) 5962-9231401

Ordering Code:

Military	Package Number	Package Description
54ABT543J-QML	J24A	24-Lead Ceramic Dual-In-Line
54ABT543W-QML	W24C	24-Lead Cerpack
54ABT543E-QML	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagrams

Pin Assignment for DIP and Flatpak



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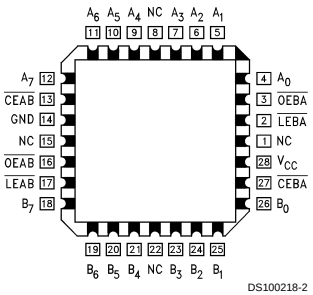
Pin Assignment for LCC



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Pin Descriptions

Pin Names	Description
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable Inputs
$\overline{LEAB}$, $\overline{LEBA}$	Latch Enable Inputs
$\overline{CEAB}$, $\overline{CEBA}$	Chip Enable Inputs
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Functional Description

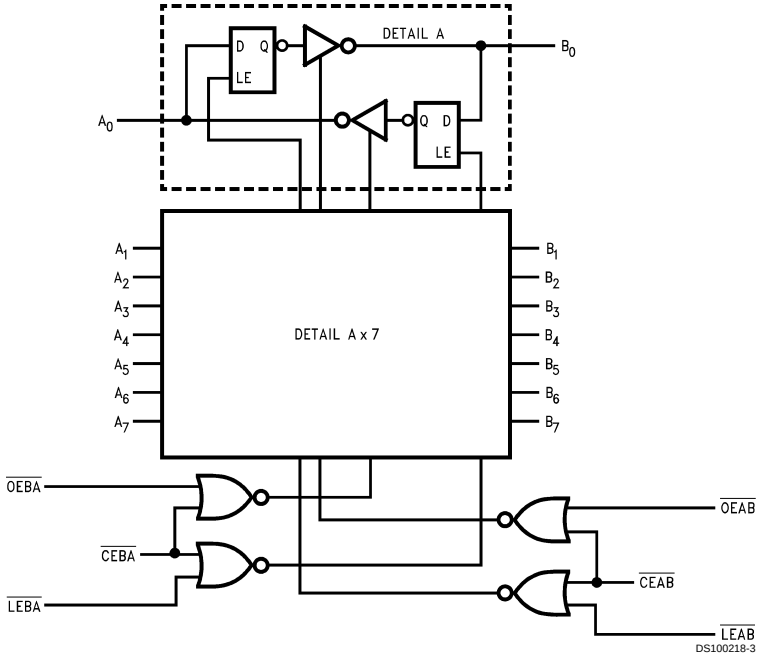
The 'ABT543 contains two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable ($\overline{CEAB}$) input must be low in order to enter data from the A port or take data from the B port as indicated in the Data I/O Control Table. With $\overline{CEAB}$ low, a low signal on ($\overline{LEAB}$) input makes the A to B latches transparent; a subsequent low to high transition of the $\overline{LEAB}$ line puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Logic Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT543 Min	ABT543 Typ	ABT543 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	54ABT	2.5					I_{OH} = −3 mA, (A_n, B_n)
		54ABT	2.0			V	Min	I_{OH} = −24 mA, (A_n, B_n)
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA, (A_n, B_n)
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current				5	µA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 3) V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test				7	µA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				100	µA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current				−5	µA	Max	V_{IN} = 0.5V (Non-I/O Pins)(Note 3) V_{IN} = 0.0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current				50	µA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEAB}$ or $\overline{CEAB}$ = 2V
I_{IL} + I_{OZL}	Output Leakage Current				−50	µA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEAB}$ or $\overline{CEAB}$ = 2V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test				100	µA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCLH}	Power Supply Current				50	µA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	µA	Max	Outputs TRI-STATE All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input				2.5	mA	Max	V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC}	No Load						Outputs Open, $\overline{CEAB}$

DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT543			Units	V_{CC}	Conditions
		Min	Typ	Max			
	(Note 3)			0.18	mA/MHz	Max	and $\overline{OEAB}$ = GND, $\overline{CEBA}$ = V_{CC}, One Bit Toggling, 50% Duty Cycle, (Note 4)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Note 3: Guaranteed but not tested.

Note 4: For 8-bit toggling. $I_{CCD} < 1.4$ mA/MHz.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		1.1	V	5.0	T_A = 25˚C (Note 5)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}		-0.45	V	5.0	T_A = 25˚C(Note 5)

Note 5: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW.

AC Electrical Characteristics

Symbol	Parameter	54ABT T_A = −55˚C to +125˚C V_{CC} = 4.5V−5.5V C_L = 50 pF		Units	Fig. No.
		Min	Max		
t_{PLH}	Propagation Delay	1.6	6.4	ns	*Figure 4*
t_{PHL}	A_n to B_n or B_n to A_n	1.6	6.2		
t_{PLH}	Propagation Delay				
t_{PHL}	$\overline{LEAB}$ to B_n, $\overline{LEBA}$ to A_n	1.6	6.6	ns	*Figure 4*
	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.6	6.4		
t_{PZH}	Enable Time				
t_{PZL}	$\overline{LEAB}$ to B_n, $\overline{LEBA}$ to A_n	1.3	6.4	ns	*Figure 6*
	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.8	7.4		
t_{PHZ}	Disable Time	2.0	7.2	ns	*Figure 6*
t_{PLZ}	$\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.5	7.0		

AC Operating Requirements

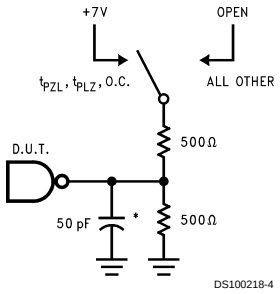
Symbol	Parameter	54ABT $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Max		
$t_S(H)$	Setup Time, HIGH or LOW	3.5		ns	*Figure 7*
$t_S(L)$	A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	3.0			
$t_H(H)$	Hold Time, HIGH or LOW	2.0		ns	*Figure 7*
$t_H(L)$	A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	2.0			
$t_S(H)$	Setup Time, HIGH or LOW	3.3		ns	*Figure 7*
$t_S(L)$	A_n or B_n to $\overline{CEAB}$ or $\overline{CEBA}$	2.5			
$t_H(H)$	Hold Time, HIGH or LOW	2.0		ns	*Figure 7*
$t_H(L)$	A_n or B_n to $\overline{CEAB}$ or $\overline{CEBA}$	2.0			
$t_W(L)$	Pulse Width, LOW	3.5		ns	*Figure 5*

Capacitance

Symbol	Parameter	Typ	Units	Conditions: $T_A = 25^\circ C$
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 0V (non I/O pins)
$C_{I/O}$(Note 6)	Output Capacitance	11.0	pF	V_{CC} = 5.0V (A_n, B_n)

Note 6: $C_{I/O}$ is measured at frequency, f = 1 MHz, PER MIL-STD-883, METHOD 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

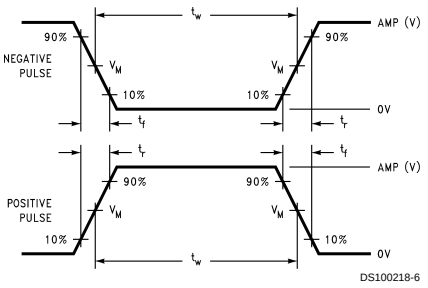


FIGURE 2. V_M = 1.5V Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Loading (Continued)

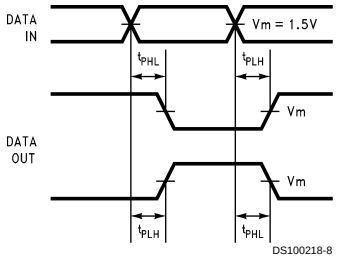


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

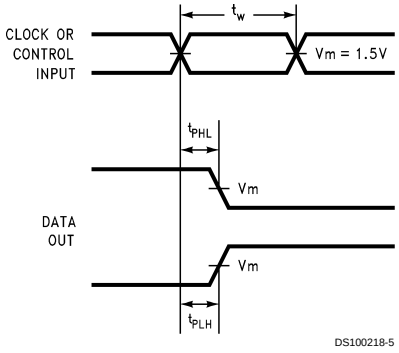


FIGURE 5. Propagation Delay, Pulse Width Waveforms

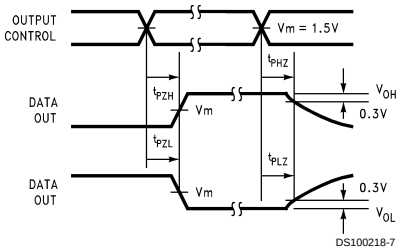


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

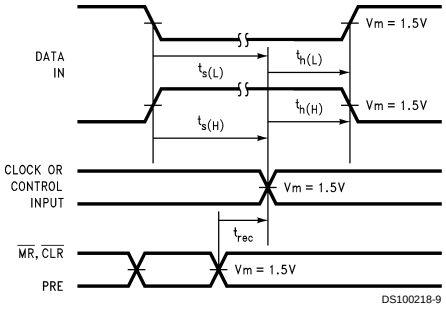
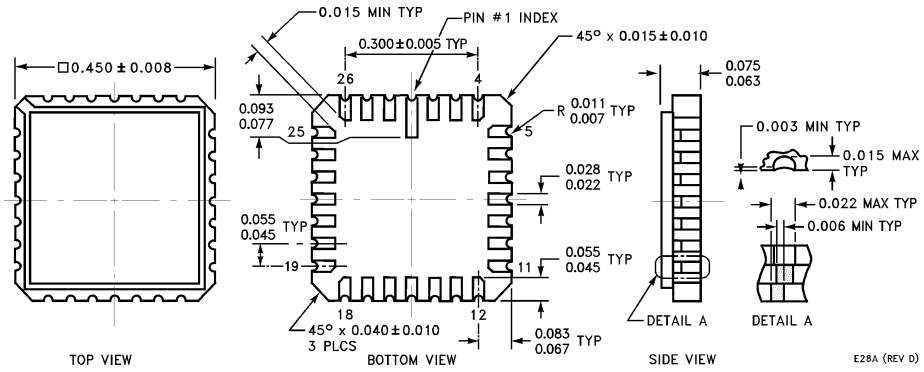
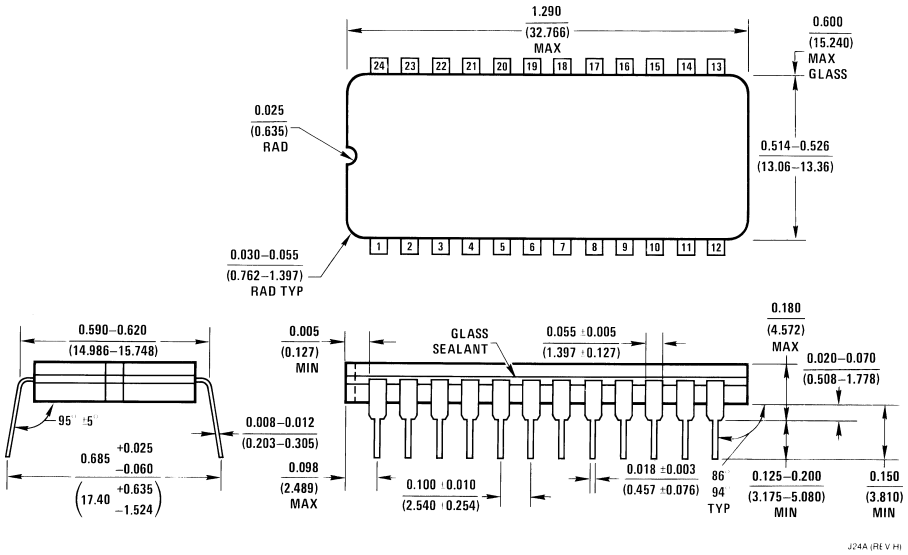


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

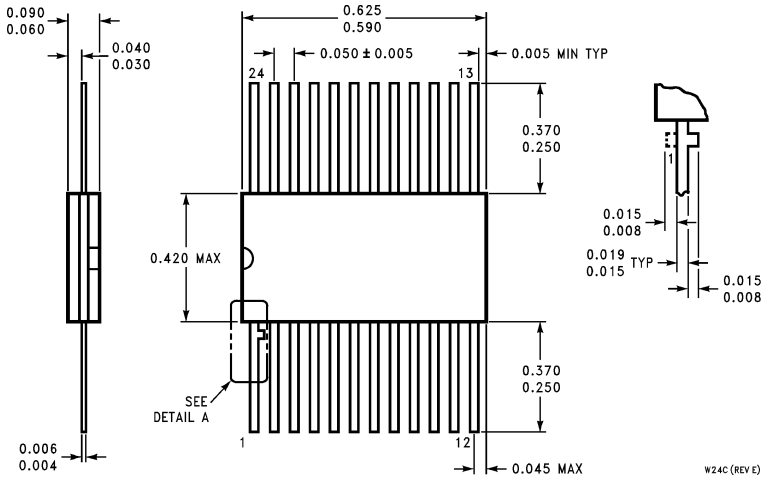


28-Lead Ceramic Leadless Chip Carrier (L)
Order Number 54ABT543E-QML
NS Package Number E28A



24-Lead Ceramic Dual-In-Line Package
Order Number 54ABT543J-QML
NS Package Number J24A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Ceramic Flatpak Package (F)
Order Number 54ABT543W-QML
NS Package Number W24C

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179