National Semiconductor

July 1998

54ABT377
Octal D-Type Flip-Flop with Clock Enable

General Description

The 'ABT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

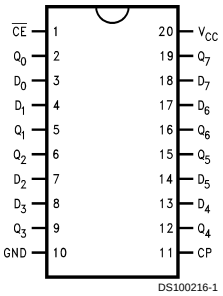
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- See 'ABT273 for master reset version
- See 'ABT373 for transparent latch version
- See 'ABT374 for TRI-STATE® version
- Output sink capability of 48 mA, source capability of 24 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time less than enable time to avoid bus contention
- Standard Microcircuit Drawing (SMD) 5962-9314801

Ordering Code:

Military	Package Number	Package Description
54ABT377J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT377W-QML	W20A	20-Lead Cerpack
54ABT377E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

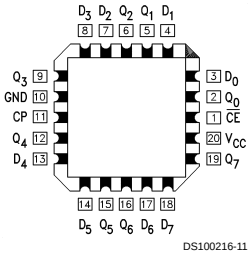
Connection Diagram

Pin Assignment for DIP and Cerpack



DS100216-1

Pin Assignment for LCC



DS100216-11

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

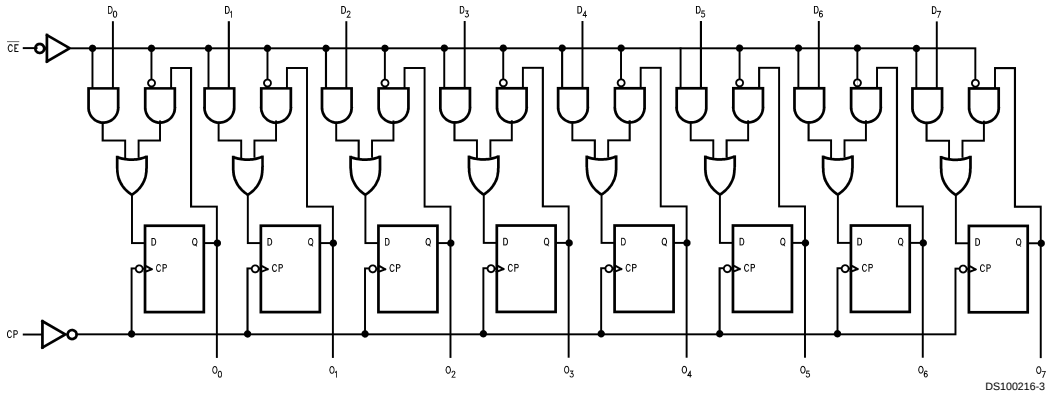
Truth Table

Mode Select-Function Table

Operating Mode	Inputs			Output
	CP	$\overline{CE}$	D_n	Q_n
Load “1”		I	h	H
Load “0”		I	I	L
Hold		h	X	No Change
(Do Nothing)	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
I = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
= LOW-to-HIGH Clock Transition

Logic Diagram



DS100216-3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to +4.75V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	Twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
(Across Comm Operating Range)	
Over Voltage Latchup	V_{CC} + 4.5V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT377 Min	ABT377 Typ	ABT377 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0					I_{OH} = −24 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V (Note 4)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V (Note 4)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA
								All Other Pins Grounded
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCT}	Maximum I_{CC}/Input	Outputs Enabled						V_I = V_{CC} − 2.1V
					1.5	mA	Max	Data Input V_I = V_{CC} − 2.1V
								All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC}	No Load			0.3	mA/ MHz	Max	Outputs Open (Note 3)
								One bit Toggling, 50% Duty Cycle

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Note 3: For 8 bits toggling, I_{CCD} < 0.5 mA/MHz.

Note 4: Guaranteed but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units
		$T_A = -55^\circ C$ to $+125^\circ C$ $V_{CC} = 4.5V$ to $5.5V$ $C_L = 50$ pF		
		Min	Max	
f_{max}	Max Clock Frequency	150		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	2.2 2.8	6.0 6.8	ns

AC Operating Requirements

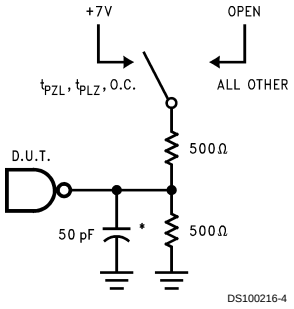
Symbol	Parameter	54ABT		Units
		$T_A = -55^\circ C$ to $+125^\circ C$ $V_{CC} = 4.5V$ to $5.5V$ $C_L = 50$ pF		
		Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	1.8 1.8		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CE}$ to CP	3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CE}$ to CP	1.0 1.0		ns
$t_w(H)$ $t_w(L)$	Pulse Width, CP, HIGH or LOW	3.3 3.3		ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0V$, $T_A = 25^\circ C$
C_{OUT} (Note 5)	Output Capacitance	9	pF	$V_{CC} = 5.0V$

Note 5: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

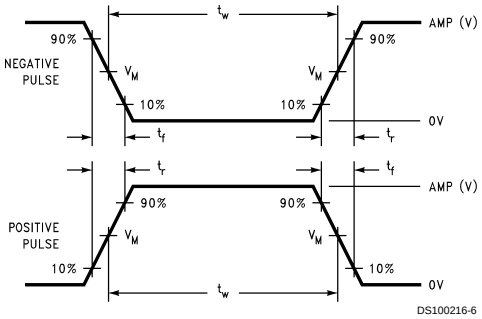


FIGURE 2. V_M = 1.5V

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

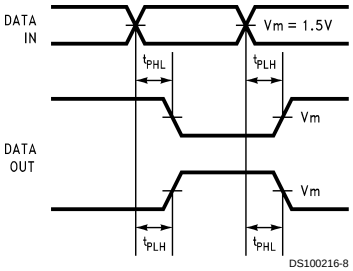


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

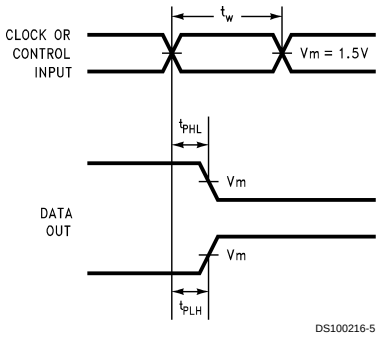


FIGURE 5. Propagation Delay, Pulse Width Waveforms

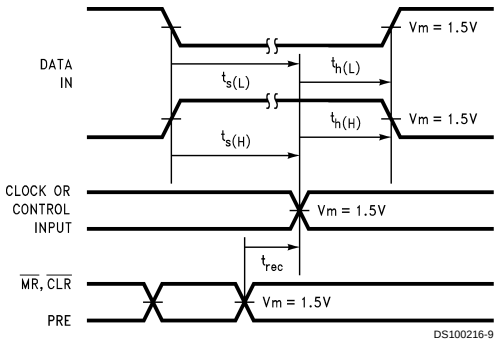
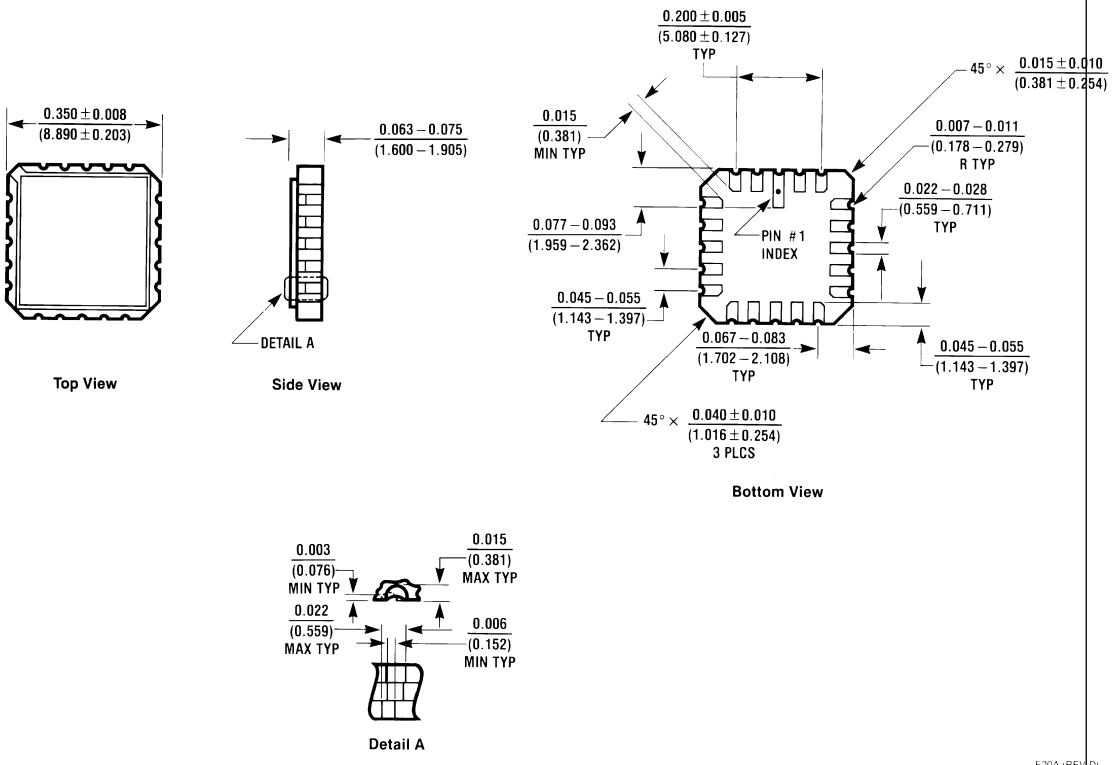


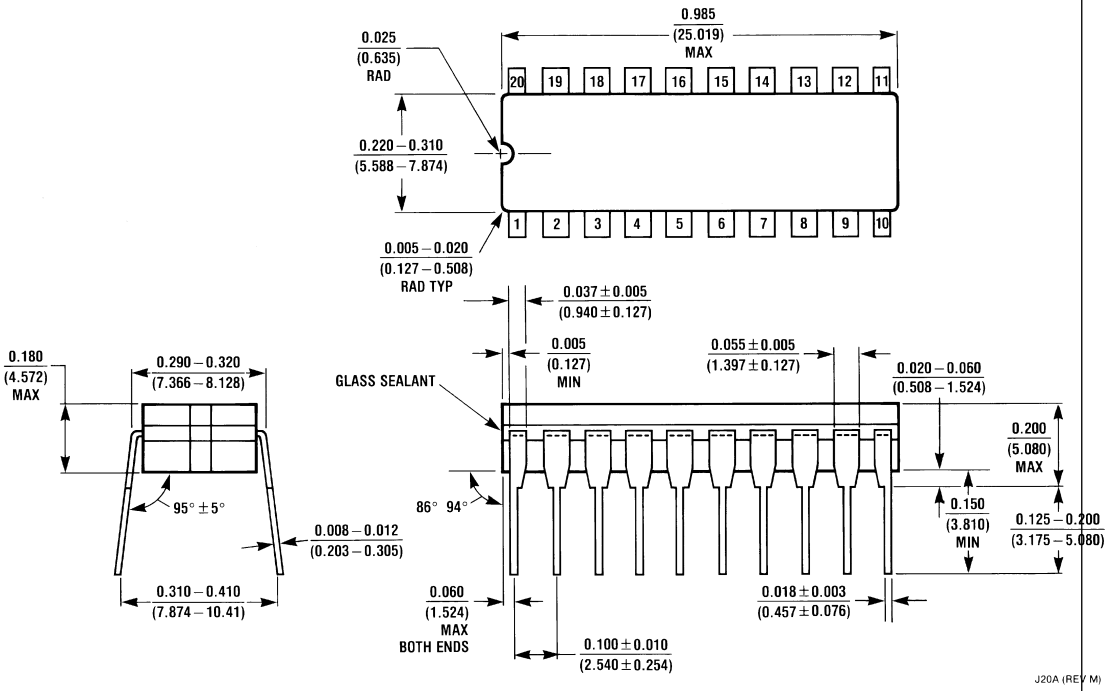
FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

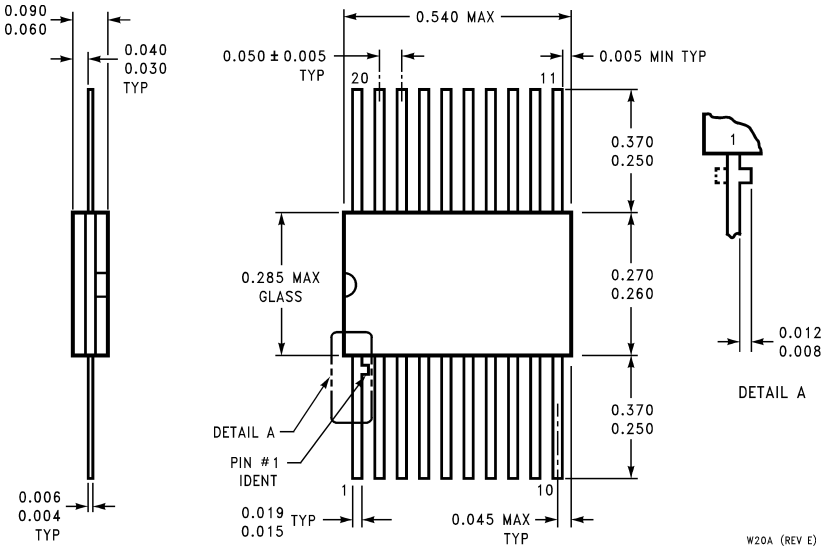


20-Lead Ceramic Chip Carrier
NS Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Dual-In-Line Package
NS Package Number J20A



20-Lead Ceramic Flatpack
NS Package Number W20A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179