July 1998



54ABT273 Octal D-Type Flip-Flop

General Description

The 'ABT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset $(\overline{\text{MR}})$ inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{\text{MR}}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

- Buffered common clock
- Buffered, asynchronous Master Reset
- See 'ABT377 for clock enable version
- See 'ABT373 for transparent latch version
- See 'ABT374 for TRI-STATE® version
- Output sink capability of 48 mA, source capability of 24 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time less than enable time to avoid bus contention
- Standard Microcircuit Drawing (SMD) 5962-9321701

Features

■ Eight edge-triggered D flip-flops

Ordering Code

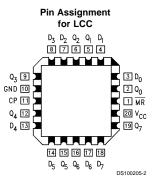
Military	Package Number	Package Description	
54ABT273J-QML	J20A	20-Lead Ceramic Dual-In-Line	
54ABT273W-QML	W20A	20-Lead Cerpack	
54ABT273E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C	

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Connection Diagrams

Pin Assignment for DIP and Flatpack





Pin	Description		
Names			
D ₀ -D ₇	Data Inputs		
MR	Master Reset		
	(Active LOW)		
CP	Clock Pulse Input		
	(Active Rising Edge)		
$Q_0 - Q_7$	Data Outputs		

Truth Table

Mode Select-Function Table

Operating Mode	Inputs			Output
	MR	CP	D _n	Q _n
Reset (Clear)	L	Х	Х	L
Load "1"	Н	~	h	Н
Load "0"	Н	~	I	L

H = HIGH Voltage Level steady state

h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition

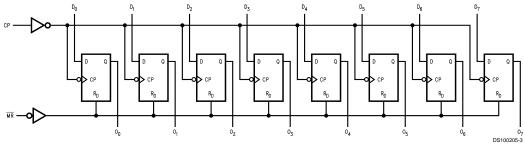
L = LOW Voltage Level steady state

I = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition

X = Immaterial

∠ = LOW-to-HIGH clock transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature -65°C to +150°C

Ambient Temperature under Bias -55°C to +125°C

Junction Temperature under Bias

Ceramic -55°C to +175°C

 $\ensuremath{\text{V}_{\text{CC}}}$ Pin Potential to

Voltage Applied to Any Output

in the Disabled or

Power-Off State -0.5 V to +4.75 V in the HIGH State $-0.5 \text{V to } \text{V}_{\text{CC}}$

Current Applied to Output

in LOW State (Max) $\qquad \qquad \text{twice the rated I}_{\text{OL}} \ (\text{mA})$

DC Latchup Source Current -500 mA (Across Comm Operating Range)

Over Voltage Latchup V_{CC} + 4.5V

Recommended Operating Conditions

Free Air Ambient Temperature

Military -55°C to +125°C

Supply Voltage

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these

conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		ABT273		Units	V _{cc}	Conditions	
		Min	Тур	Max				
V _{IH}	Input HIGH Voltage				V		Recognized HIGH Signal	
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal	
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage 54ABT	2.5					I _{OH} = -3 mA	
	54ABT	2.0			V	Min	I _{OH} = -24 mA	
V _{OL}	Output LOW Voltage 54ABT			0.55	V	Min	I _{OL} = 48 mA	
I _{IH}	Input HIGH Current			5	μΑ	Max	V _{IN} = 2.7V (Note 4)	
				5			V _{IN} = V _{CC}	
I _{BVI}	Input HIGH Current			7	μA	Max	V _{IN} = 7.0V	
	Breakdown Test							
I _{IL}	Input LOW Current			-5	μA	Max	V _{IN} = 0.5V (Note 4)	
				-5			$V_{IN} = 0.0V$	
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA	
							All Other Pins Grounded	
Ios	Output Short-Circuit Current	-100		-275	mA	Max	V _{OUT} = 0.0V	
I _{CEX}	Output High Leakage Current			50	μA	Max	V _{OUT} = V _{CC}	
I _{CCH}	Power Supply Current			50	μA	Max	All Outputs HIGH	
I _{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW	
I _{CCT}	Maximum I _{CC} /Input Outputs Enabled						$V_I = V_{CC} - 2.1V$	
				1.5	mA	Max	Data Input V _I = V _{CC} - 2.1V	
							All Others at V _{CC} or GND	
I _{CCD}	Dynamic I _{CC} No Load			0.3	mA/	Max	Outputs Open (Note 3)	
					MHz		One Bit Toggling, 50% Duty Cycle	

Note 3: For 8 bits toggling, I_{CCD} < 0.5 mA/MHz.

Note 4: Guaranteed but not tested.

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Symbol	Parameter	54/ T _A = -55°C	Units	
		V _{CC} = 4.5 C _L =		
		Min	Max	
f _{max}	Max Clock	150		MHz
	Frequency			
t _{PLH}	Propagation Delay	1.0	7.0	ns
t _{PHL}	CP to O _n	1.0	7.5	
t _{PHL}	Propagation Delay MR to O _n	1.0	8.2	ns

AC Operating Requirements

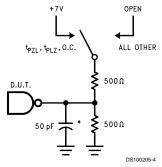
Symbol	Parameter	54ABT T _A = -55°C to +125°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		Units
		Min	Max	
t _s (H)	Setup Time, HIGH	2.0		ns
t _s (L)	or LOW D _n to CP	2.5		
t _h (H)	Hold Time, HIGH	1.4		ns
t _h (L)	or LOW D _n to CP	1.4		
t _w (H)	Pulse Width, CP,	3.3		ns
$t_w(L)$	HIGH or LOW	3.3		
t _w (L)	Master Reset Pulse	3.3		ns
	Width, LOW			
t _{REC}	Recovery Time	2.0		ns
	MR to CP			

Capacitance

Symbol	Parameter	Тур	Units	Conditions T _A = 25°C
C _{IN}	Input Capacitance	5	pF	V _{CC} = 0V
C _{OUT} (Note 5)	Output Capacitance	9	pF	V _{CC} = 5.0V

Note 5: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-833B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

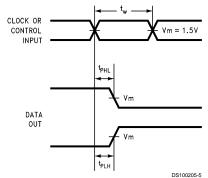


FIGURE 2. Propagation Delay, Pulse Width Waveforms

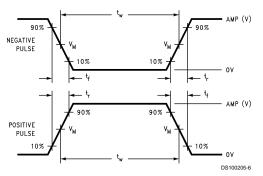


FIGURE 3. V_M = 1.5V Input Pulse Requirements

Amplitude	Rep. Rate	t _w	t _r	t _f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 4. Test Input Signal Requirements

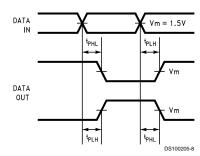


FIGURE 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

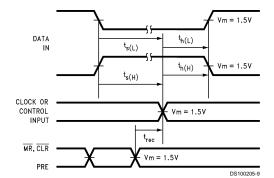
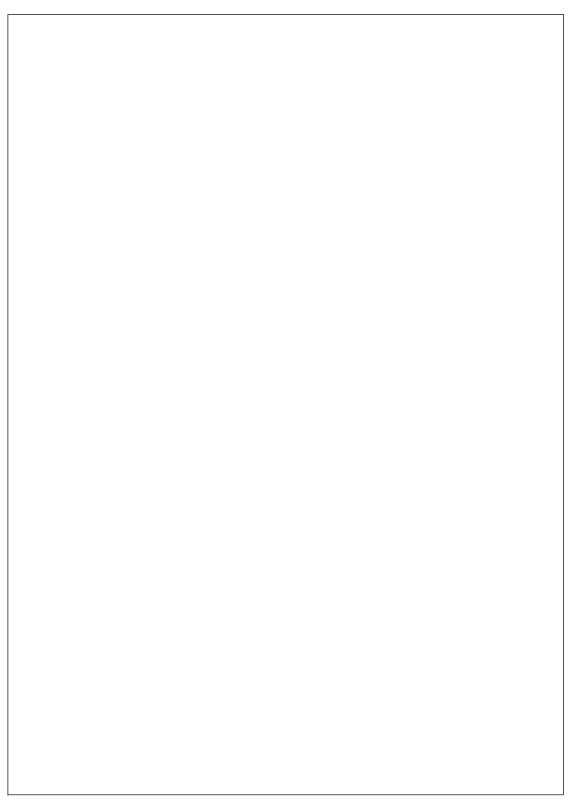
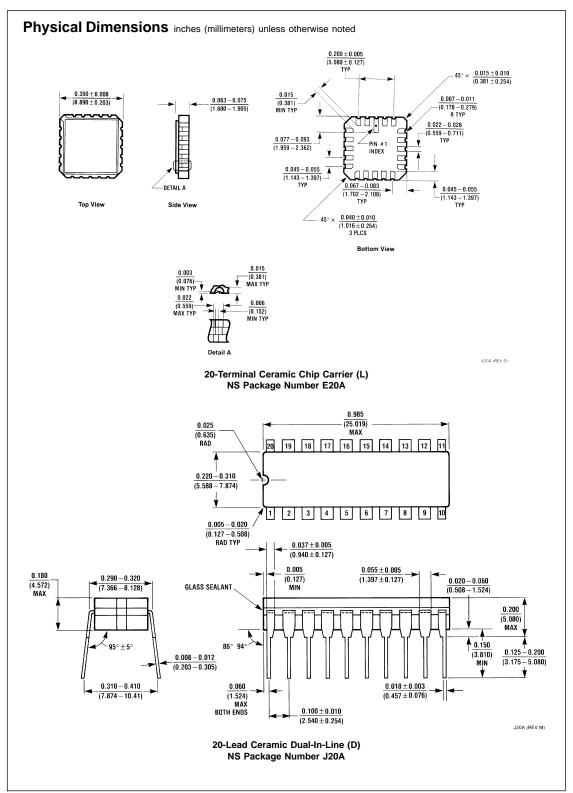
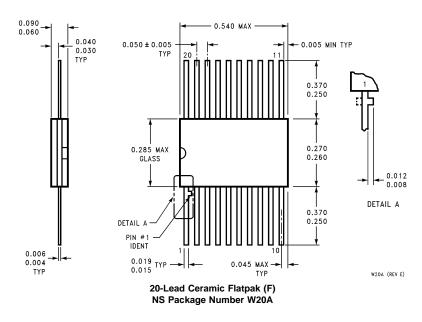


FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms





Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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