Packaging/CSP

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Substrate CSP

Top View



- 68% Board Area Reduction (vs. TSSOP 20)
 - Only 25% larger than die
- Standard SMT Process
- JEDEC Registration:
 - 3 Registrations Completed (16/24/28L)
 Reg # M0-208
- First Package: 24 lead,0.5 mm pitch
 - Delivering 150K/mo from SC pilot line
 - Availability
 - Customer Samples : CSP16, CSP28...
 - Pre -production CSP24
 - 8,16,20,24,28,48,64,81,100,144 + ..

CSP Packaging Acceptance

- Products available: LMX2330L/31L/32L/36L, LMX2324
- All new products will be available in CSP
- Demand is growing with many design wins already recorded
- Largest CDMA manufacture in the world is purchasing product in Chip Scale
- Japanese manufacturers are driving the requirement for Chip Scale Packaging in the market

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CSP Packaging

- Samples available(now) for LMX2330L/31L/32L/36L, LMX2324
- Package suffix "SLB" (LMX2330LSLBX)
- Package option for future products
 - Available on existing products based on demand
- Qualification in process (CSP24)
 - Expected completion mid November
 - CSP16/28 to be qual'd by extension (similarity)







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2nd Generation - Dual Low Power PLLs



Substrate CSP General Q&A

- What is the substrate material?
 - BT Resin with Taiyo PSR4000-AUS5 solder mask
- What is the pad material? Plating thickness?
 - 15 um Cu, 5 um Ni and .5 um Au plating.
- How thick is the resist around the pad?
 - 45 +/- 15 um
- What is the package size tolerance?
 - Pad to package edge should be within +/- .05mm
 - Package body size tolerance is +/- .1 mm
- Package flatness? (Required +/- 0.05mm)
 - No problem with +/- .05 mm
- Suggested pad size and soldering on PCB
 - Recommend using .5 mm x .3 mm pad size for PCB with metal pad defined structure and 6 mils stencil for solder screen printing.

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Substrate CSP General Q&A (continued)

- Should the PCB mother board be designed with tented via hole around the CSP solder pad?
 - Yes. It is preferred that the solder pad via holes for the mother board be tented it they are close (eg< 1mm) to the solder pads. However, if the via holes are far away (eg.> 1mm), then tenting is probably not necessary.
- What is the suggested reflow conditions?
 - Same as standard IR reflow profile used by all SMT components.
 - Ramp up: Dwell Time > 183C: Solder Temp: Dwell Time @ Max Temp: Ramp Down:

2 deg.C/sec 75 sec 215 C (max. @ 240 C) 5 sec 2 deg.C/sec

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Substrate CSP General Q&A

(continued)

- What desoldering tool is available for CSP?
 - The desoldering tool is the same as that used for any package type including TSSOP.
 - The manufacture of the desoldering tool is PRB LINE (Zephyrtronics). The model is DSZT3 SYSTEM. The complete system cost is about \$ 2000.
 - Contact Person: John F. Dwinell Jr. (Sales Engineer)
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