LMX3162 Evaluation Notes

National Semiconductor, Inc.
Wireless Communications Group

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General Description

The LMX3162 Evaluation Kit consists of the LMX3162 Evaluation Board, CodeLoader 1.32 Software, MICROWIRE™ Emulation Cable and datasheets of the LMX3162 and the VCO. The LMX3162 Evaluation Board simplifies the evaluation of the LMX3162 Single Chip Radio Transceiver. The board enables all performance measurements with no additional support circuitry.

The LMX3162 Evaluation Board is an implementation of the schematic shown in Figure 1 and Figure 22. The board consists of the LMX3162, a modular RF VCO, a ceramic RF filter, a discrete LNA, and an IF SAW filter. This board is not intended to be an ISM reference design, rather as a means to demonstrate the general performance and functionality of the LMX3162.

The board has two kinds of interconnections with the external world. SMA flange mount connectors are supplied for the External Reference, External LO Input, Power Supply, RF Input and RF Output. For the convenience of the user, there are provisions to mount SMA connectors for Data Input, RSSI Output, Trigger Output and Threshold.

The other type of connector is a 10-pin header for connection to the Emulation Cable that has been supplied with this kit. The Emulation Cable connects the Evaluation Board to the parallel port of a PC, facilitating the emulation of a MICROWIRE™ Bus connection between the PC and the Evaluation Board. The emulation is done by CodeLoader 1.32 software. For instructions on how to install and use CodeLoader, see reference 2. Since most PC's have a nominal output level of 5volts, resistive dividers for the interfacing the parallel port to the MICROWIRE™ Bus pins of the LMX3162 are included on the Evaluation Board.

An onboard 12-pin jumper header provides ease and flexibility in powering up the various sections of the Evaluation Board and the LMX3162 itself. The user can either drive the entire board from a single power supply, or test separate sections of the Evaluation Board or the LMX3162 in isolation. For example, the user may test a VCO that requires a higher tuning voltage by giving a separate, higher voltage supply to the charge pump section the LMX3162.

The Evaluation Board has been designed to accept RF input signals from 2.4 to 2.5 GHz, with the LO 110.6 MHz below the RF signal. The onboard PLL locks to half the desired LO frequency, and then the doubler onboard the LMX3162 doubles the frequency. For example, to receive a 2.4506 GHz signal, the required LO is 2.4000 GHz, and the onboard PLL locks to 1170 MHz. The PLL uses a phase reference frequency of 500kHz, and has a loop bandwidth of 80 kHz. The choice of the loop bandwidth arose from a need to keep the PLL lock at around 300µS, a requirement typical of some wireless standards. An IF frequency of 110.5 MHz can be used without any significant loss of performance, this greatly simplifies the choice of crystals if round numbered channels are required.

The LMX3162 implements a Limiter Discriminator Demodulator, and can perform incoherent demodulation of all kinds of Frequency Modulation schemes i.e. GFSK, GMSK etc. These schemes are prevalent in standards such as IEEE 802.11, Bluetooth and HomeRF. However, the Evaluation Board has been designed to perform best with a GFSK signal having a deviation of 250kHz, BT=0.5, and a bit rate of 1Mbps. The Quadrature Detector and various filters can be modified to optimize the Evaluation Board for other modulation standards and data rates.

The Evaluation Board achieves a sensitivity of about –93 dBm for a BER of 1e-3, under burst mode open loop conditions. With the use of a lower loss ceramic filter and a higher performing LNA, sensitivity of –96 dBm can be achieved.

Quick Start

The LMX3162 Evaluation Board is fully assembled and factory tested. Follow the instructions below to set up the hardware platform for the measurement of interest.

Recommended Test Equipment

- Spectrum Analyzer, operating frequency range ≥ 3.9 GHz.
- Modulation Domain Analyzer
- DC Power Supply with adjustable voltage outputs
- 10 MHz signal source/generator, high quality TCXO is preferred
- RF Signal Generator, with ability to generate GFSK signals and operating range ≥ 2.5 GHz.
- BER Setup
- Oscilloscope

Connection and Setup

Receive Mode

1. Connect a 3.3-volt supply to the SMA connector marked **Vcc**.
2. Connect the MICROWIRE™ Emulation Cable to the 10-pin header and the parallel port of the PC.
3. Connect a 10 MHz, 0 dBm source to the SMA connector **Osc In.** Typically this can be the reference output of the spectrum analyzer
4. Connect a 2.4506 GHz GFSK source to the SMA connector **RF In.**
5. Program the Evaluation Board using the CodeLoader. The settings of the Main Menu of the CodeLoader are shown in Figure 23. For a description on the usage of the CodeLoader, see the accompanying note on it.
6. Perform the BER Test. The signal on the SMA connector marked **Disc** Out is the raw demodulated signal, with a pedestal of about 1.5 volts. Some signal conditioning may be required to remove this pedestal and convert the signal to levels and form acceptable by the user's BER Setup.

Transmit Mode

1. Repeat Steps 1,2 and 3 as above in the Receive Mode description.
2. Repeat Step 5, except that on the Main Menu of the CodeLoader the check mark is placed on RX_PD instead of being on TX_PD.
3. Connect a Gaussian Low Pass Filtered Baseband Datastream to the SMA connector marked **Mod In**, adjusting its amplitude to get the correct frequency deviation.
4. Connect the SMA connector marked **TX Out** to the Spectrum Analyzer and see the transmitted spectrum.

Note:

1. This is not a reference design, and better design and layout may improve the BER sensitivity. Decoupling is layout sensitive and components may be reduced in many cases.
2. Computer monitors and other lab equipment have been known to cause noise spikes. If you see noise spikes on the signal, try turning off the monitor or other equipment to see if they are cause. Also, noise may be induced onto the Emulation Cable that connects to the parallel port of the computer.
3. Some components in the schematic are shown without values. They are not present on the Evaluation Board, but land patterns for placement are. These extra component pads have been included to allow the user flexibility in customizing the board design as per the required application.

Circuit Description

Block Schematic

The block schematic diagram of the Evaluation Board is shown in Figure 1. As shown in the diagram, the Evaluation Board has been designed to enable separate testing of the Transmit and Receive functions of the LMX3162. The Evaluation Board can be logically subdivided into three distinct sections: The PLL and the MICROWIRE™, the Transmit and the Receive sections. The functioning of each will be explained below.

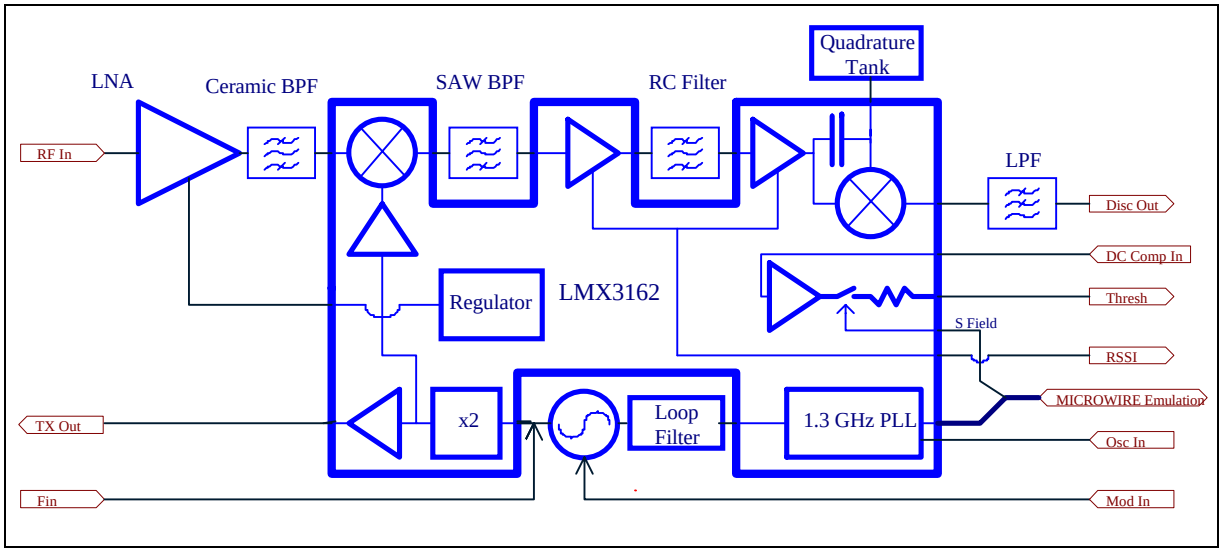

Figure 1: Block Schematic of the Evaluation Board

Operation of the PLL and the MICROWIRE™

The LMX3162 has an onboard 1.3 GHz PLL, which is used to control a VCO external to the LMX3162. The VCO is mounted on the Evaluation Board. The LMX3162 has been designed to operate in TDMA Systems. This means that data is transmitted and received by the device in bursts, and the two operations are mutually exclusive. The time length of the burst is determined by the protocol under which the LMX3162 transceiver is designed to work. A typical value employed by popular protocols in the 2.4 GHz ISM Band would be about 400 µS.

To improve performance and reduce the cost of implementation, the LMX3162 has been designed to transmit and receive data in the Open Loop Mode. In this scheme, the onboard PLL is first locked to the desired frequency and then shut down during the short duration that data transmission or reception takes place. During the burst, the unlocked VCO starts to drift. However, the amount of frequency drift is usually a negligible fraction of the requirements mandated by the various ISM Band Protocols. This is due to the excellent leakage characteristics of National's PLLs, which help retain charge on the Loop Filter capacitors. Typical requirements are < 50 kHz of frequency offset including drift during the burst. As shown in **Figure 13**, the measured drift on the Evaluation Board is less than 500 Hz/ms at T_{amb}=25°C.

The PLL is locked to half the frequency desired for transmission or reception, and is then doubled by the internal frequency doubler. This gives a number of benefits. The most important one is that when the Power Amplifier (PA) is switched on it may radiate the transient and cause Load Pulling of the VCO by shifting the frequency. This is avoided by use of the frequency doubler. Secondly, operating the PLL and the VCO at half the frequency helps reduce the operating current. Also, the process of

doubling provides some isolation in terms of frequency pulling the VCO is subjected when the PLL is shut down or other such switching events.

The Evaluation Board provides an option of bypassing the onboard PLL and directly injecting a signal source to the doubler, as shown in the schematic Figure 1. This feature enables the user to measure the performance with a an external signal generator or customer's specific VCO. In order to inject an external LO, a Zero Ohm Resistor R6 needs to be soldered on to the board. The default value of R6 is "No Place". The pad for Resistor R16 provides the means to experiment with matching, if need be. Also, resistor R21 needs to be removed. R6 is kept a "No Place" when using the onboard VCO to avoid any possible VSWR from the track containing R6 and C22.

The sensitivity of the PLL to the input at pin F_{IN} (Pin 15) reduces as you increase the supply voltage. That is, at higher supply voltages you need more LO power. The Evaluation Board has been designed for operation at 3.6 Volts. If there is a need to test the Evaluation Board at a higher supply voltage, there may arise a requirement to increase the LO power being delivered to Pin 15.

The onboard VCO runs off a National Semiconductor LDO (Low Drop Out Regulator) LP2980 which provides a clean supply and isolates the VCO from frequency pulling due to switching events in other parts of the Evaluation Board. To bypass the regulator and provide unfiltered supply to the VCO resistor R11 needs to be made Zero Ohms and R40 needs to be removed.

The VCO chosen for the Evaluation Board is dual band VCO. This allows for a smaller VCO gain in MHz/volt and reduces the open loop drift. It also helps in reducing the susceptibility of the VCO to noise on the Frequency Control pins, and also makes it more robust to noise on the power supply pin. One band is used for Transmit purposes and the other for Receive. Band control is achieved by controlling the voltage at Pin "V_{SW}" of the VCO. Resistors R15 and R13 provides the means to implement this. It is also possible to control this selection through software by using one of the three CMOS output pins of the LMX3162, Pin 21, 22 and 23, to control a small, external transistor. The output of this transistor may be wired to control the bandswitch pin "V_{SW}" of the VCO. There is no provision on the Evaluation Board for this transistor.

The Evaluation Board PLL has been designed to perform phase comparison at a frequency of 500 kHz. This PLL incorporates a dual modulus prescaler, and this allows a step size of 500 kHz in the frequency synthesized. This synthesized frequency is doubled, and the final step size at **TX Out** is 1 MHz. Protocols for the 2.4 GHz ISM Band require channels to be spaced at ≥ 1MHz.

The Loop Filter for the PLL has been designed for a loop bandwidth of 80kHz, in order to have "Start and Lock Time" of around 300µs. This is the time required to power up the PLL and then lock it, and can be substantially more than the time required to simply change the lock frequency from one adjacent channel to another. PLL Lock is measured as the instant the PLL achieves a frequency error of less than 50kHz with respect to the programmed frequency. This is similar to the offset frequencies permitted by 2.4 GHz ISM Band protocols. The locking time requirement of a specific application comes from the packet structure of the protocols.

The other defining parameters of the Loop Filter are Phase Margin 45° and Attenuation 20dB. The term Attenuation refers to the extra amount of reference attenuation provided by the RC Filter made by R3 and the parallel combination of C3 and C40. The component values for the Loop Filter have been calculated using CodeLoader's **Calc Filter** Utility. Using the software the loop filter can be modified to adjust the loop bandwidth.

The MICROWIRE™ Emulation Cable has the three signals required by the MICROWIRE™ Bus: LE, Data and Clock. In addition, it also has the S_Field and the Trigger signals. The Trigger signal may be used to synchronize test equipment such as oscilloscopes and spectrum analyzers to state changes in the LMX3162. The use of the S_Field is explained in the Receiver section.

A magnified schematic of the Loop Filter and the PLL is shown in Figure 2.

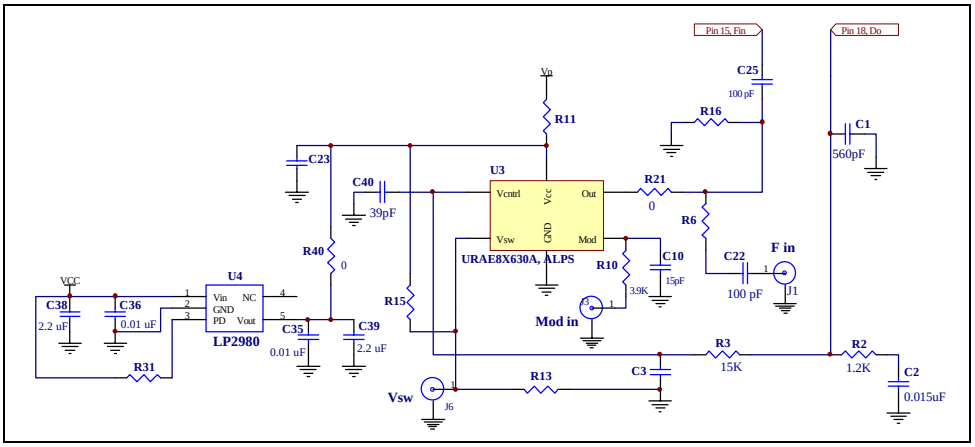

Figure 2: PLL and VCO

Receiver Operation

The Evaluation Board achieves a BER of 1e-3 for an input power of –93dBm when operating in the Open Loop Burst Mode. The BER Sensitivity gets degraded by a dB or two if the Evaluation Board is operated in the PLL Locked, Continuos Mode. The tests are done with a GFSK, BT=0.5, 1Mbps, 250kHz Deviation signal. Other FM based modulation schemes are possible with Evaluation Board, but the relevant need to be modified. With the use of a lower loss ceramic filter and a higher performing LNA, sensitivity of –96dBm can be achieved.

LNA

The LNA has been designed around a Siemens' BFP420 Transistor, and achieves a performance of 13dB Gain and 2dB Noise Figure. It is possible to improve the gain of this LNA while maintaining the same Noise Figure, using the same transistor. “No Place” component L4, along with components already placed C54, L1, and L15 provide flexibility in modifying the LNA impedance match. The voltage regulator internal to the LMX3162, which supplies 2.7 Volts, powers the LNA. It draws 10mA. The LNA can be redesigned to run at 5mA and provide similar performance. A magnified schematic of the LNA is shown in Figure 3.

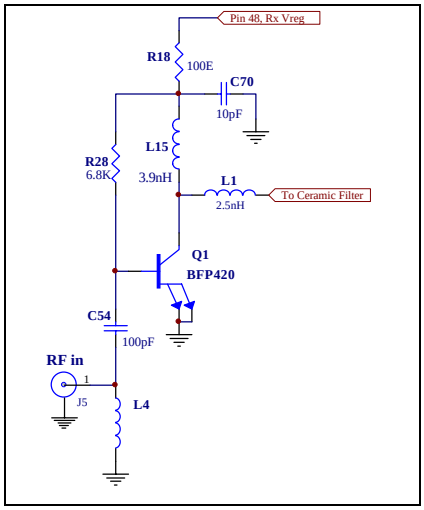

Figure 3: Low Noise Amplifier

Image Reject Filter and Mixer

The LMX3162 processes the IF signals at 110.6 MHz, and the LO is chosen to be 110.6MHz below the RF Input. This makes the Image Frequency 110.6MHz above the RF Input, and the Evaluation Board has to be able to reject this unwanted signal. This filtering is done by a 2-pole ceramic bandpass filter U2. Capacitor C47 and the pad of "No Place" L8 and provide the impedance match. The user may modify L8 and C47 to try out other possible solutions. The ceramic filter has a 3dB bandwidth of 84 MHz centered at 2442 MHz. It has a typical insertion loss of 2dB.

The mixer downconverts the RF signal to 110.6 MHz and has about 17dB gain with 11dB Noise Figure. The Output Third Order Intercept Point of this mixer is 7.5dBm.

IF SAW and RC Filter

After the RF signal gets downconverted to IF, it needs to be bandlimited for channel selection. IF filtering is very helpful in a multi-signal environment. When the receiver receives more signals at more than one frequency, the IF filter provides the desired selectivity and prevents generation of spurii in the Limiter and the Quadrature Detector. Limiters are inherently very nonlinear devices and in a hostile environment stronger, unwanted signals can "Capture" the receiver if no IF filtering is employed. The IF filtering thus has to be implemented before the Limiter. Bandlimiting is also required to provide an optimum BER, the primary requirement for which is to limit the noise power as much as possible. This filtering can be done either before the Quadrature Detection or after it. To restate the above, for every IF filter, there is an equivalent baseband filter. As baseband filters are easier to implement than IF filters, it would appear that we can forgo IF filtering and do all the filtration in the baseband. However, it is a known fact that discriminators have non-linear performance with respect to the input signal-to-noise ratio. This is called the Threshold Effect. The discriminator needs to see a signal-to-noise ratio that is above a certain threshold, otherwise its performance degrades very rapidly. Hence there is a requirement to filter the IF signal early on in the chain. In the Evaluation Board the IF Filter is implemented by a SAW Filter, U5. The SAW Filter is centered nominally at 110.6 MHz, and has a 3dB Bandwidth of 1.5 MHz. The minimum insertion loss is about 2.55dB. The input and output matching components for the SAW Filter are C9, L3 and L2, L5 respectively. Capacitor C4 is a DC block element. The number of matching and decoupling components required can be reduced by changing the layout of the board.

After the initial filtering, the IF signal is amplified by the IF Amplifier. The output of the IF Amplifier needs to be fed to the IF Limiter, but after an attenuation by 8dB. This is required for the RSSI circuitry of the LMX3162 to operate linearly. This attenuation is achieved by the combination of R7, C26 and C50, which also provide some filtering.

The SAW and RC IF Filters are shown in Figure 4.

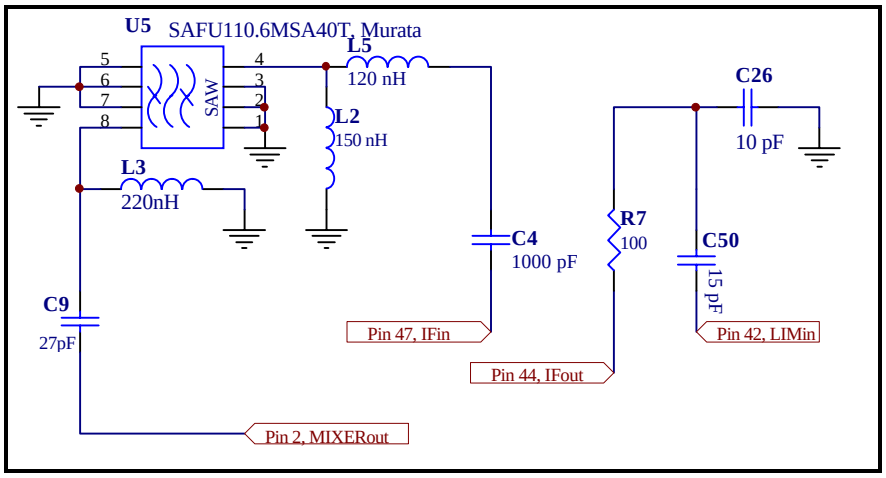

Figure 4: SAW and RC IF Filters

Quadrature Detector and Output Low Pass Filter

The LMX3162 demodulates the IF signal by Quadrature Demodulation. The Quadrature Demodulation Tank consists of C52, L16 and the variable capacitor C51. The variable capacitor is utilized to tune the Tank, along with its associated parasitics, at exactly the right frequency such that when the a CW signal at 110.6 MHz is given to the IF Limiter of the LMX3162, the output at the SMA connector **Disc Out** is 1.4 – 1.5 Volt. The user may, if need be, change the Tank elements to those having different Q's and values. Higher Q's mean a narrower bandwidth and greater sensitivity. This translates to better SNR and also greater ISI. Conversely, lower Q's result in slightly lower SNR and lesser ISI. The LMX3162 has a Quadrature Shift Capacitor internal to it. The value of this capacitor is 1pF.

Once the signal has been demodulated, it is passed through an Active Low Pass Filter. This further limits the noise bandwidth of the system and provides larger V_{PP} output. The 3dB bandwidth of this filter is 1.2 MHz. The Quadrature Tank and the Active LPF are shown in Figure 5.

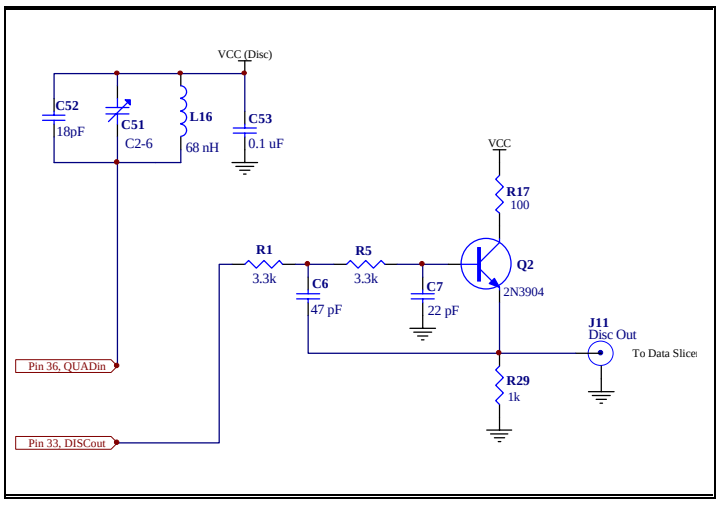

Figure 5: Quadrature Tank and Active LPF

The LMX3162 provides a feature that eliminates the effect of any initial frequency offset between the Transmitter and the Receiver. Most RF protocols have an initial Synchronization Field during which a string of alternating 1's and 0's is transmitted. During this time, the demodulated signal is well known and its average represents the nominal center frequency of the transmitter. This average level can be captured by a Sample-And-Hold (SAH) circuit and used as a reference level for a data slicing comparator which converts the demodulated signal into logic level 0's and 1's. The LMX3162 features an onboard SAH. The input to the SAH is through the SMA connector **DC Comp In**, the output is SMA Connector **Thresh** and the SAH action is controlled by the **S_Field** Logic Control. An Internal Resistor of 3000 Ohms and external capacitor C33 provide the averaging time constant.

In production, it is possible to get rid of the manual tuning that variable capacitor C51 requires by replacing it with a varactor. The voltage at the LPF output **Disc Out** is measured by the systems' ADC, compared inside the systems' µC to a reference of 1.5 Volts, and the generated error signal is amplified and converted back to an analog signal by using the µC's Digital to Analog Converter (DAC). The scheme is shown in Figure 6.

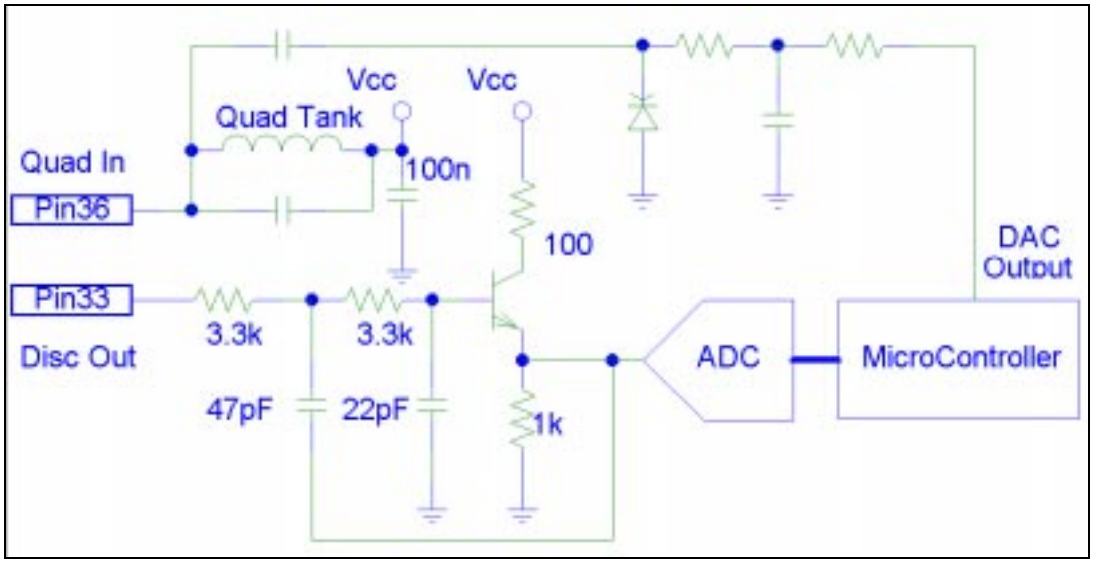

Figure 6: Automatic Tank Tuning

Transmitter Operation

Generating a Transmit RF signal is done by simple Frequency Modulation of the VCO. It is done Open Loop as otherwise the PLL would react to the Frequency Shift produced by the modulation process and try to correct for it. The rate at which the PLL would react is determined by the loop parameters such as loop bandwidth. The VCO chosen for the Evaluation Board has a pin called the Modulation Pin. Its is available as a SMA connector input marked **Mod In**. The doubled output is available at the SMA connector marked **Tx Out**. Components C48, C55, L7 and L9 provide flexibility in filtering or impedance matching the output. The doubler is designed to work looking into a real impedance between 50 and 100 Ohms. It delivers about –8.5dBm to a real 50-Ohm load.

The Evaluation Board expects a filtered baseband signal at the input **Mod In**, and its amplitude needs to be adjusted externally to give the right frequency deviation. This can be as simple as a resistive divider.

Typical Performance Of The LMX3162 Evaluation Board

The LMX3162 has been designed for Open Loop Burst Mode operation, and parameters such as spectrum during open loop and open loop frequency drift are important from the point of view of design and meeting system requirements. Also important are PLL lock times and Frequency Doubler Output spectrum. These measurements are easily made with the LMX3162 Evaluation Board and some typical plots are shown below.

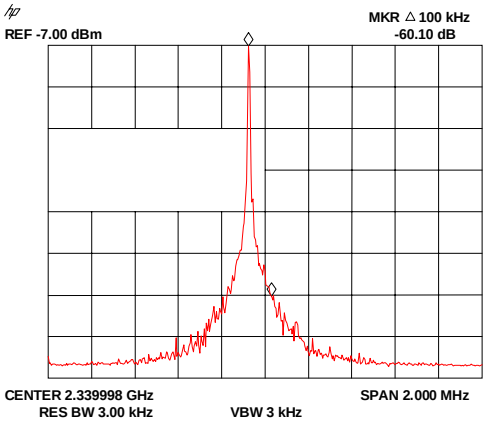

Figure 7: Open Loop Spectrum at Tx Out, Span 2MHz

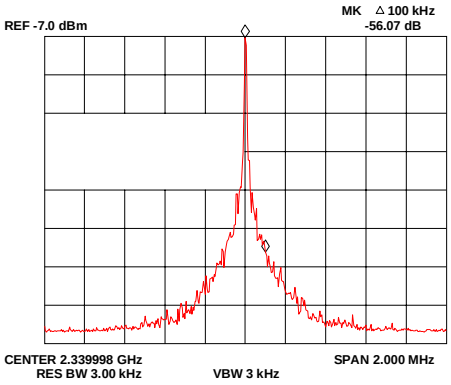

Figure 8: Closed Loop Sectrum at Tx Out, CP=1.5mA, Span 2MHz

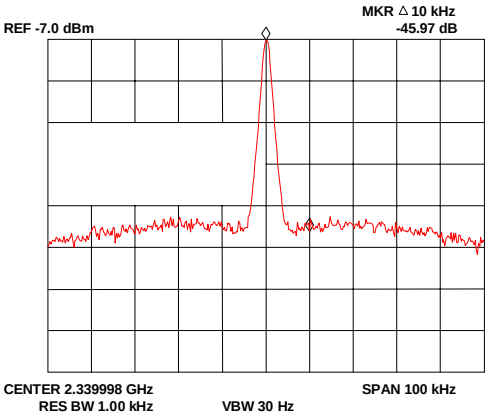

Figure 9: Closed Loop Spectrum at Tx Out, CP=6mA, Span 100kHz

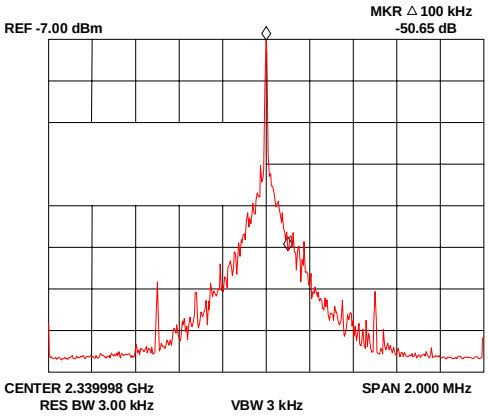

Figure 10: Closed Loop Spectrum at Tx Out, CP=6mA, Span 2MHz

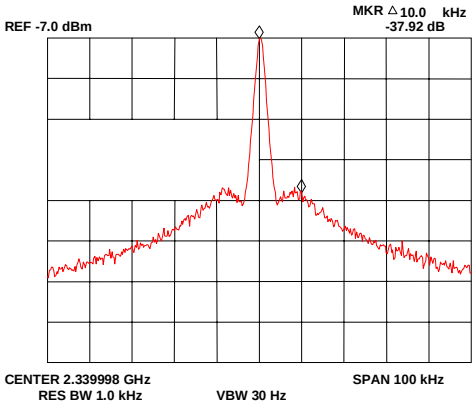

Figure 11: Closed Loop Spectrum at Tx Out, CP=1.5mA, Span 100kHz

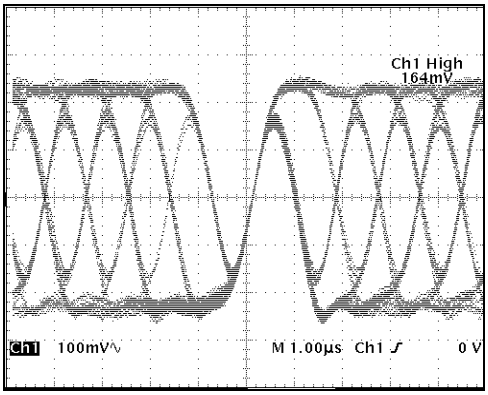

Figure 12: Demodulated Signal at Disc Out

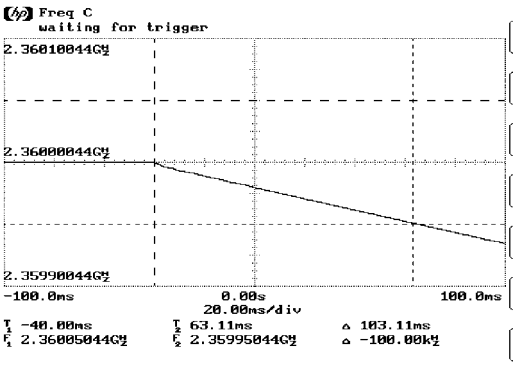

Figure 13: Open Loop Frequency Drift

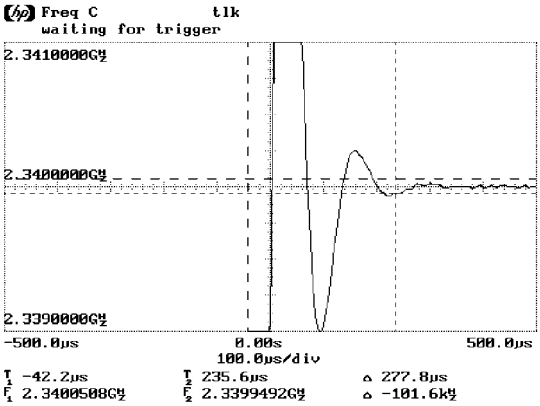

Figure 14: Start and Lock Time

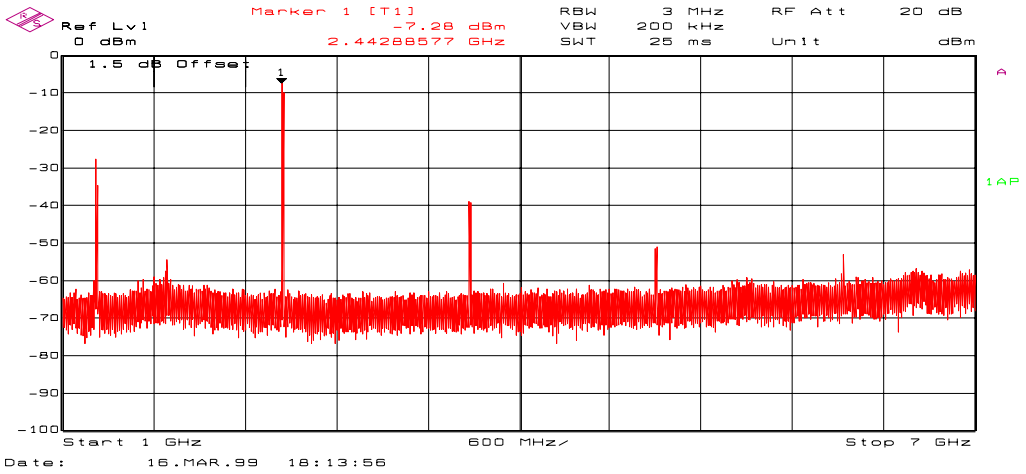

Figure 15: Transmit Output and its Harmonics

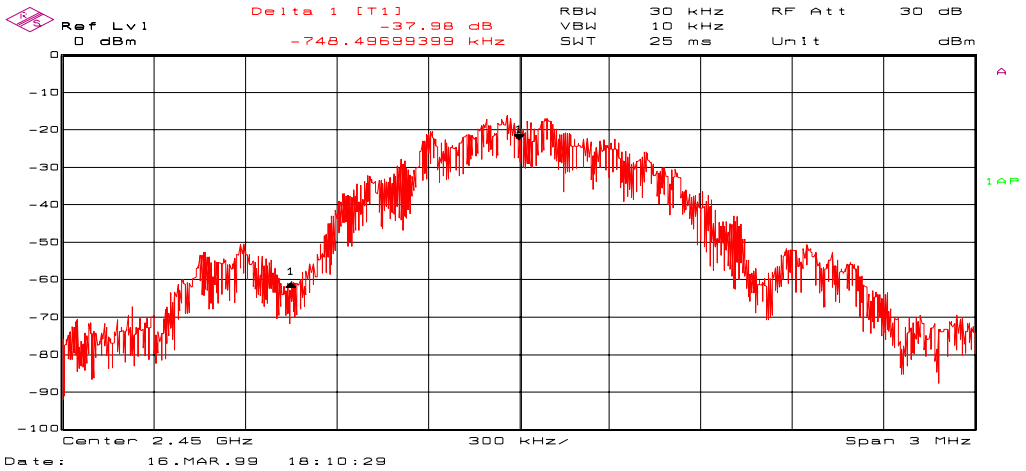

Figure 16: Tx Out Spectrum in Transmit Mode, 1 Mbps, GFSK, Gaussian BT=0.5, Deviation=250kHz

LMX3162 Evaluation Board Schematic and Layout Diagrams

The Evaluation Board has four layers: Top, Mid1, Mid2 and Bottom. Layer Mid1 is not shown as it is a ground plane. Components without values in the Schematic are “No Place”. They are intended to give flexibility in customizing the board.

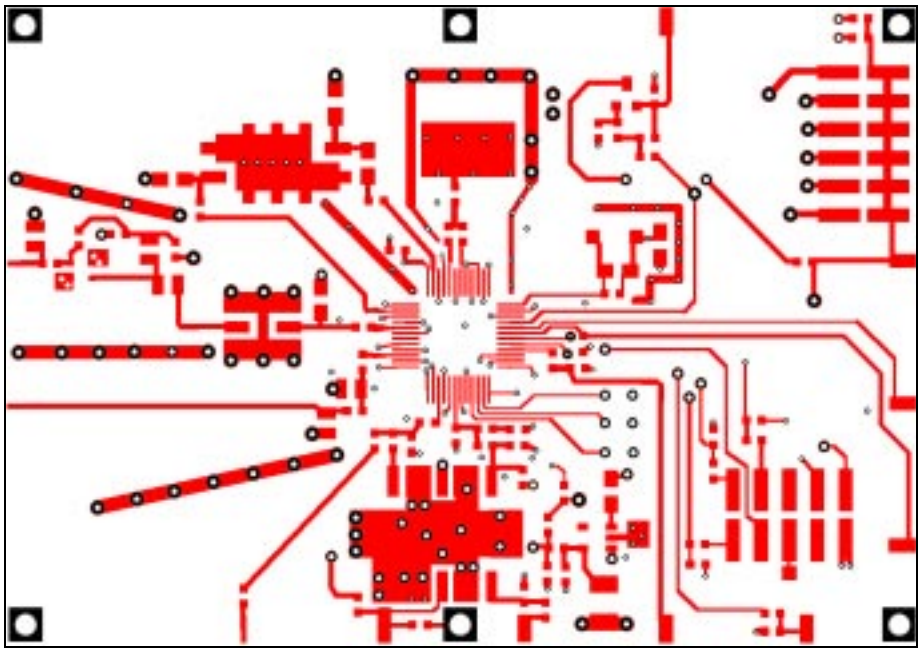

Figure 17: Top Layer, Not to Scale

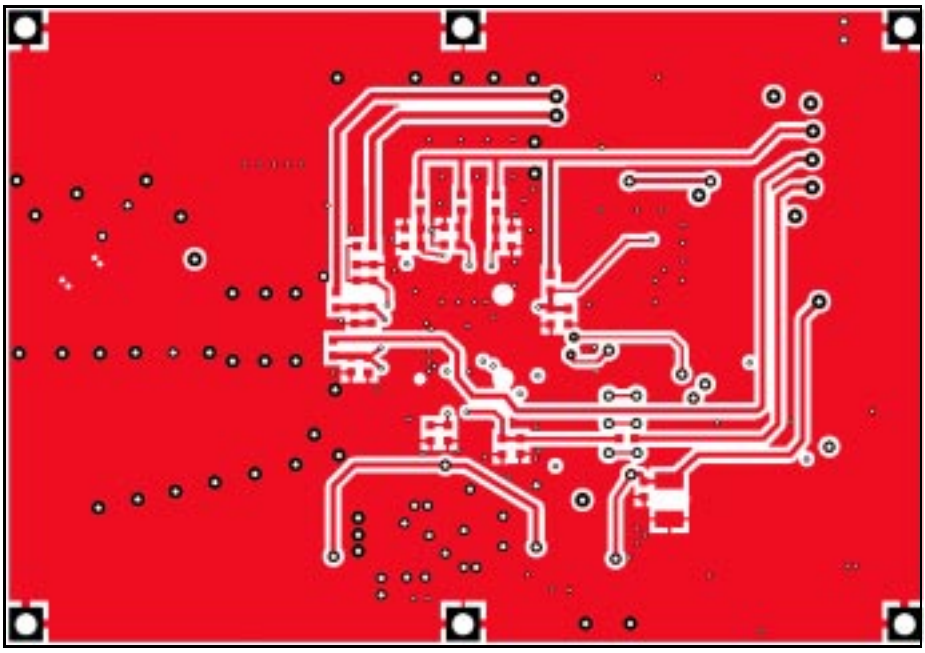

Figure 18: Bottom Layer, Not to Scale

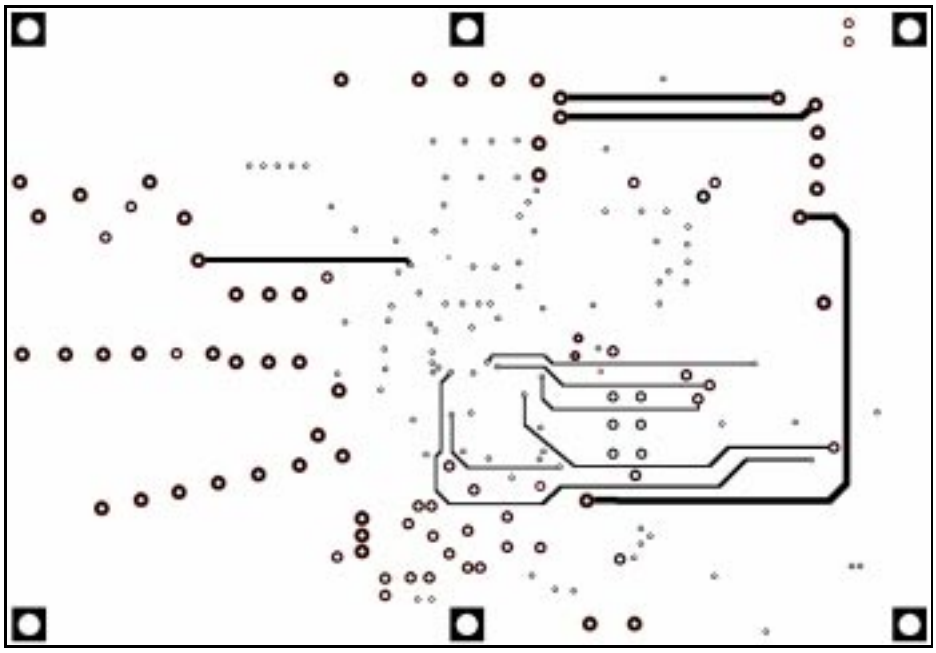

Figure 19: Mid Layer 2, Not to Scale

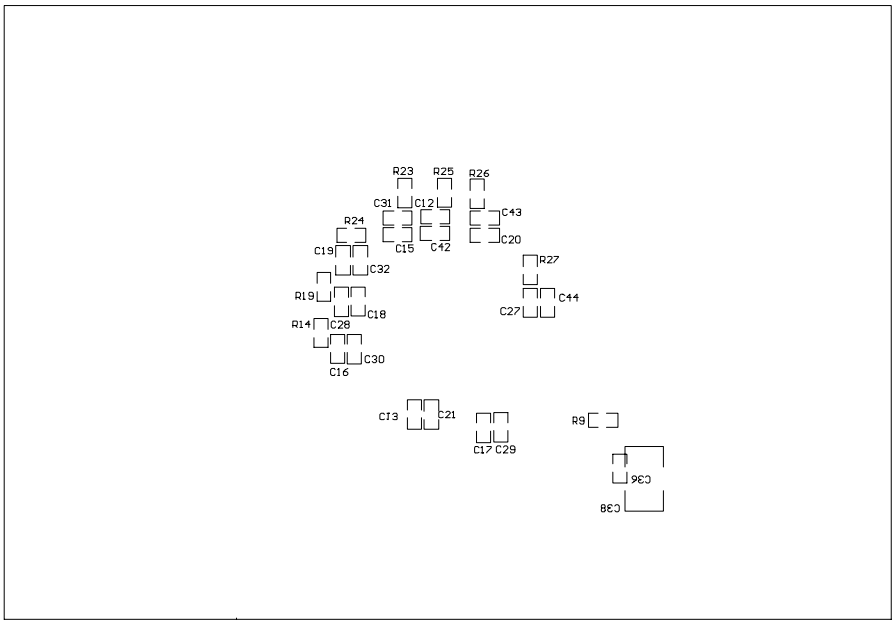

Figure 20: Bottom Overlay, Not to Scale

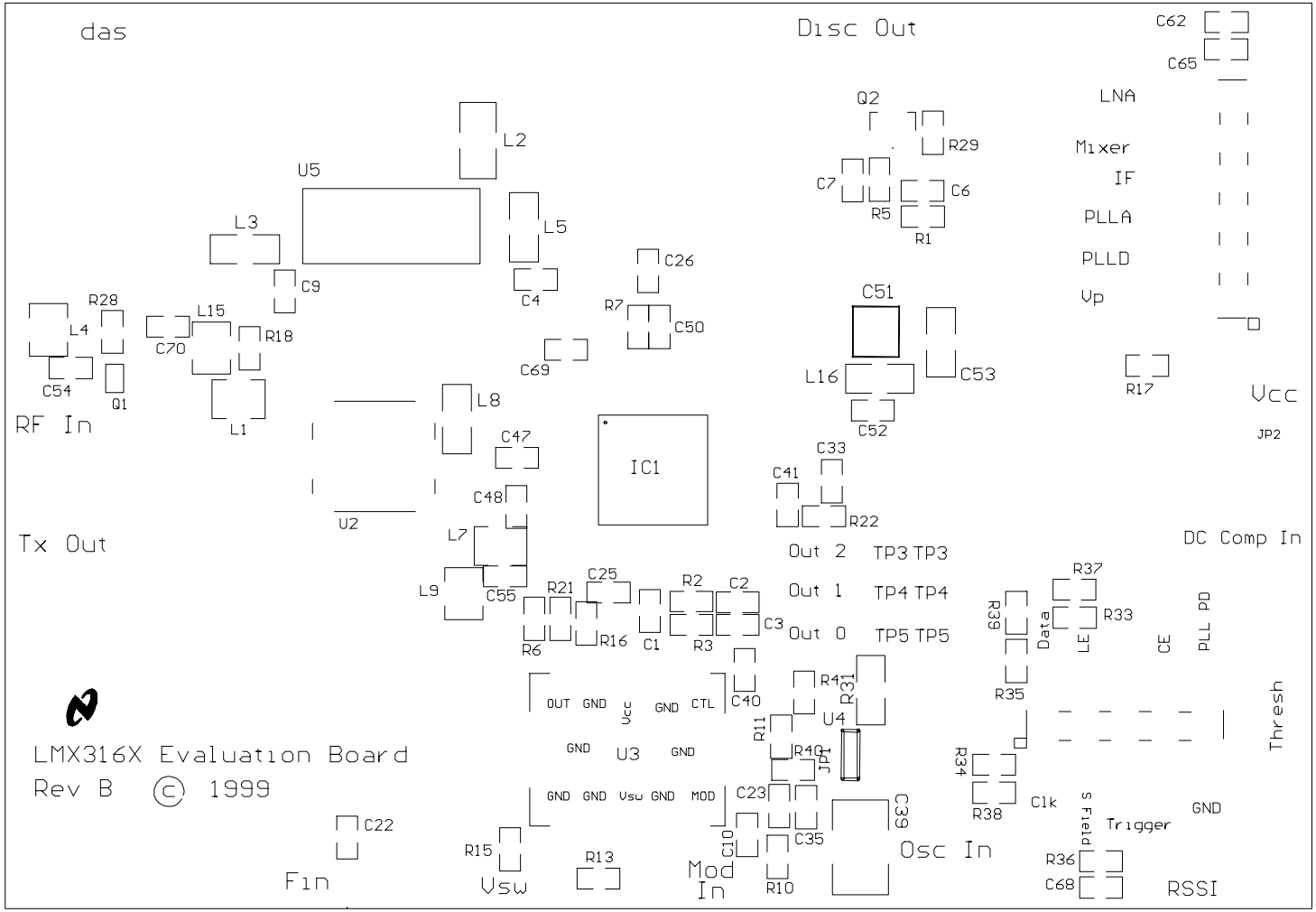

Figure 21: Top Overlay, Not to Scale

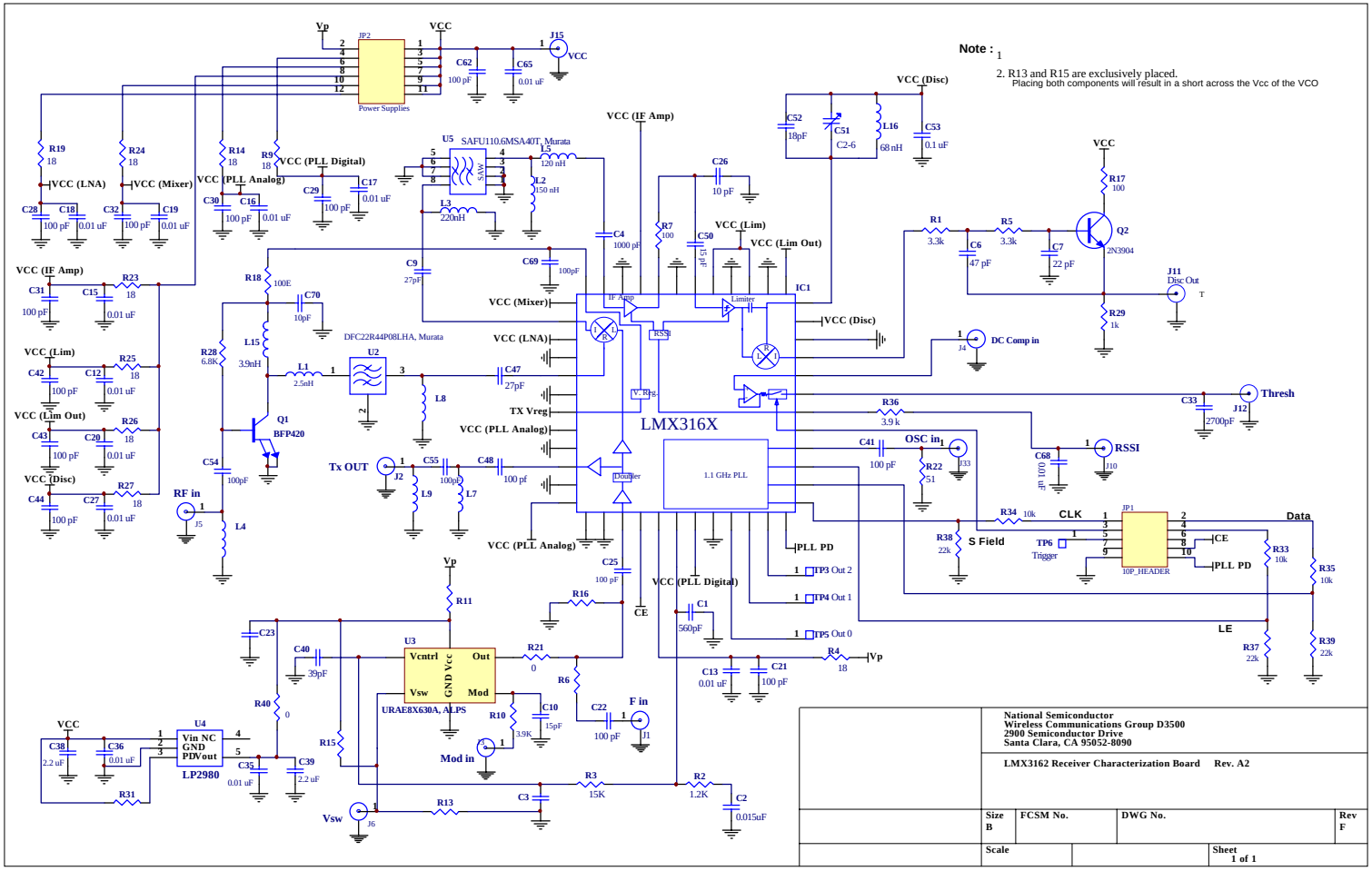

Figure 22: Schematic

Bill Of Materials

Serial Number	Number Used	Part Type	Designator
1	1	560pF	C1
2	1	15pF	C10
3	13	0.01 uF	C12 C13 C15 C16 C17 C18 C19 C20 C27 C35 C36 C65 C68
4	1	0.015uF	C2
5	14	100 pF	C21 C22 C25 C28 C29 C30 C31 C32 C41 C42 C43 C44 C48 C62
6	2		C23 C3
7	1	10 pF	C26
8	1	2700pF	C33
9	2	2.2 uF	C38 C39
10	1	1000 pF	C4
11	1	39pF	C40
12	2	27pF	C47 C9
13	1	15 pF	C50
14	1	C2-6	C51
15	1	18pF	C52
16	1	0.1 uF	C53
17	3	100pF	C54 C55 C69
18	1	47 pF	C6
19	1	22 pF	C7
20	1	10pF	C70
21	1	LMX316X	IC1
22	1	F in	J1
23	1	RSSI	J10
24	1	Disc Out	J11
25	1	Thresh	J12
26	1	VCC	J15
27	1	Tx OUT	J2
28	1	Mod in	J3
29	1	OSC in	J33
30	1	DC Comp in	J4
31	1	RF in	J5
32	1	Vsw	J6

Serial Number	Number Used	Part Type	Designator
33	1	10P_HEADER	JP1
34	1	Power Supplies	JP2
35	1	2.5nH	L1
36	1	3.9nH	L15
37	1	68 nH	L16
38	1	150 nH	L2
39	1	220nH	L3
40	4		L4 L7 L8 L9
41	1	120 nH	L5
42	1	BFP420	Q1
43	1	2N3904	Q2
44	2	3.3k	R1 R5
45	1	3.9K	R10
46	6		R11 R13 R15 R16 R31 R6
47	9	18	R14 R19 R23 R24 R25 R26 R27 R4 R9
48	2	100	R17 R7
49	1	100E	R18
50	1	1.2K	R2
51	2	0	R21 R40
52	1	51	R22
53	1	6.8K	R28
54	1	1k	R29
55	1	15K	R3
56	3	10k	R33 R34 R35
57	1	3.9 k	R36
58	3	22k	R37 R38 R39
59	1	Out 2	TP3
60	1	Out 1	TP4
61	1	Out 0	TP5
62	1	Trigger	TP6
63	1	DFC22R44P084LHA, Murata	U2
64	1	URAE8X630A, ALPS	U3
65	1	LP2980, NSC	U4
66	1	SAFU110.6MSA40T, Murata	U5

Configuring the CodeLoader for the LMX3162

The Main Menu and the Port Setup Menu of the CodeLoader should be programmed as shown in Figure 23and Figure 24 respectively.

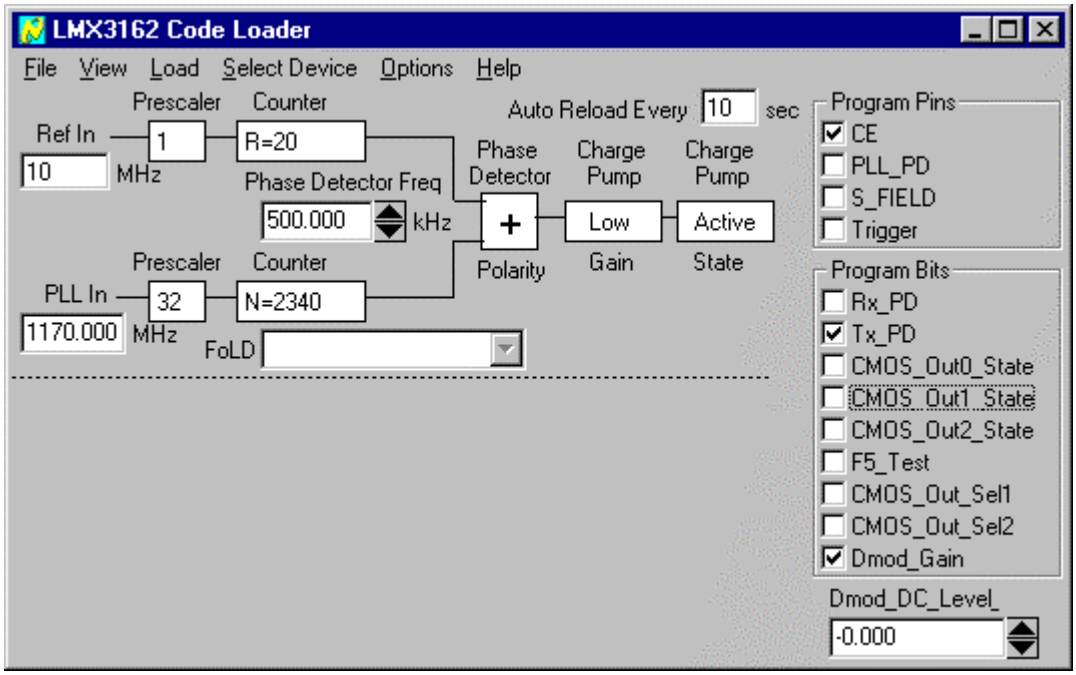

Figure 23: Main Menu Settings of the CodeLoader for operation in the Receive Mode

The parameters above the dotted line are for the PLL. The parameter boxes can be changed by by clicking on and entering new values. The user must press **Enter** on the keyboard after the parameters are changed. Only registers for which the new changes are relevant are loaded when the **Enter** is pressed.

- **Ref In** - TCXO or reference crystal oscillator input. NSC's LMX3162 evaluation board is designed for a 10 MHz TCXO. The user is advised to use a high quality crystal reference for an accurate and low noise measurement. A high quality 10 MHz reference signal is generally available from most spectrum analyzer's reference output port or signal generator reference output port.
- **Phase Detector** - Phase detector (comparator) frequency. NSC's LMX3162 evaluation board has been designed for a 500 kHz PLL phase detector frequency. The component values of the loop filter require redesign if the user wishes to use other phase detector frequency.
- **PLL In** - VCO output frequency (PLL fin input frequency). The operating frequency for the VCO on NSC's LMX3162 evaluation boards is 1170MHz. The VCO used is ALPS' EX630A. The user is allowed to enter a frequency within the VCO operating frequency range. The component values of the loop filter should be redesigned if the user wishes to use other VCOs.
- **Prescale** - Prescaler value of the counters. The prescaler value can be changed by clicking on the **Prescale** box.
- **Phase Detector Polarity** - The polarity can be changed by clicking on the "+" or "-". Refer to the datasheet for the description of this function.
- **Charge Pump Gain** - Charge pump output current. The LMX3162 has high and low charge pump gain modes. The modes can be changed by clicking on "High" or "Low". The LMX3162 evaluation loop filter is designed for the "Low" charge pump gain.

- **Auto Reload Every [XX] sec** - Time interval the program reloads all the counters. The user enables the reload function by selecting **Options - Auto Reload** from the pull down menu.
- **FoLD** – Not used.
- **Program Pins - Trigger:** External Trigger for the programming port. The programming port assigned for **Trigger** becomes high when selected and port goes low when not selected. Can be used in the **BurstMode** to trigger external test equipment for measurements.
- **Program Pins – CE:** Chip Enable.
- **Program Pins – PLL_PD:** PLL Power Down.
- **Program Pins – S_Field:** Controls the S_Field pin. See datasheet for description.
- **Program Bits –Rx_PD:** Power Down the Receiver
- **Program Bits –Tx_PD:** Power Down the Transmitter
- **Program Bits –CMOS_Out0_State:** Control CMOS I/O pin Out0. See Datasheet for description.
- **Program Bits –CMOS_Out1_State:** Control CMOS I/O pin Out1. See Datasheet for description.
- **Program Bits –CMOS_Out2_State:** Control CMOS I/O pin Out2. See Datasheet for description.
- **Program Bits –F5_Test:** Not used in Application.
- **Program Bits –CMOS_Out_Sel1:** Not used in Application.
- **Program Bits –CMOS_Out_Sel2:** Not used in application.
- **Program Bits –DMOD_Gain:** Toggles between demodulator gain 1X/3X. Checking the box on the left means operation in 3X.
- **Dmod_DC_Level:** DC shift the demodulator output by the selected amount. See datasheet for description.

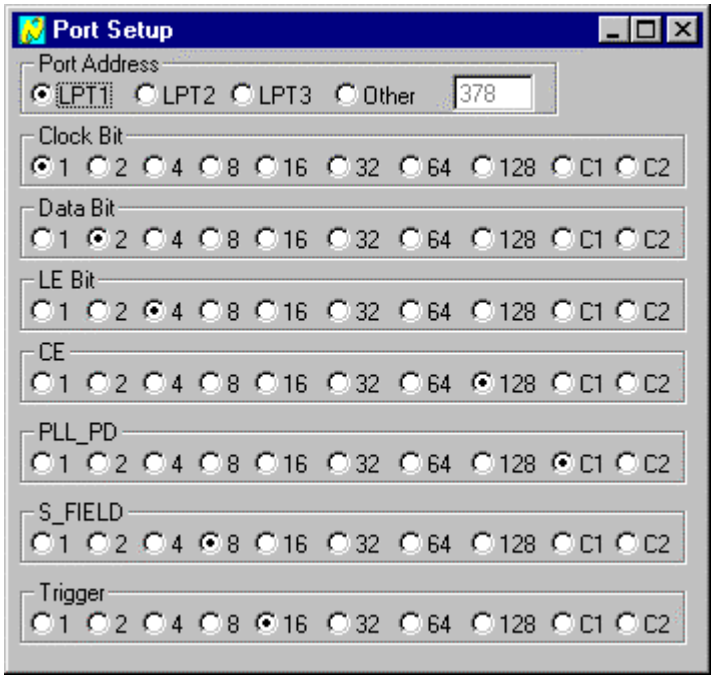

Figure 24: Port Setup Menu Settings of the Codeloader.

The Port Address in the Port Setup Menu must show the address of the Parallel Port in the User's PC.

References

1. LMX3162 Datasheet, National Semiconductor Corporation.
2. CodeLoader 1.32 Instructions, National Semiconductor Corporation
3. LP2980 Datasheet, National Semiconductor Corporation.
4. DFC22R44P084LHA Datasheet, Murata manufacturing Co., Ltd.
5. SAFU110.6MSA40T Datasheet, Murata Manufacturing Co., Ltd.
6. URAE8X630A Datasheet, Alps Electric Co., Ltd.
7. BFP420 Datasheet, Siemens.
8. PMBS3904 Datasheet, Philips Semiconductors.