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LMX2352 Evaluation Board Operating Instructions

General Description

The LMX2352 Evaluation Board simplifies evaluation of the LMX2352 1.2 GHz/550 MHz PLLatinum dual frequency synthesizer. The board enables all performance measurements with no additional support circuitry.

The evaluation board consists of a LMX2352 device, a RF VCO module and IF VCO & RF/IF loop filters built by discrete components. The SMA flange mount connectors are provided for external reference input, RF and IF VCO outputs, and the power and grounding connection. A cable assembly is bundled with the evaluation board for connecting to a PC through the parallel printer port. By means of MICROWIRE™ serial port emulation, the Code Loader software included can be run on a PC to facilitate the LMX2352 internal register programming for the evaluation and measurement.

Quick Start

The LMX2352 Evaluation Board is fully assembled and factory tested. Follow the instructions below to set up the hardware platform for the measurement of interest.

Recommended Test Equipment

- Spectrum analyzer (operating frequency range ≥ 2 GHz)
- Modulation domain analyzer
- DC power supply with adjustable voltage outputs
- 14.4 MHz signal source/generator (high quality TCXO is preferred).

Connection and Setup

1. Connect the RF_OUT/IF_OUT output port to the input of a spectrum analyzer for phase noise and reference spur measurement or the input of a modulation analyzer for lock time measurement.

2. Connect a 14.4 MHz oscillator reference to the OSCin input port. It is advised to use a high quality reference source (i.e. TCXO) for an accurate and low noise measurement. Remove the 51 Ω resistor at OSCin input port (R51 of the schematic in Appendix A) if a TCXO is used for the reference source. Keep the 51 Ω resistor if signal generator is used.

3. Plug the DB25 connector end of the cable assembly to the parallel port of the PC. Connect the other end of the cable to the on-board 5x2 pin header. Refer to the "Data cable configuration" section of the "Applications Information, Code Loader Operation" for pin #1 position.

4. Verify that six jumper blocks are placed to shunt pin 1 & 2, pin 3 & 4, and so on to connect RF_Vvco, Vp_RF, Vcc_RF, Vcc_IF, Vp_IF, and IF_Vvco respectively to Vcc power source. Refer to Appendix A for more details.

5. Turn on the DC power supply and adjust the voltage output to 3 volts. Turn off supply.

6. Connect the DC power supply output to the Vcc port of the evaluation board. Turn on supply.

7. Connect a 14.4 MHz TCXO to the OSCin port, or turn on the signal generator and set the reference output frequency to 14.4 MHz.

8. Run the Code Loader software on the PC for LMX2352 register programming. Refer to Appendices D and E for more details.

Phase Noise Measurement Using A Spectrum Analyzer

1. Use the Code Loader software to set the desired frequency and to program the LMX2352 device. Refer to Appendix E for more details.

2. Set the spectrum analyzer to the desired center frequency, and adjust the span so the appropriate offset frequency can be viewed.

3. Turn ON the video averaging feature of the analyzer for better determination of the noise level.

4. The difference between the carrier level and the noise level minus 10[log(resolution bandwidth)] is equal to the phase noise in dBc/Hz. The resolution bandwidth can be read directly from the spectrum analyzer.

Reference Spur Measurement Using A Spectrum Analyzer

1. Use the Code Loader software to set the desired frequency and to program the LMX2352 device. Refer to Appendix E for more details.

2. Set the spectrum analyzer to the desired center frequency, and set the span to allow the reference sidebands to be viewed. For example, the span can be set to 500 kHz during RF VCO measurement because its loop filter design is based on 160 kHz reference frequency.

3. The reference spur is the difference between the level of the VCO output frequency tone and the level of the reference spur (at the center frequency +/- the reference frequency).

Lock Time Measurement Using A Modulation Domain Analyzer

1. Decide the maximum and minimum frequency to be switched alternately. The VCO operating frequency range can be obtained in Appendix E. Enter Burst Mode menu of Code Loader software to create a macro to program the LMX2352 to the maximum and minimum frequency alternately over time. It is necessary to put a sufficient delay between PLL programming (i.e. 100,000). Refer to the "Burst Mode configuration and operation" section of the "Application Information, Code Loader Operation" for more details.

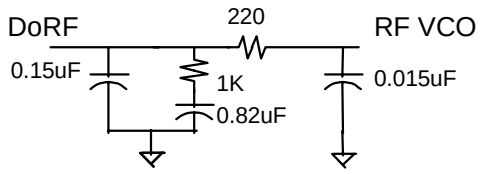
2. Set the center frequency of the modulation domain analyzer to be half-way between the maximum and minimum frequencies. Set the frequency span to cover the entire frequency range. A switching signal should be seen on the screen.

3. Set the center frequency to be the trigger condition for One-Shot mode. Press [Start/Stop] button to capture the switching curve. Adjust the frequency and time scale accordingly to get a close-up plot for detailed information.

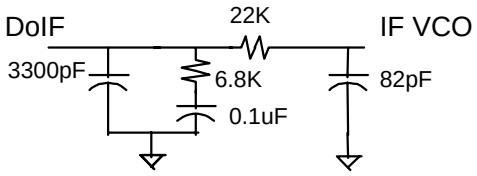
4. The lock time is the time difference between the point the frequency starts to change and the point that the PLL frequency settles within +/- 1 kHz range.

Loop Filter Illustration

A type 2 third-order passive loop filter configuration is employed on the LMX2352 evaluation board. The RF loop filters were designed assuming a 600 Hz loop bandwidth, 45 degree phase margin, 160 kHz reference frequency, and 1600 uA charge pump current mode. The IF loop filter was designed for a 200 kHz reference frequency for high charge pump current mode. The actual implementations are shown below:



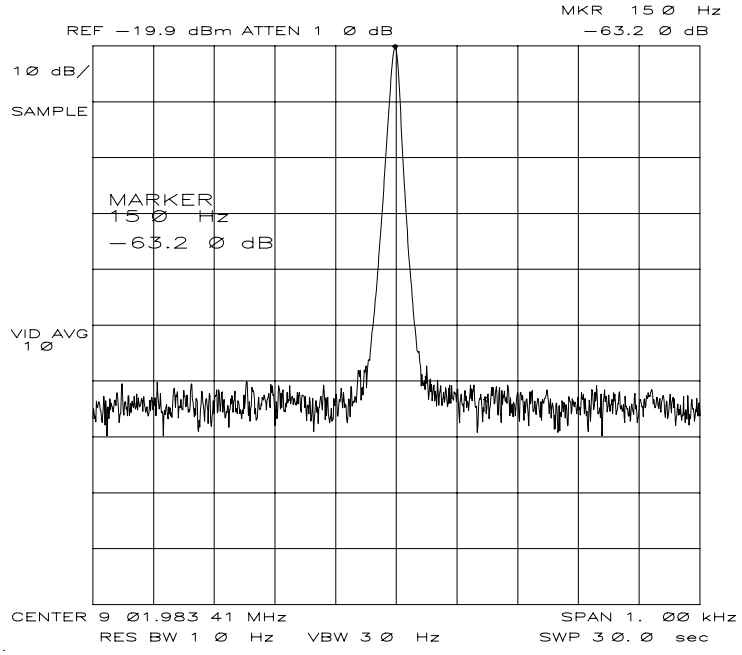
RF LOOP FILTER



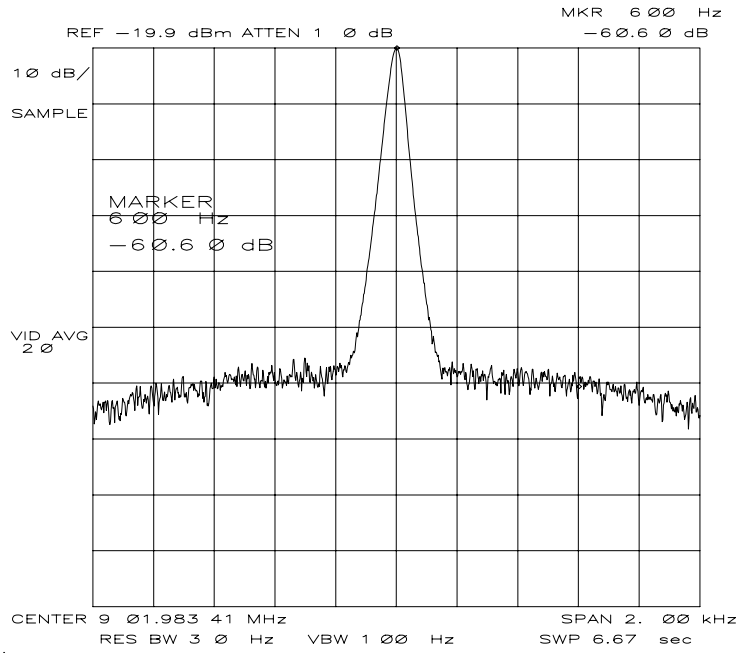
IF LOOP FILTER

LMX2352 Performance Measurement Result – A Typical Example

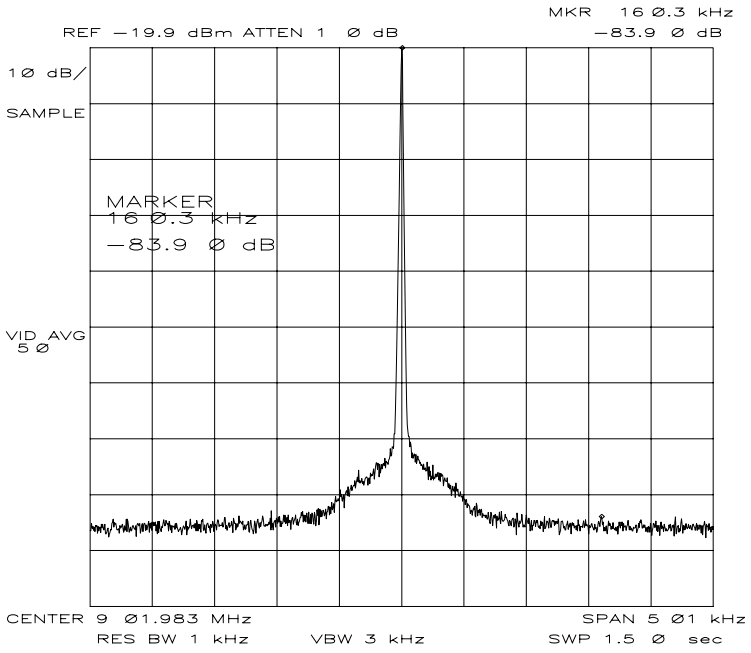
Phase Noise Measurement Result (@150Hz offset = -73.2 dBc/Hz)



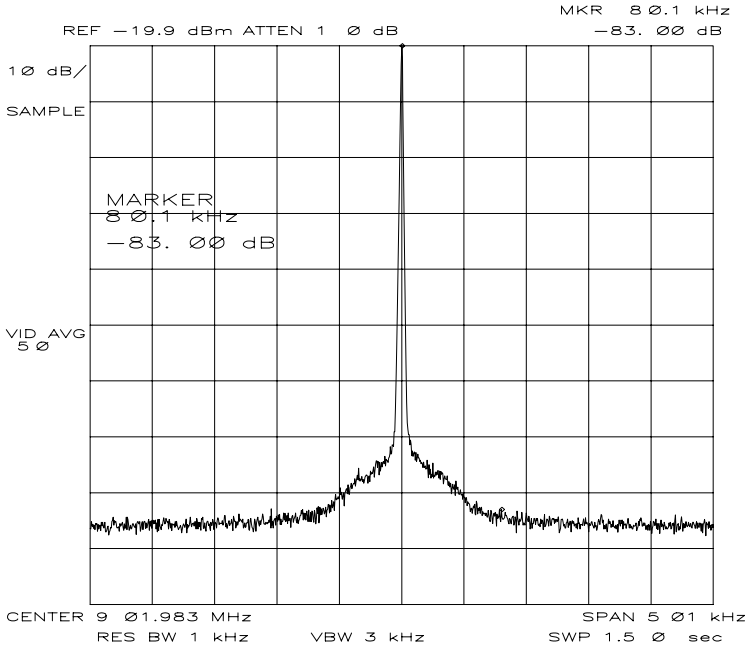
Loop Filter Bandwidth Measurement (about 600 Hz)



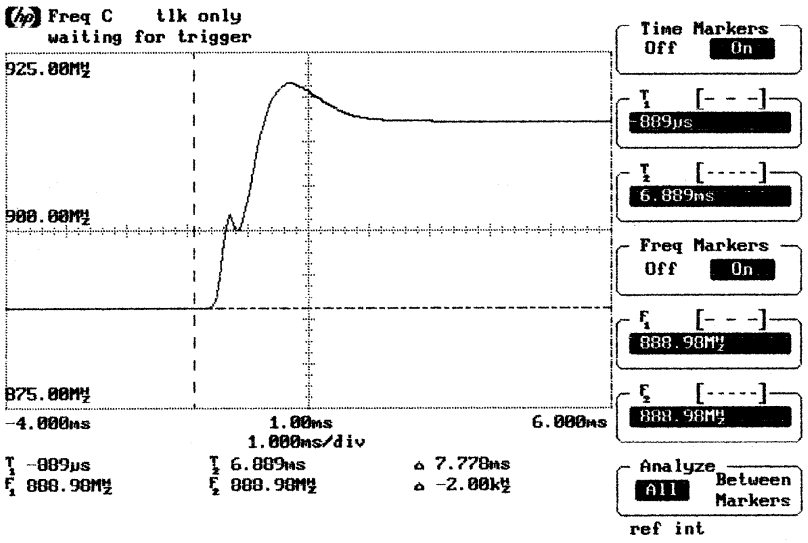
Reference Spur Measurement Result (@160KHz offset = -83.9dBc)



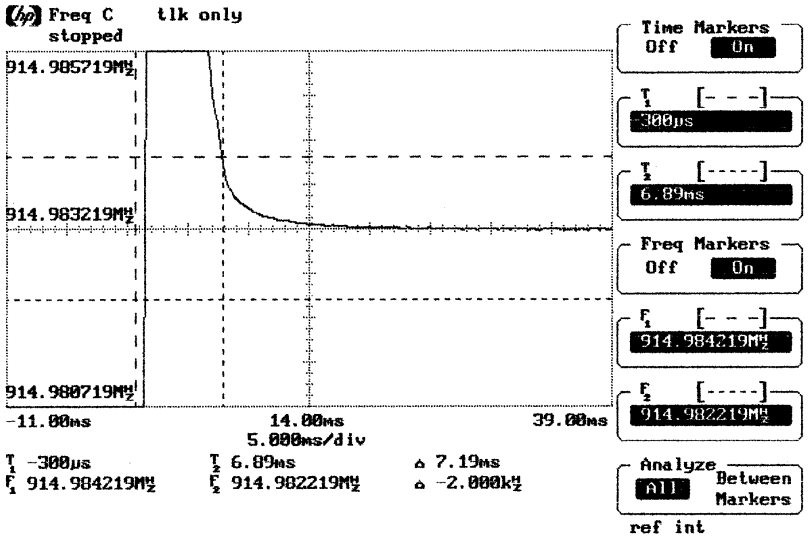
Fractional Spur Measurement Result (@80 kHz offset = -83.0 dBc, Fractional Compensation = 8/16)



Lock Time Measurement Result

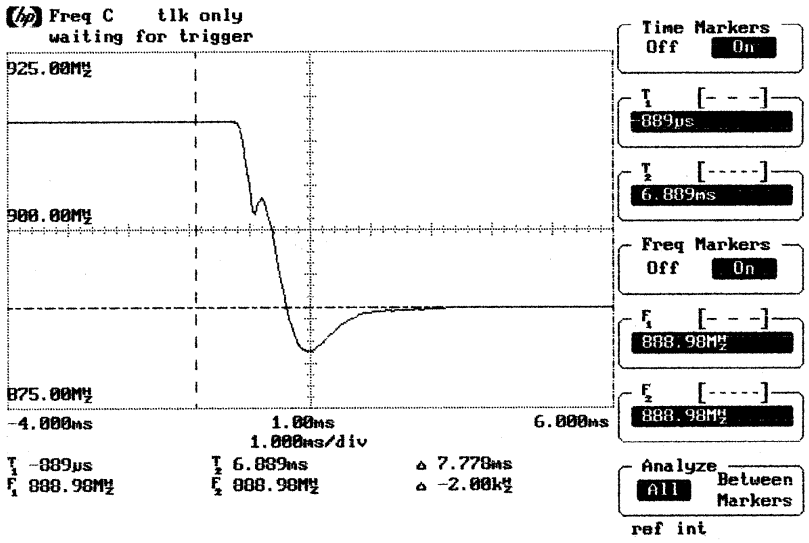


Positive Frequency Switching Waveform

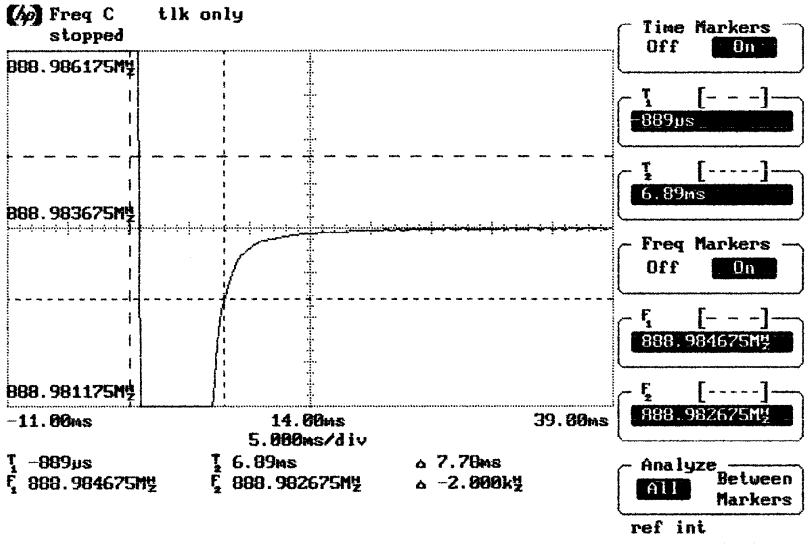


Positive Lock Time to within 1 kHz Range

Lock Time Measurement Result (Cont.)



Negative Frequency Switching Waveform



Negative Lock Time to within 1kHz Range

MEASUREMENT CONDITIONS

The LMX2352 Evaluation Board has been tested to meet the typical performance criteria as shown below:

Testing Condition

Vcc Operating Voltage	:	3.0 volts
TCXO frequency	:	14.4 MHz
RF VCO Tuning Range	:	890 - 915 MHz
Fractional Modulus:	:	16
RF Comparison Frequency	:	160 kHz (minimum channel space = 10 kHz)
IF VCO Tuning Range	:	Typical 200 MHz (See back of the evaluation board and Code Loader diskette label for the exact tuning frequency.)
IF Comparison Frequency	:	200 kHz

Typical Performance Criteria

RF VCO Phase Noise	:	Less than -65 dBc/Hz @ 150 Hz
RF VCO Reference Spur	:	Less than -70 dBc @ 160 kHz
RF VCO Lock Time	:	Less than 15 ms (within +/- 1 kHz settling frequency)

Remark

Computer monitors and other lab equipment have been shown to cause noise spikes. If you see noise spikes on the signal, try turning off the monitor or other equipment to verify that they are not the cause. Also noise may be getting onto the signal through the cable that connects to the parallel port of the computer.

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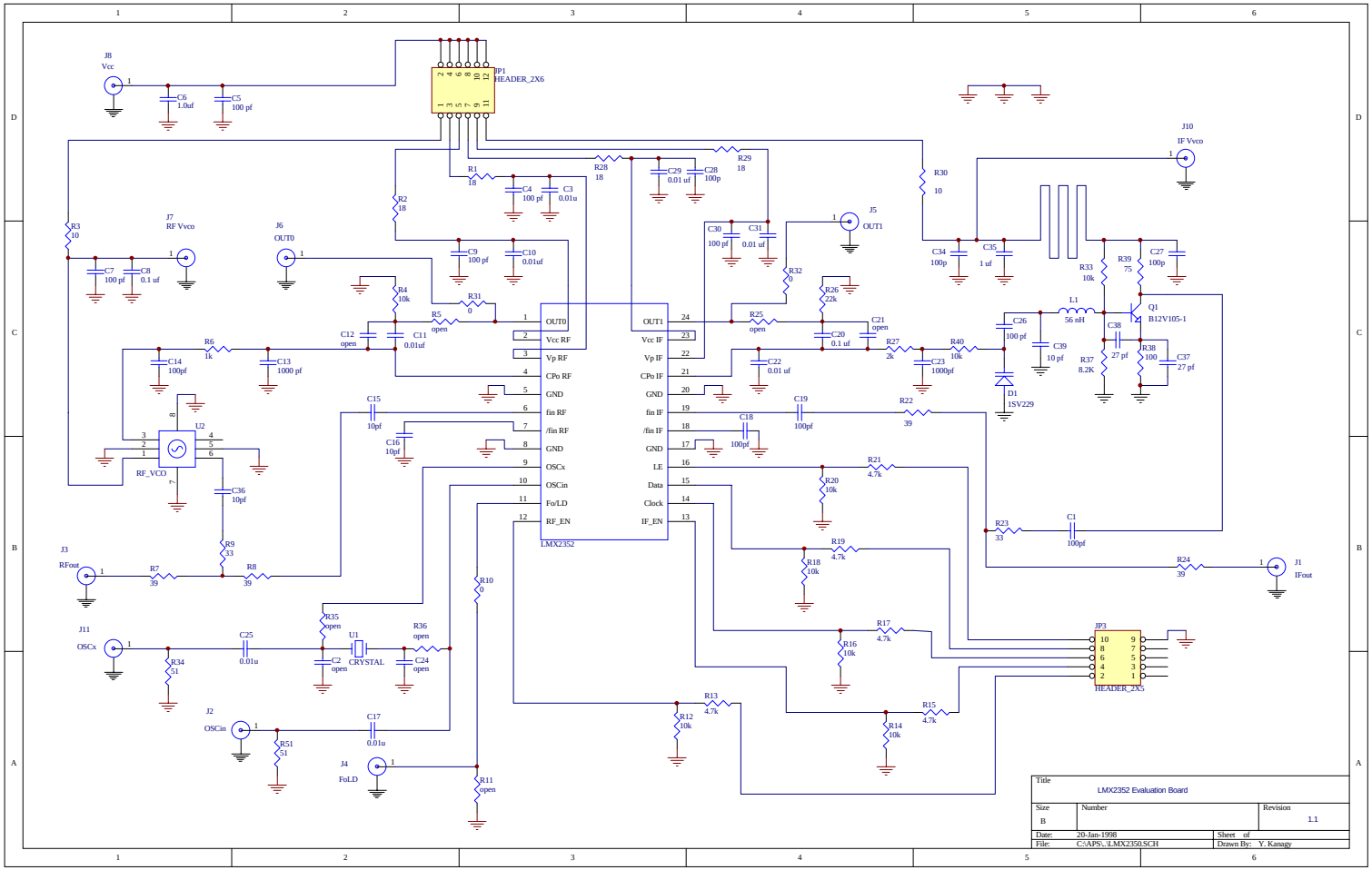
Appendix A - LMX2352 Evaluation Board Schematic Diagram



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Appendix B - LMX2352 Evaluation Board - Bill of Materials

QTY	Description	Location
3	0.01 uf	C3 C17 C25
2	0.1 uf	C8 C20
5	0.01 uf	C10 C11 C22 C29 C31
1	1.0 uf	C6
1	1k	R6
1	1 uf	C35
1	2k	R27
5	4.7k	R13 R15 R17 R19 R21
1	8.2K	R37
2	10	R3 R30
8	10k	R4 R12 R14 R16 R18 R20 R33 R40
4	10pf	C15 C16 C36 C39
4	18	R1 R2 R28 R29
1	22k	R26
2	27 pf	C37 C38
2	33	R9 R23
4	39	R7 R8 R22 R24
2	51	R34 R51
1	56 nH	L1
1	75	R39
1	100	R38
13	100 pf	C27 C28 C34 C1 C4 C5 C7 C9 C14 C18 C19 C26 C30
2	1000 pf	C13 C23
1	1SV229	D1
1	B12V105-1	Q1
1	CRYSTAL	U1
1	FoLD	J4
1	HEADER_2X5	JP3
1	HEADER_2X6	JP1
1	IF Vvco	J10
1	LMX2352	LMX2352
1	Varil1960 VCO	U2
1	Surface mount Header 0.100" X 0.100" Double Row, 5 position	
1	Surface mount Header 0.100" X 0.100" Double Row, 6 position	
6	Shunts 0.100" Doublewipe contacts	
4	SMA PC Mount End Launch Jack Receptacles for Rfout, OSCin, IFout, and Vcc.	

VCO Supplier:

Varil

11101 East 51st Ave.
Denver, Co. 80239
Phone (303) 371-1560
Fax (303) 371-0845

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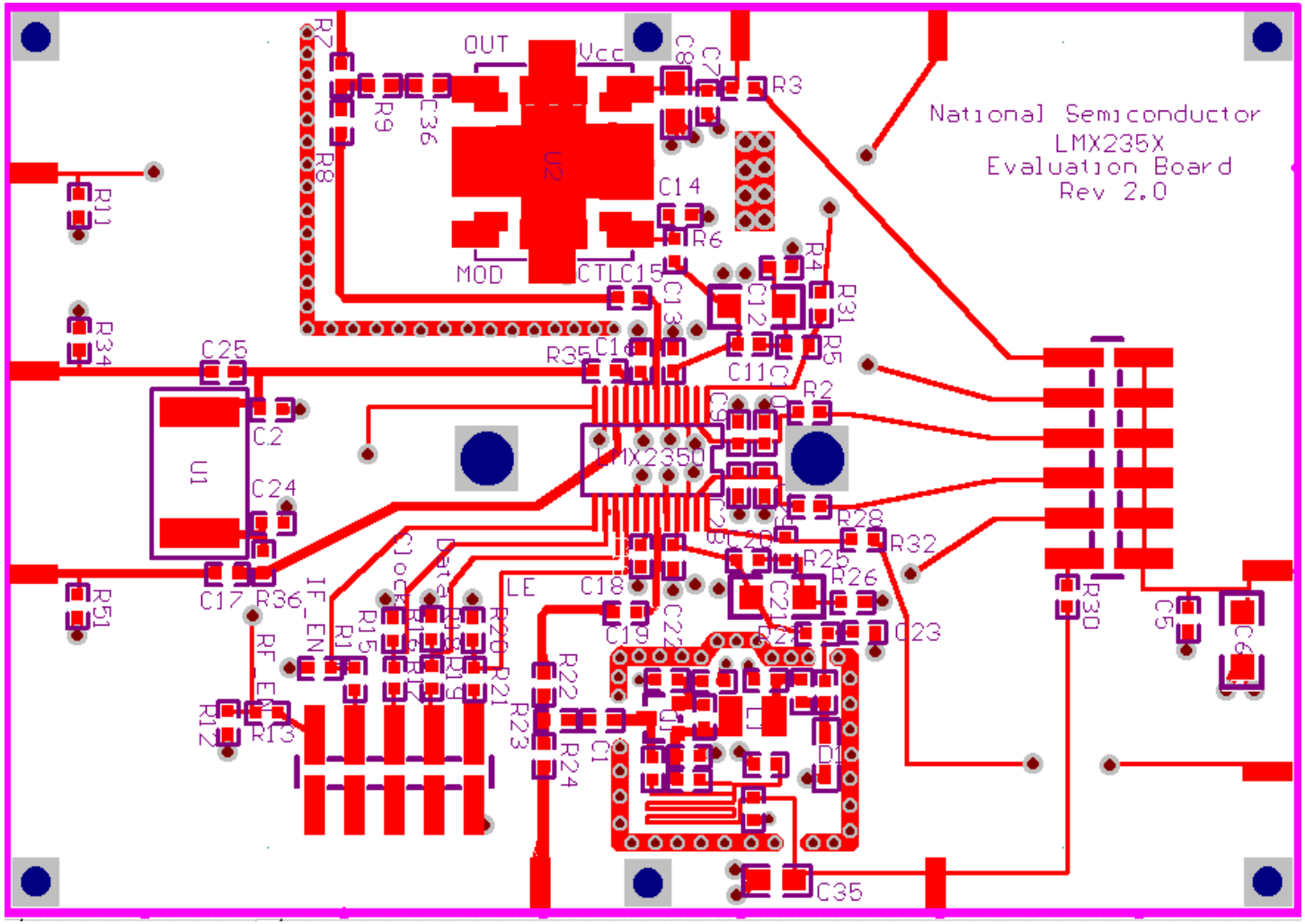
Appendix C - LMX2352 Evaluation Board Layout



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Appendix D - How To Setup Code Loader Software

The LMX2352 Evaluation board is designed so that the port setup is required to be configured as follows except for the **Port Address**. The **Port Address** should be selected according to the user PC parallel port.

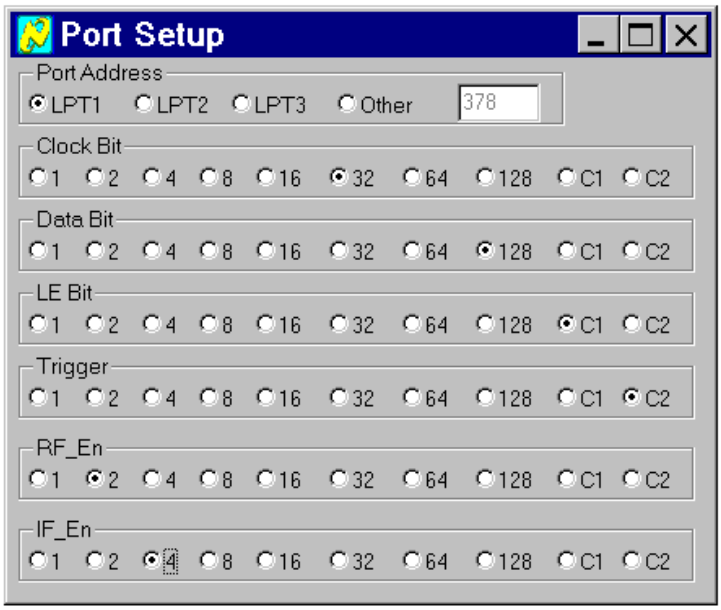

Figure D-1: Port setup for LMX2352

Appendix E - LMX2352 Code Loader Quick Reference

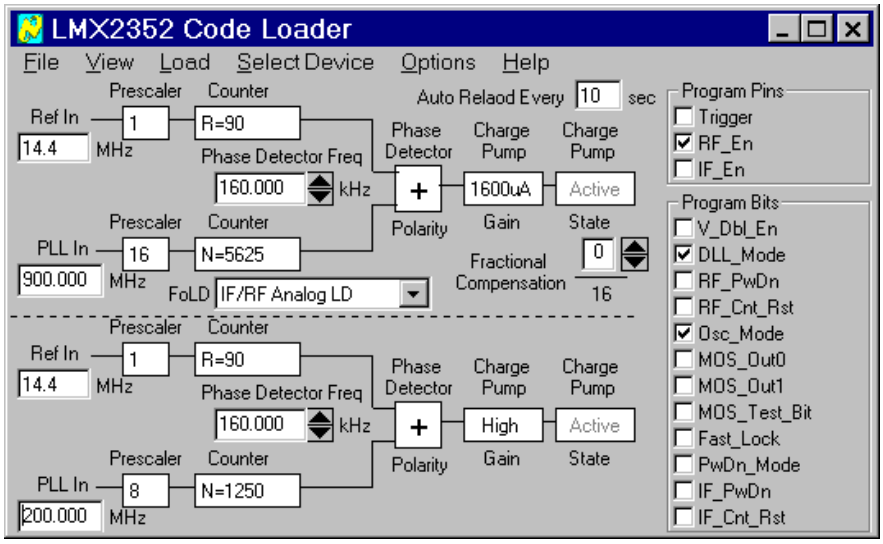

Figure E-1: "Code loader" main menu for LMX2352

The parameters above the dotted line are for the main PLL (RF PLL) and the parameters below the dotted line are for the auxiliary (IF PLL) in the main menu. All parameter values or states can be changed except the charge pump states and R counter prescalers. The parameter boxes can be changed by just clicking on or by clicking on and entering new values. The user must press **Enter** on the keyboard after the parameters are changed. Only registers for which the new changes are relevant are loaded when **Enter** is pressed. To load all registers in both RF and IF PLLs, select the **Load - PLL** pull down menu or enter Ctrl + L.

Ref In - TCXO or reference crystal oscillator input. NSC's normal LMX2352 evaluation board is designed for a 14.4 MHz TCXO. The RF and IF Ref In frequencies are required to be the same. The user is advised to use a high quality crystal reference (i.e. TCXO) for an accurate and low noise measurement.

Phase Detector - Phase detector (comparator) frequency. NSC's normal LMX2352 evaluation boards are designed for a 160 kHz **RF** PLL phase detector frequency and a 200 kHz **IF** PLL phase detector frequency. The component values of the loop filter require redesign if the user wishes to use other phase detector frequencies.

PLL In - VCO output frequency (PLL fin input frequency). Operating frequencies for the **RF** VCO's used on NSC's normal LMX2352 evaluation boards are as follows:

	VCO used	Operating frequency range [MHz]
LMX2352	Varil 2549	890 - 915

The **IF** tuning frequency range is noted at the bottom of the evaluation board or on the code loader diskette label. It is usually around 200 MHz.

The user is allowed to enter a frequency within the VCO operating frequency range. The component values of the loop filter should be redesigned if the user wishes to use other VCOs.

Prescale - Prescaler value of the counters. There is no prescaler used in the R counter indicated by 1. Available RF prescaler values for N divider are 16 and 8. The prescaler 16 should be used for the RF VCO tuning frequency between 0.5 and 1.2 GHz, and the prescaler 8 should be used for the RF VCO tuning frequency between 0.25 and 0.5 GHz. Only the prescaler of 8 is available for IF N divider. The prescaler value can be changed by clicking on the **Prescale** box.

Phase Detector Polarity - The polarity can be changed by clicking on the "+" or "-". Refer to the datasheet for the description of this function.

Charge Pump Gain - Charge pump output current. The LMX2352 have sixteen levels of charge pump gain modes. The modes can be changed by clicking on the charge pump gain current value. The LMX2352 evaluation board loop filter values are designed for 1600 uA mode.

Auto Reload Every [XX] sec - Time interval the program reloads all the counters. The user enables the reload function by selecting **Options - Auto Reload** from the pull down menu.

Fractional Compensation - The fractional compensation value can be changed by toggling the up-down button next to the nominator and the denominator 15 or 16. The NSC normal evaluation board is designed for 1/16.

Program Pins - Trigger - External Trigger for the programming port. The programming port assigned for **Trigger** becomes high when selected and port goes low when not selected.

Program Pins - RF_En - RF Enable pin. The RF PLL is enabled when it is selected.

Program Pins - IF_En - IF Enable pin. The IF PLL is enabled when it is selected.

FoLD - FoLD pin output mode selection. Refer to the databook for a description of the FoLD output selections.

Program Bits - Refer to the detasheet for the function of each programming mode. The codeloader program bits names which are different from the datasheet programming bits names are as follows.

V_Dbl_En = V2_EN

RF_PwDn = PWDN_RF

Osc_Mode = OSC

MOS_Out0 = OUT0

MOS_Out1 = Out1

MOS_Test_Bit = TEST

IF_PwDn = PWDN_IF

The **OSC_Mode** and **DLL_Mode** should be selected when the NSC's normal evaluation boards is evaluated.