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OPERATING INSTRUCTIONS FOR THE NATIONAL SEMICONDUCTOR LMX2335L EVALUATION BOARD

SET-UP INSTRUCTIONS

The LMX2335L Evaluation Board is an implementation of the schematic shown as Figure 4. The board, shown in Figure 5, consists of the LMX2335L, modular RF1 and RF2 VCOs and their respective loop filters.

Resistors denoted as O.C. / S.C. are for connecting various outputs to output pads or to ground by using O Ω resistors as shorts. The board has two kinds of interconnections. SMA flange mount connectors are supplied for the external reference and VCO output, power supply biasing and grounding. A four pin header allows VCC, VP, and Vvco to be driven off either a single voltage supply, or separately. The cable provided connects to the evaluation board pin header and the parallel port of a PC XT (or better) equivalent. Since most P.C.'s parallel port output level is 5 V, pads for resistive dividers on the Clock, Data, and Load Enable are also included. This will allow low voltage operation of the PLL without overdriving the *Microwire* inputs. The power supplies should be connected through the SMA connectors.

The user should make the following connections to operate the evaluation board in standard mode: (1) Connect the RF1 or RF2 VCO output, (or both)**VCO OUT,** to a spectrum analyzer, (2) Connect a reference input from 5 MHz to 40 MHz at 0 dBm to the **REF IN** port, a 50 ohm termination is already on the board for using an external signal generator. (3) Connect the cable assembly to the parallel port of the PC and to the 6 pin header on the evaluation board. Connect the power supplies to the appropriate biasing (3.3V) using the SMA connectors and shorting bars on the pin headers (see schematic). Connect the cable with the arrow on the connector facing the board. If you were holding the cable in your hand the sockets to the far left should attach to the pins on the board. The board is now ready to operate. This configuration is for evaluation purposes only and is not meant show how it will be used in a system. The Loop values for the 2 integrators have been selected and placed in the loop in the configurations shown below. The loop filters were designed for a narrow loop filter bandwidth < 500 Hz in the 1mA mode. The phase detector comparison frequency of 30 kHz to 31.25 kHz (31.25 kHz to allow use of a 10 Mhz crystal frequency) was used. The VCO tuning constant, Kvco, is approximately 35 MHz/V. The evaluation board has been designed to accept more complex configurations.

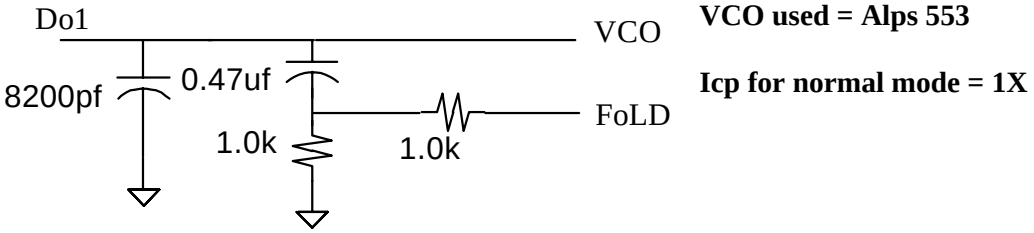
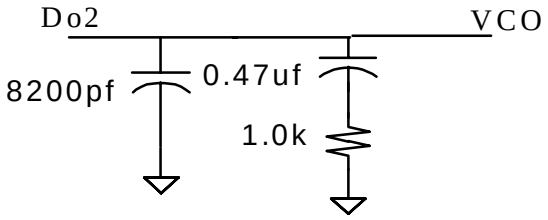


Figure 1: RF1 LOOP FILTER

The resistor R2' is connected to the FoLD output in the RF1 loop filter in order to allow the use of the Fastlock™ feature of the LMX2335L. If the user desires to use the FoLD pin to monitor one of the divider or lock detect outputs, this resistor must be removed. When the FoLD pin is disabled it is resides in a low logic state.



VCO used = Alps 553

Icp for normal mode = 1X

Figure 2: RF2 LOOP FILTER

Fastlock Circuit Implementation

A diagram of the Fastlock scheme as implemented in National Semiconductors LMX2335L PLL is shown in Figure 3. When a new frequency is loaded, the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second R2 resistor element to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the PLL will then return to standard, low noise operation. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between Fastlock and standard mode.

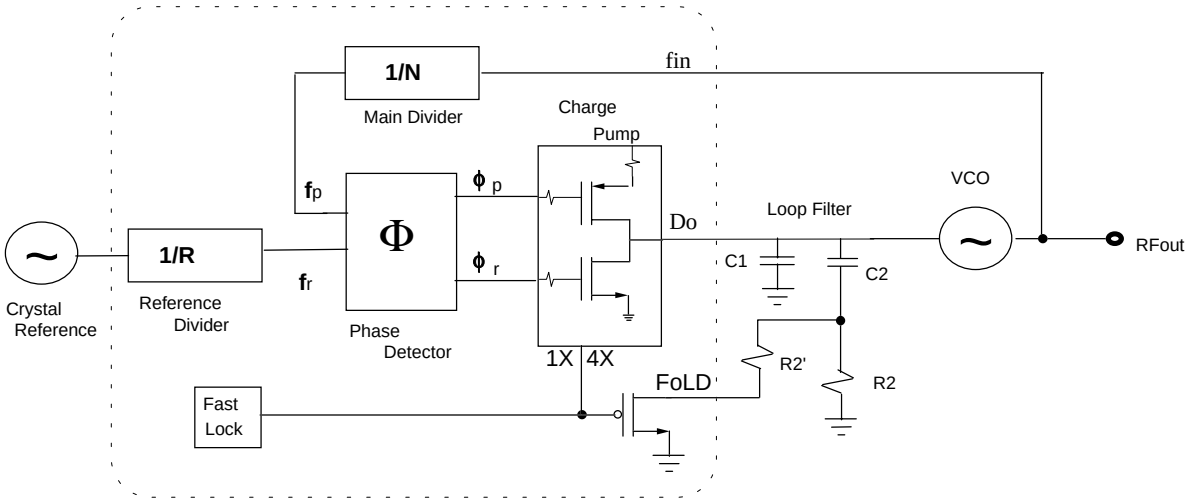


Figure 3 Fastlock PLL Architecture

USING LMX2335L SOFTWARE

Insert the diskette into drive a: or b:. The program may be operated from the floppy or may be copied onto a hard disk. Because the program uses extended precision real numbers in its calculations the program may not operate on some older DOS computers. A PC-AT or equivalent is recommended. The program may be started by typing LMX2335L.

The LMX2335L evaluation program controls the LMX2335L Evaluation Board via a standard parallel port. A cable is provided to make the connection from the computer to the board. The program is intended to be easy to install and use, exercise the PLL, and demonstrate typical performance. It is not intended to be representative of the control code which the customer will implement within their application.

Upon power-up the program will detect the number and location of parallel ports available to the system. The user will be prompted to select one port. The evaluation program is menu driven. All menu selections may be made by pressing "Enter" when a menu is highlighted. Up, down, left and right arrows are used to change which menu id highlighted. Speed keys are also included for each active menu item. Use Speed keys by typing the letter displayed in red corresponding to the mode desired. The top menu pane consists of pull down menus titled "Set (F)requency", "Set (R)egister", "(T)uning", "(M)odes", "Fo/(L)D", and "(Q)uit" where the speed keys are listed in parentheses. To exit from a menu at anytime press "Escape". A status pane is included at the bottom of the pane to give on-line help descriptions of highlighted menu items.

The program displays a block showing the present tuning parameters for VCO, Crystal Reference, and Phase detector reference frequency for the RF1 PLL. To display and edit the second PLL select "RF2 P(L)L" under the "Modes" pulldown menu. Activate the "Set Frequency" pulldown menu to control these values. To the right of this block is the "Scratchpad", showing the values as you enter them. The program will issue a warning and a suggestion if a value is selected which does not maintain an integer relationship between the VCO or crystal frequency and the reference frequency. The suggestion will be the nearest value of the parameter just changed which will produce an integer relationship. The user may select this value, or any other, so long as the integer relationship is established.

Upon successful selection of tuning parameters, the download values are calculated and loaded. The board must be powered up in order for the values to be loaded. If power is applied after the software is on or power is turned off for some reason all that is required is entering "Load Dual PLL" to download the values for both PLL's.

The program displays, and allows modification of, the binary values for the VCO divider (P), Reference Divider(R), and control codes. The value of P (either 64 or 128) shows the present status of the prescaler control bit which enables either the 64/65 prescaler or the 128/129 prescaler. When an N value is entered which is invalid for P=64, the program will display an error message and automatically switch to P=128. To modify N, R or P directly, activate the "Set Register" menu, select the desired mode and use the arrow keys to move horizontally or to change values ("up" changes "0" to "1", "down" changes "1" to "0"). You may also type in "1" or "0".

Users will find items in the "Tuning" menu useful. In "Hand Tune" mode the user may step up or down in single increments by using the up or down arrows, or in increments of 10 by using the left and right arrows. Other steps, 2 up to 9, are taken by pressing any number from 2 to 9. Steps downward are taken by pressing the down or left arrow keys or by holding down the shift key when pressing any number from 2 to 9.

The "Switch" mode in the "Tuning" menu allows measurement of PLL switching time by initiating switching between the presently tuned frequency and a frequency an arbitrary number of steps away. In "Switch" mode, the user will be prompted for an integer (+ or -) number of steps and a delay (msec). The delay will allow the user to specify the time delay between switching. The "Enable" input forms a fairly good trigger (it is written twice, once for N and once for R). Load time will vary depending upon the processing speed of the computer being used.

The "Auto Tune" mode in the "Tuning" menu allows the user to switch to a set frequency and specify the interval to step in. Entering this mode, the user will be prompted for an integer to step up to, an integer to step by and a delay (msec). The delay allows the user to specify the time delay between steps. This would allow a user to verify operation at all channels of interest.

The "Modes" menu is used to toggle the PLL between different states. The menu items are interactive and change with the state of the PLL. Choosing the first menu item (either "RF2 PLL" or "RF1 PLL") switches the active display from the RF1 PLL to the RF2 PLL, or vice versa. The second menu item toggles the slope of the phase detector between "PD = Positive" and "PD = Negative". "Icp = 1(4) mA" switches between the high and low current charge pump output. The "Power Down (Up)" selection powers down (or up) the currently displayed PLL only. Selecting the last menu item under modes "Do Tri-State (Active)" toggles the PLL charge pump in and out of Tri-State mode.

The "Fo/LD" menu is specifically used to control the state of the frequency divider/ lock detect/ Fastlock output pin. The user may select the Fastlock mode, as well as disable the output, or select one of seven output states which allow monitoring either the R or N divider outputs, or lock detect for each PLL. While selecting Fastlock mode, the user will be prompted for a delay time in milleseconds, and ‘Fastlock’ will appear in the active mode display. Upon using the switching mode with Fastlock activated, the part will stay in the 4mA Fastlock mode with R2’ switched in to ground for the programmed number of milleseconds and then revert to the 1mA mode with the FoLD input a high impedance. Keep in mind the number of milleseconds actually delayed may vary from computer to computer, and is more accurate when the program is run directly from DOS.

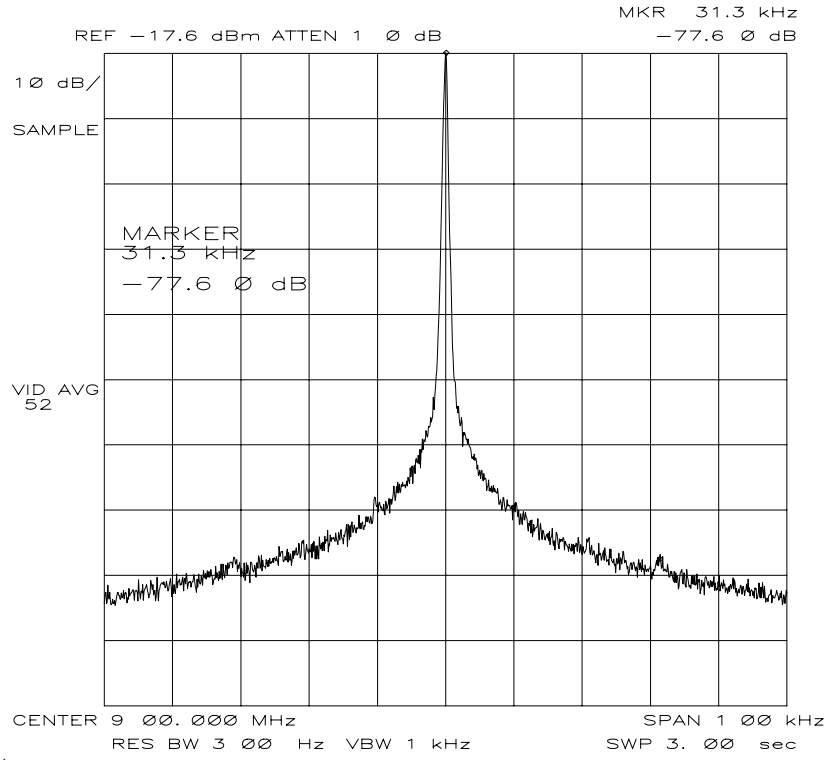
The program is exited by choosing "Yes,Quit" in the "Quit" menu, which saves the current parameters in a log file. Any mode may be exited by pressing "Enter".

TYPICAL MEASURED PERFORMANCE OF THE LMX2335L EVALUATION BOARD

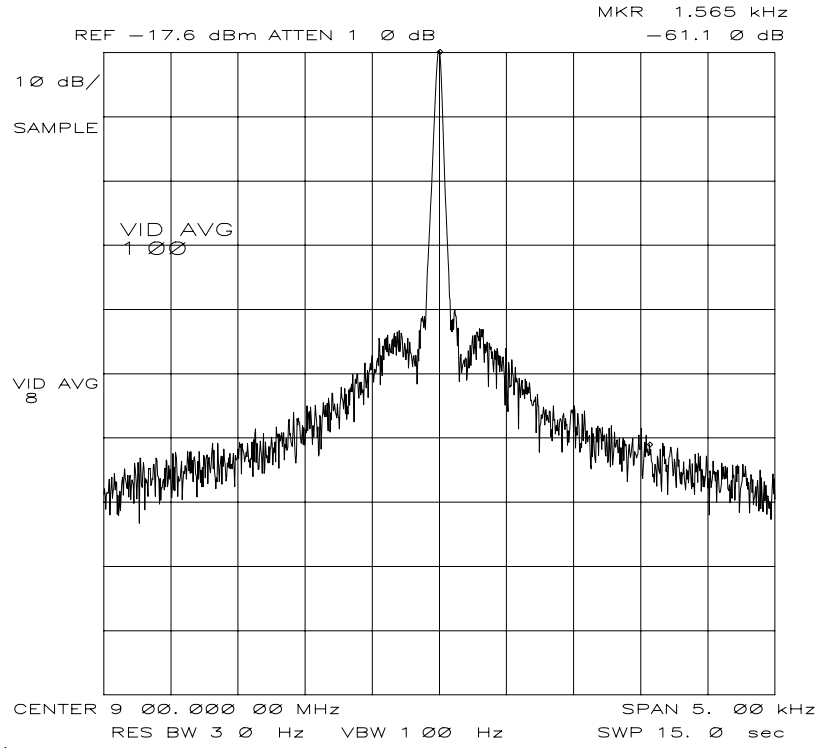
The following figures show typical spectrum plots as well as lock time in the normal mode and Fastlock mode. The lock time for a 50 MHz frequency jump to within 1 kHz in the Icp = 4mA mode with R2 = 500Ω, is shown to be 9.2 msec. With the reduction of loop bandwidth changing Icp = 1mA and R2 = 1k, the lock time increases to 16.4 msec. The phase ‘glitch’ occurring when switching between Fastlock and normal mode has been minimized to less than 2.5 kHz, as seen. By setting the fast lock delay at 8 msec, the transition between Fastlock and normal mode occurs when the loop is ‘almost’ locked. This gives almost the entire reduction in lock time achieved with the wider loop (10.7 msec vs. 9.2 msec), and allows closed loop operation in the narrower loop bandwidth, low noise 1mA mode..

NOTE: Computer monitors and other lab equipment has been shown to cause noise spikes. If you see noise spikes on the signal try turning off the monitor or other equipment to verify that they are not the cause. Also noise may be getting onto the signal through the cable that connects to the parallel port of the computer.

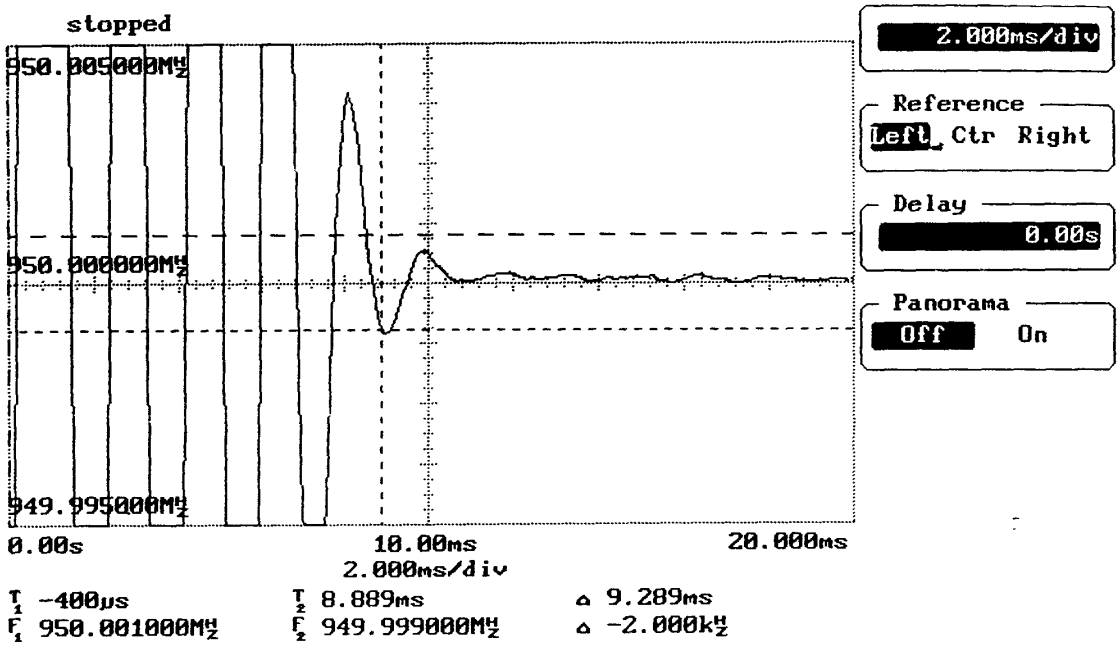
TYPICAL MEASURED DATA



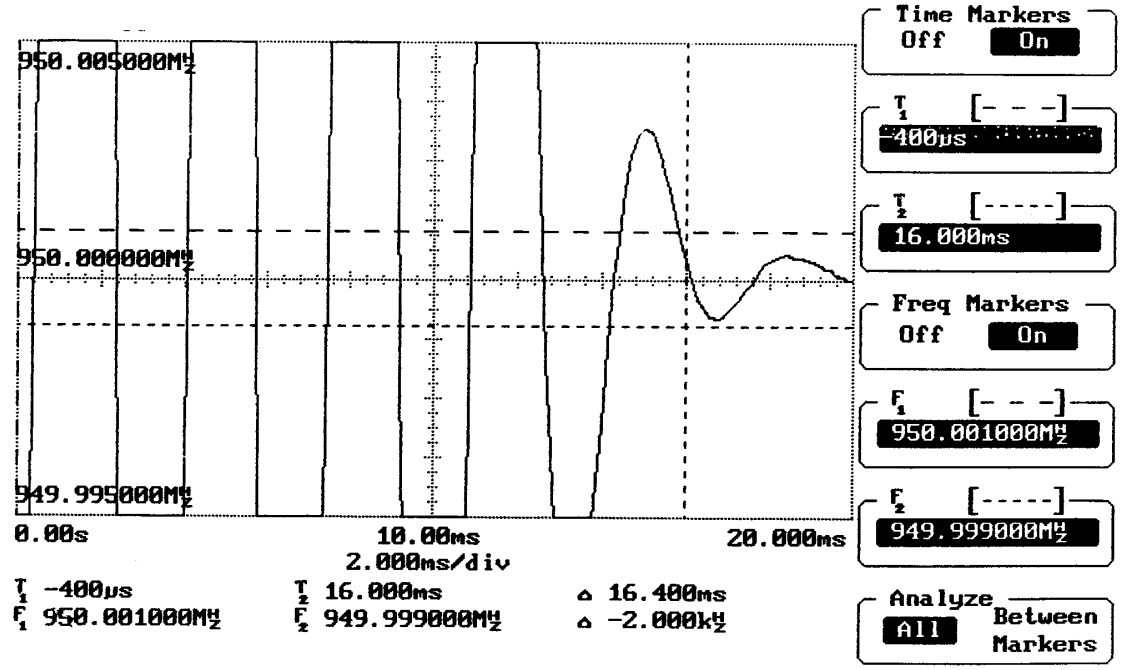
Reference spurs at 31.25 kHz.



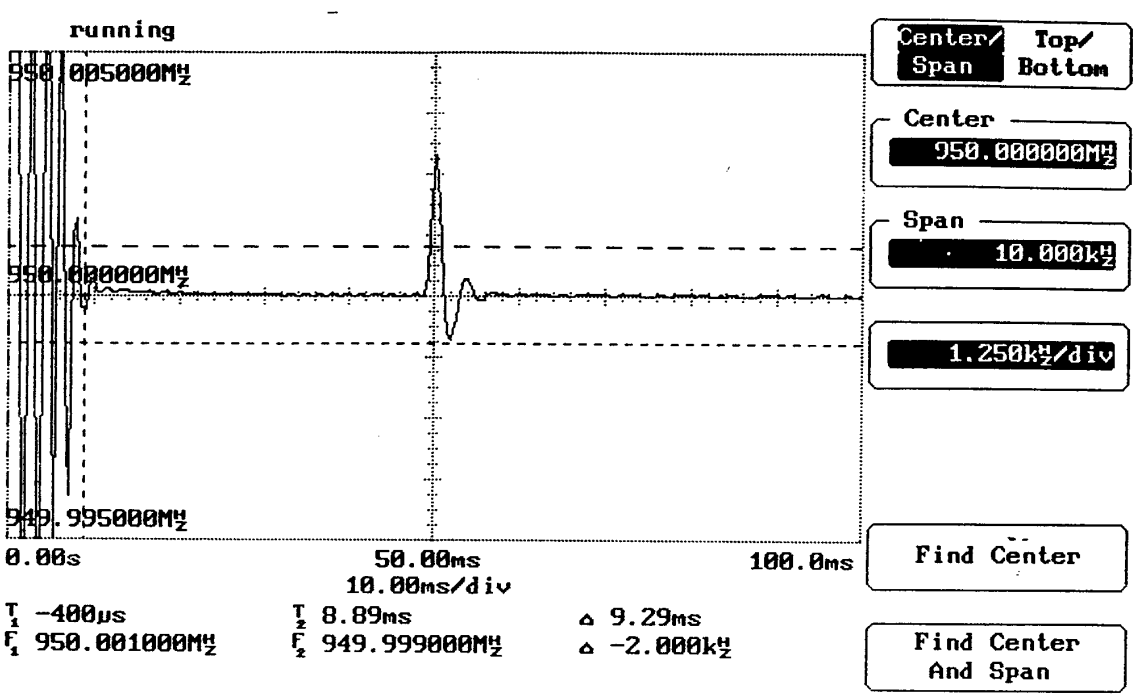
Loop Filter Bandwidth



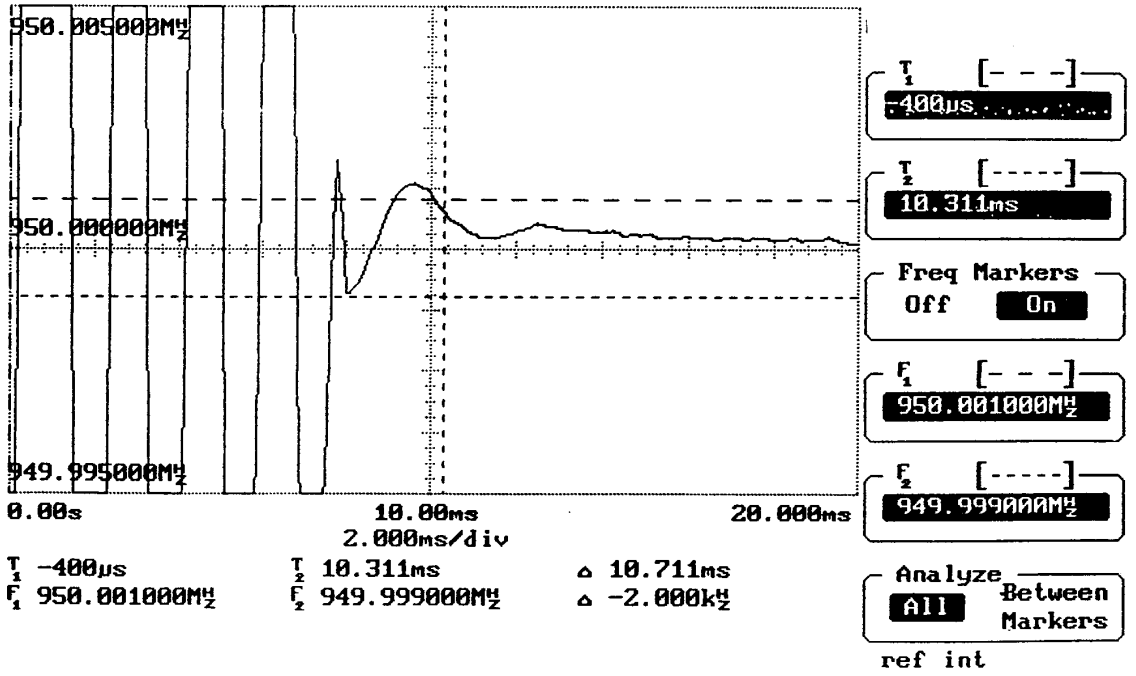
PLL Lock Time Icp = 4 mA, R2 = 500Ω



PLL Lock Time Icp = 1 mA, R2 = 1kΩ



PLL Fastlock mode delay time = 50 msec



PLL Fastlock mode delay time = 8 msec

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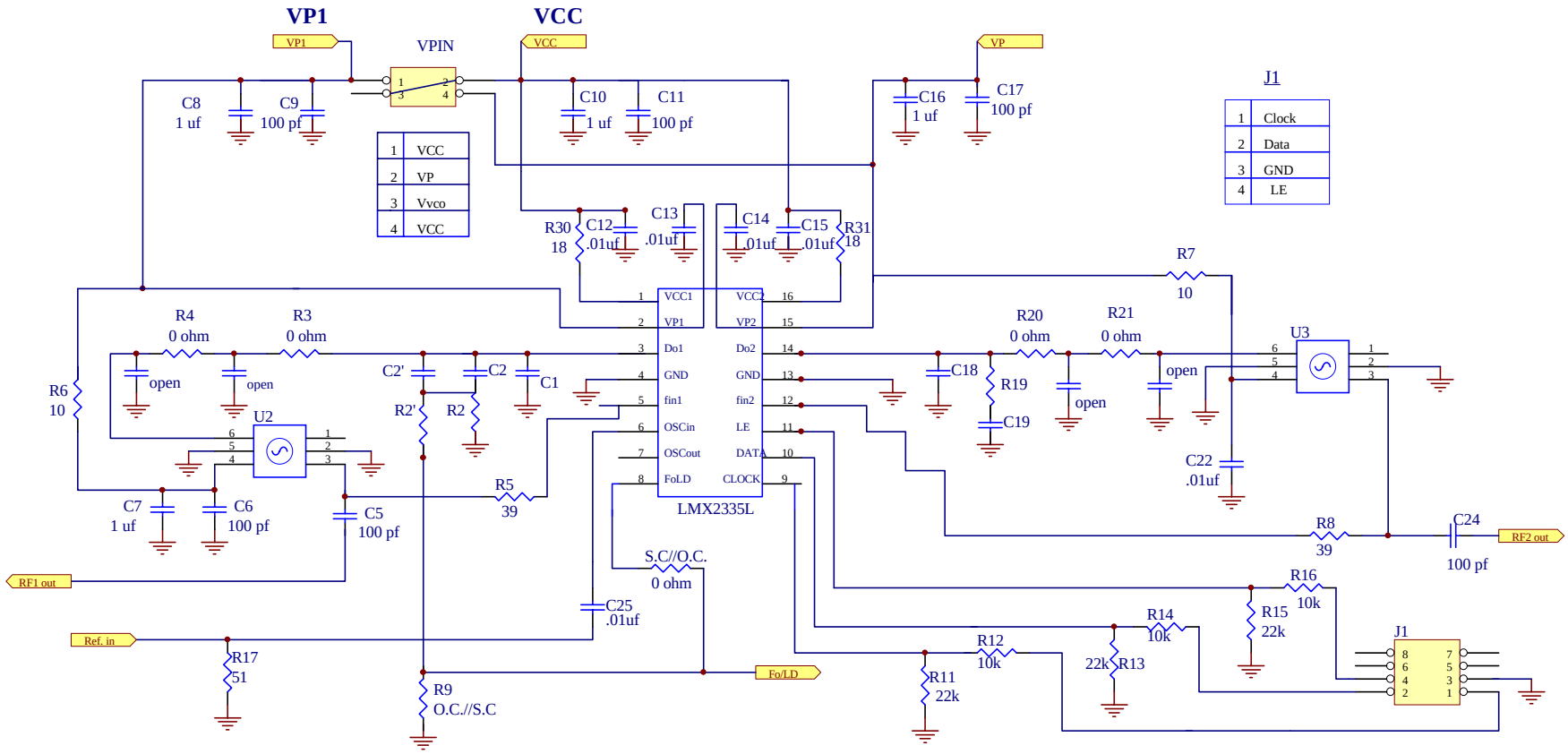
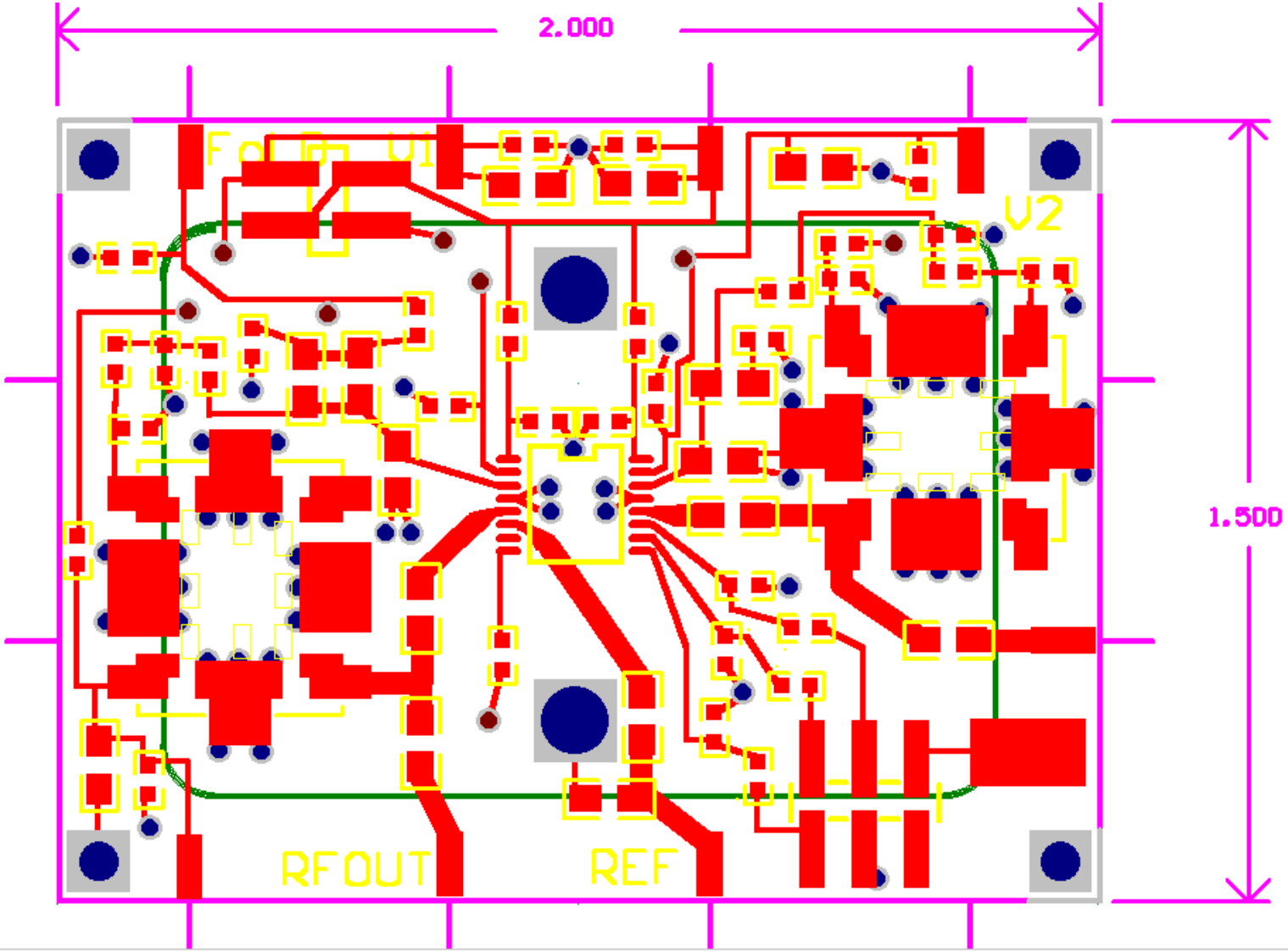
Figure 4 : LMX2335L Evaluation Board Schematic



LMX2335 Evaluation Board

3 volt operation

Figure 5 : LMX2335L Evaluation Board Layout



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LMX2335L Bill of Materials

Part	Used	PartType	Designators
2	6	.01uf	C12 C13 C14 C15 C22 C25
3	2	0.47u	C2 C19
4	5	0 ohm	R3 R4 R20 R21 S.C//O.C.
5	2	1k	R2 R19
6	4	1 uf	C7 C8 C10 C16
7	2	10	R6 R7
8	3	10k	R12 R14 R16
9	2	18	R30 R31
10	3	22k	R11 R13 R15
11	2	39	R5 R8
12	1	51	R17
13	6	100 pf	C5 C6 C9 C11 C17 C24
14	2	8200pf	C1 C18
15	1	LMX2335L	U1
16	1	1k	R2'

October 17, 1997