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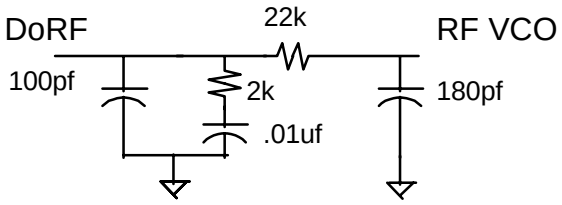
OPERATING INSTRUCTIONS FOR THE NATIONAL SEMICONDUCTOR LMX2330A EVALUATION BOARD

SET-UP INSTRUCTIONS

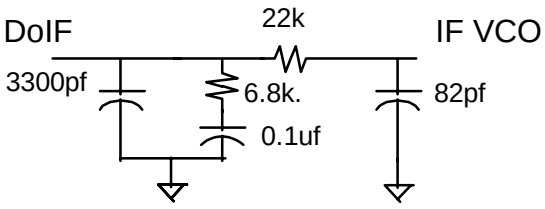
The LMX2330A Evaluation Board is an implementation of the schematic shown as Figure 2. The board, shown in Figure 3, consists of the LMX2330A, a modular RF VCO, a discrete IF VCO and their respective loop filters.

Resistors denoted as O.C. / S.C. are for connecting various outputs to output pads or to ground by using O Ω resistors as shorts. The board has two kinds of interconnections. SMA flange mount connectors are supplied for the external reference and VCO output, power supply biasing and grounding. A four pin header allows VCC, VP, and Vvco to be driven off either a single voltage supply, or separately. The cable provided connects to the evaluation board pin header and the parallel port of a PC XT (or better) equivalent. Since most P.C.'s parallel port output level is 5 V, pads for resistive dividers on the Clock, Data, and Load Enable are also included. This will allow low voltage operation of the PLL without overdriving the *Microwire* inputs. The power supplies should be connected through the SMA connectors.

The user should make the following connections to operate the evaluation board in standard mode: (1) Connect the RF or IF VCO output, (or both)**VCO OUT,** to a spectrum analyzer, (2) Connect a reference input from 5 MHz to 40 MHz at 0 dBm to the **REF IN** port, a 50 ohm termination is already on the board for using an external signal generator. (3) Connect the cable assembly to the parallel port of the PC and to the 6 pin header on the evaluation board. Connect the power supplies to the appropriate biasing (3.3V) using the SMA connectors and shorting bars on the pin headers (see schematic). Connect the cable with the arrow on the connector facing the board. If you were holding the cable in your hand the sockets to the far left should attach to the pins on the board. The board is now ready to operate. This configuration is for evaluation purposes only and is not meant show how it will be used in a system. The Loop values for the 2 integrators have been selected and placed in the loop in the configurations shown below. The loop filters were designed for an RF comparison frequency of 1000 kHz, and an IF comparison frequency of 50 kHz. The evaluation board has been designed to accept more complex configurations. For Fastlock™ operation, add resistor R2' equal to R2 and add a 0Ω resistor for R10.



RF LOOP FILTER



IF LOOP FILTER

Figure 1: Loop Filters

VCO used: Alps 926
Icp=4X mode

USING LMX2330A SOFTWARE

Insert the diskette into drive a: or b:. The program may be operated from the floppy or may be copied onto a hard disk. Because the program uses extended precision real numbers in its calculations the program may not operate on some older DOS computers. A PC-AT or equivalent is recommended. The program may be started by typing LMX2330A.

The LMX2330A evaluation program controls the LMX2330A Evaluation Board via a standard parallel port. A cable is provided to make the connection from the computer to the board. The program is intended to be easy to install and use, exercise the PLL, and demonstrate typical performance. It is not intended to be representative of the control code which the customer will implement within their application.

Upon power-up the program will detect the number and location of parallel ports available to the system. The user will be prompted to select one port. The evaluation program is menu driven. All menu selections may be made by pressing "Enter" when a menu is highlighted. Up, down, left and right arrows are used to change which menu id highlighted. Speed keys are also included for each active menu item. Use Speed keys by typing the letter displayed in red corresponding to the mode desired. The top menu pane consists of pull down menus titled "Set (F)requency", "Set (R)egister", "(T)uning", "(M)odes", "Fo/(L)D", and "(Q)uit" where the speed keys are listed in parentheses. To exit from a menu at anytime press "Escape". A status pane is included at the bottom of the pane to give on-line help descriptions of highlighted menu items.

The program displays a block showing the present tuning parameters for VCO, Crystal Reference, and Phase detector reference frequency for the HIGH frequency PLL. To display and edit the second PLL select "IF P(L)L" under the "Modes" pulldown menu. Activate the "Set Frequency" pulldown menu to control these values. To the right of this block is the "Scratchpad", showing the values as you enter them. The program will issue a warning and a suggestion if a value is selected which does not maintain an integer relationship between the VCO or crystal frequency and the reference frequency. The suggestion will be the nearest value of the parameter just changed which will produce an integer relationship. The user may select this value, or any other, so long as the integer relationship is established.

Upon successful selection of tuning parameters, the download values are calculated and loaded. The board must be powered up in order for the values to be loaded. If power is applied after the software is on or power is turned off for some reason all that is required is entering "Load Dual PLL" to download the values for both PLL's.

The program displays, and allows modification of, the binary values for the VCO divider (P), Reference Divider(R), and control codes. The value of P (either 64 or 128) shows the present status of the prescaler control bit which enables either the 64/65 prescaler or the 128/129 prescaler. When an N value is entered which is invalid for P=64, the program will display an error message and automatically switch to P=128. To modify N, R or P directly, activate the "Set Register" menu, select the desired mode and use the arrow keys to move horizontally or to change values ("up" changes "0" to "1", "down" changes "1" to "0"). You may also type in "1" or "0".

Users will find items in the "Tuning" menu useful. In "Hand Tune" mode the user may step up or down in single increments by using the up or down arrows, or in increments of 10 by using the left and right arrows. Other steps, 2 up to 9, are taken by pressing any number from 2 to 9. Steps downward are taken by pressing the down or left arrow keys or by holding down the shift key when pressing any number from 2 to 9.

The "Switch" mode in the "Tuning" menu allows measurement of PLL switching time by initiating switching between the presently tuned frequency and a frequency an arbitrary number of steps away. In "Switch" mode, the user will be prompted for an integer (+ or -) number of steps and a delay (msec). The delay will allow the user to specify the time delay between switching. The "Enable" input forms a fairly good trigger (it is written twice, once for N and once for R). Load time will vary depending upon the processing speed of the computer being used.

The "Auto Tune" mode in the "Tuning" menu allows the user to switch to a set frequency and specify the interval to step in. Entering this mode, the user will be prompted for an integer to step up to, an integer to step by and a delay (msec). The delay allows the user to specify the time delay between steps. This would allow a user to verify operation at all channels of interest.

The "Modes" menu is used to toggle the PLL between different states. The menu items are interactive and change with the state of the PLL. Choosing the first menu item (either "IF PLL" or "RF PLL") switches the active display from the High Frequency PLL to the Low Frequency PLL, or vice versa. The second menu item toggles the slope of the phase detector between "PD = Positive" and "PD = Negative". "Icp = 1(4) mA" switches between the high and low current charge pump output. The "Power Down (Up)" selection powers down (or up) the currently displayed PLL only. Selecting the last menu item under modes "Do Tri-State (Active)" toggles the PLL charge pump in and out of Tri-State mode.

The "Fo/LD" menu is specifically used to control the state of the frequency divider/ lock detect/ Fastlock output pin. The user may select the Fastlock mode, as well as disable the output, or select one of seven output states which allow monitoring either the R or N divider outputs, or lock detect for each PLL. While selecting Fastlock mode, the user will be pompted for a delay time in milleseconds, and ‘Fastlock’ will appear in the active mode display. Upon using the switching mode with Fastlock activated, the part will stay in the 4mA Fastlock mode with R2’ switched in to ground for the programmed number of milleseconds and then revert to the 1mA mode with the FoLD input a high impedance. Keep in mind the number of milleseconds actually delayed may vary from computer to computer, and is more accurate when the program is run directly from DOS.

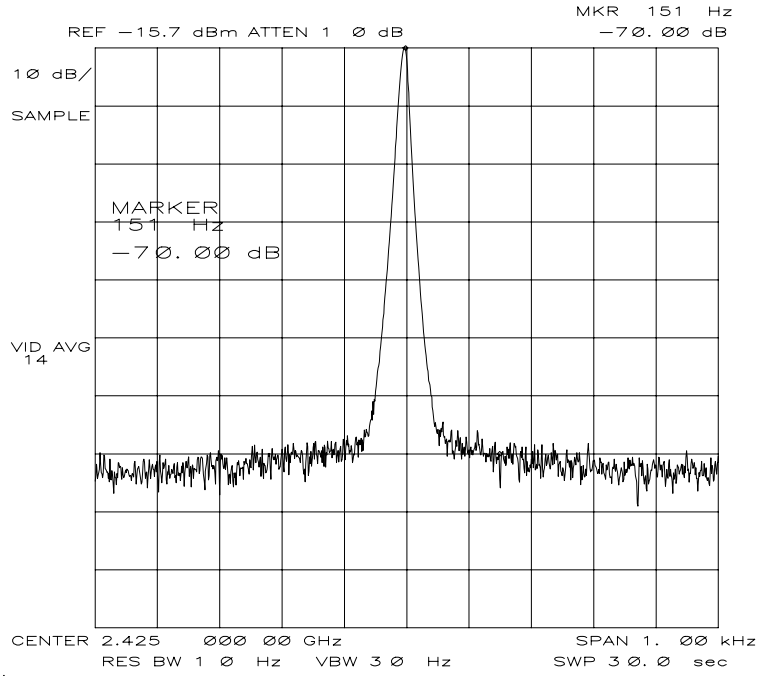
The program is exited by choosing "Yes,Quit" in the "Quit" menu, which saves the current parameters in a log file. Any mode may be exited by pressing "Enter".

TYPICAL MEASURED PERFORMANCE OF THE LMX2330A EVALUATION BOARD

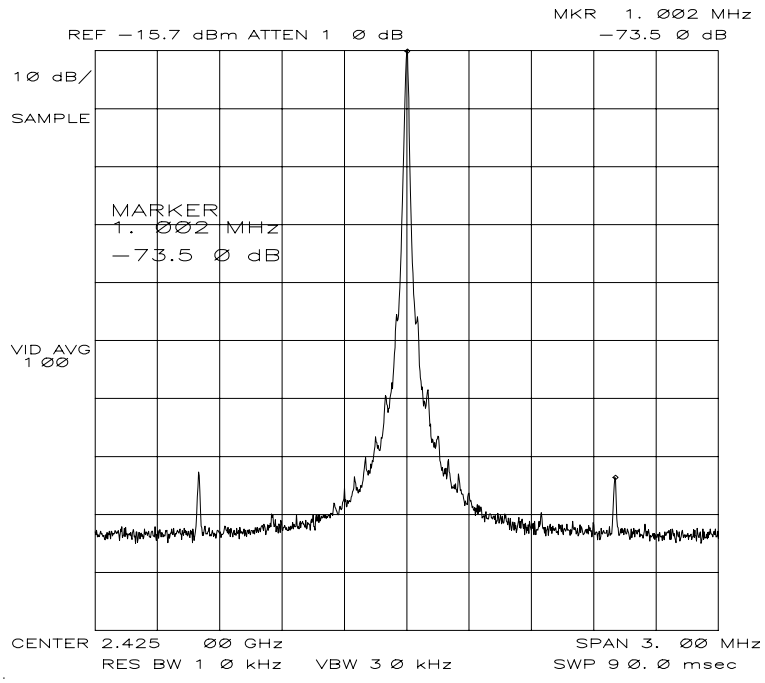
Normal operating parameters for the RF PLL include spurious at less than -70 dBc, switching speed (for a 200 kHz reference frequency and a step of 50 MHz to within a frequency error of 1 kHz) < 750 microseconds. Phase noise is under -70 dBc/Hz at 1 kHz offset. Noise at 100 kHz is under -110 dBc/Hz. The VCO operating voltages are 3V. The high frequency VCO tunes over a frequency range of 2.40 to 2.45 GHz, while the low frequency VCO has a frequency range of approximately 230 MHz to 238 MHz. Typical current draw at 3 volts is 13 mA (not including the 7 mA VCO). These parameters were measured on a very small sample size. All parameters are subject to change.

NOTE: Computer monitors and other lab equipment has been shown to cause noise spikes. If you see noise spikes on the signal try turning off the monitor or other equipment to verify that they are not the cause. Also noise may be getting onto the signal through the cable that connects to the parallel port of the computer.

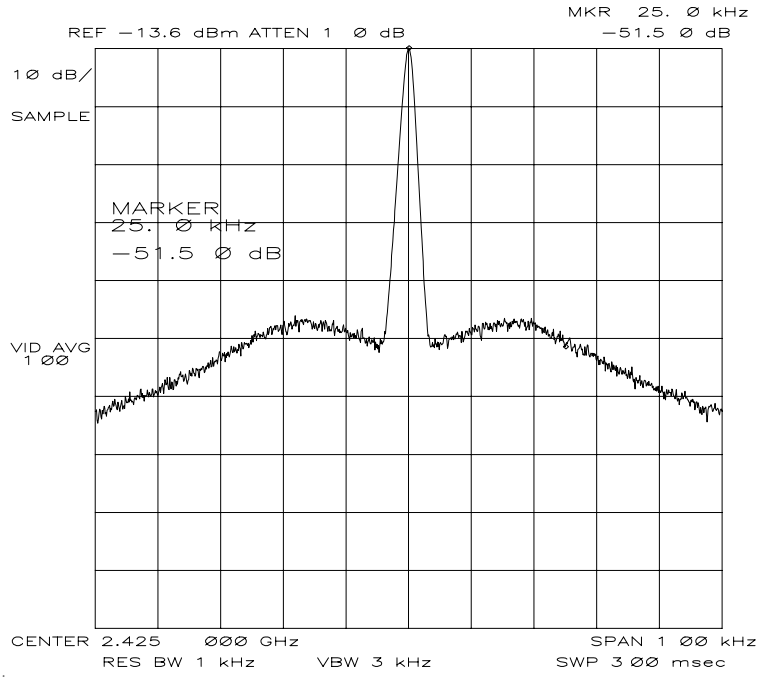
TYPICAL MEASURED DATA



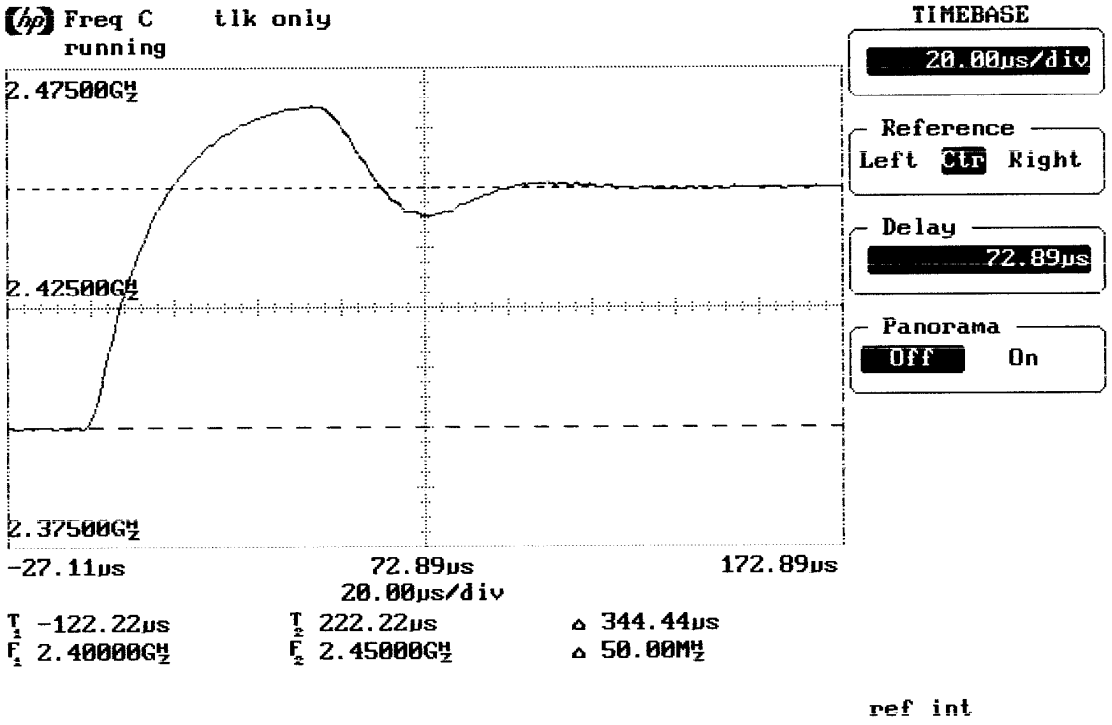
“Close in” Phase Noise



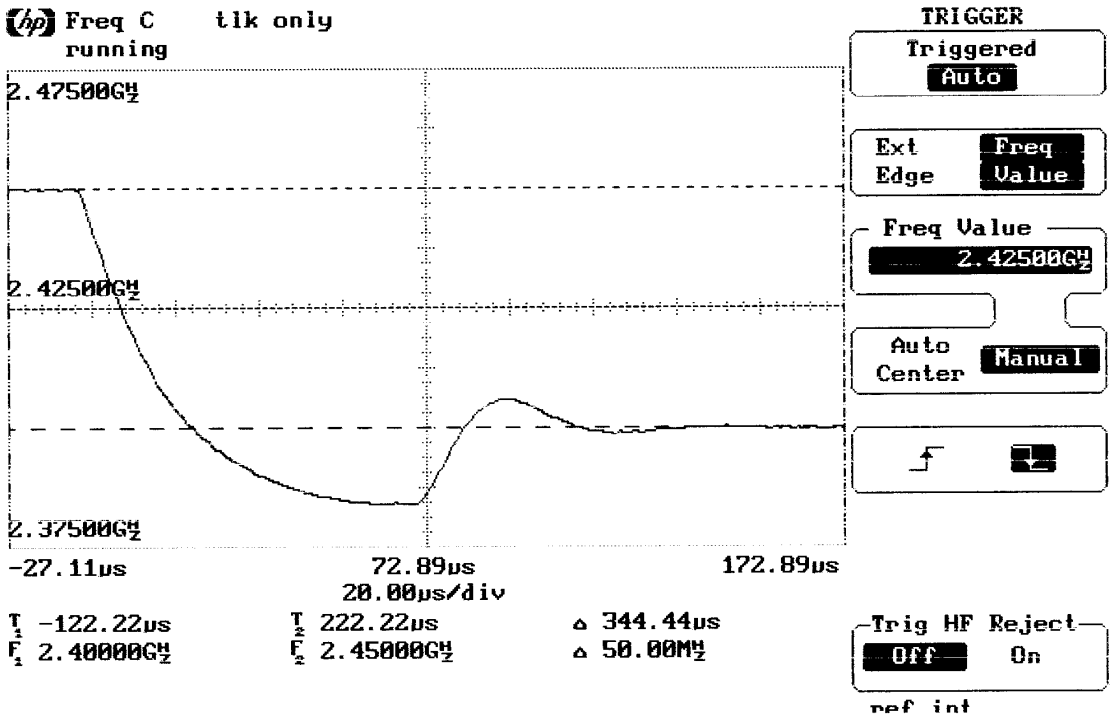
Reference Spurs



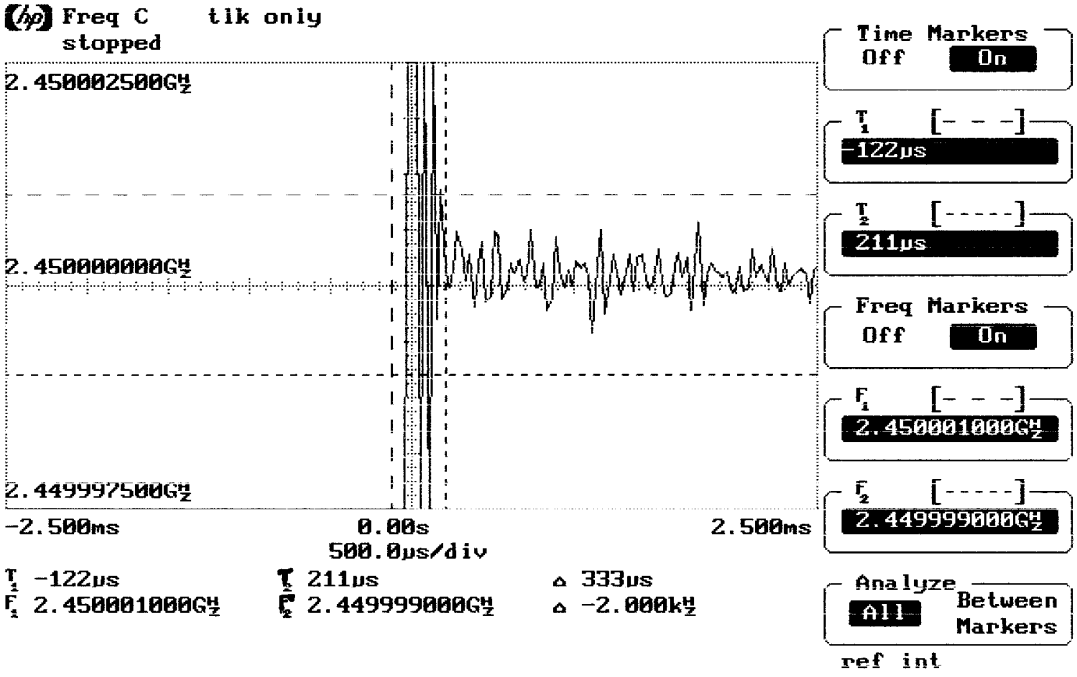
Loop Bandwidth



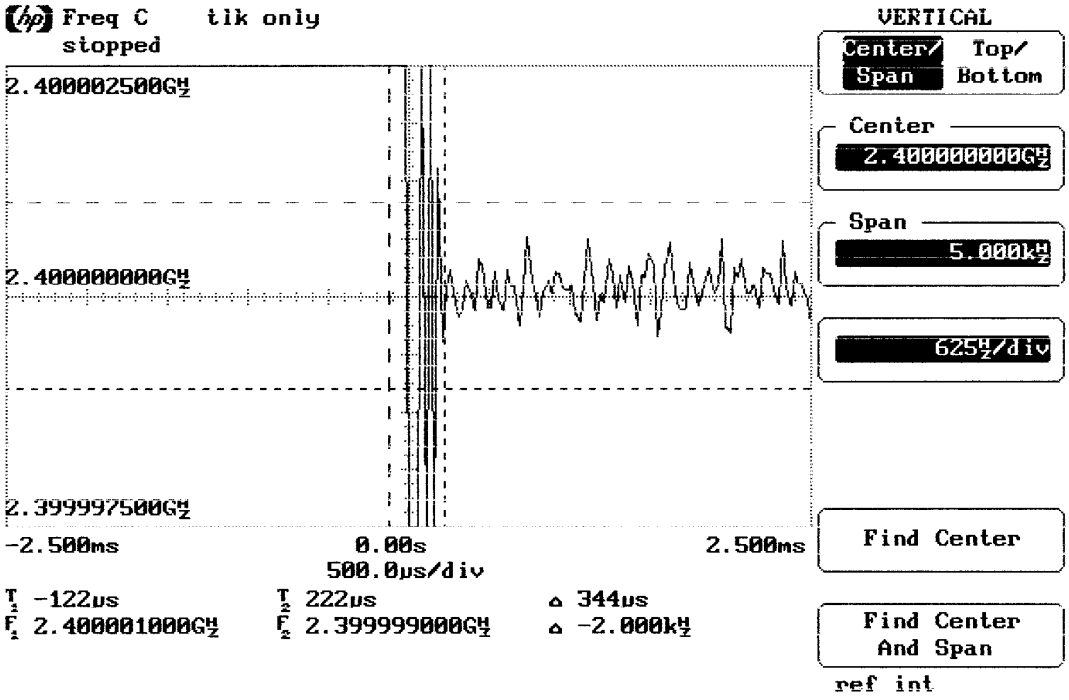
Positive Frequency Switching Waveform



Negative Frequency Switching Waveform



PositiveLock Time to within 1 kHz



Negative Lock Time to within 1kHz

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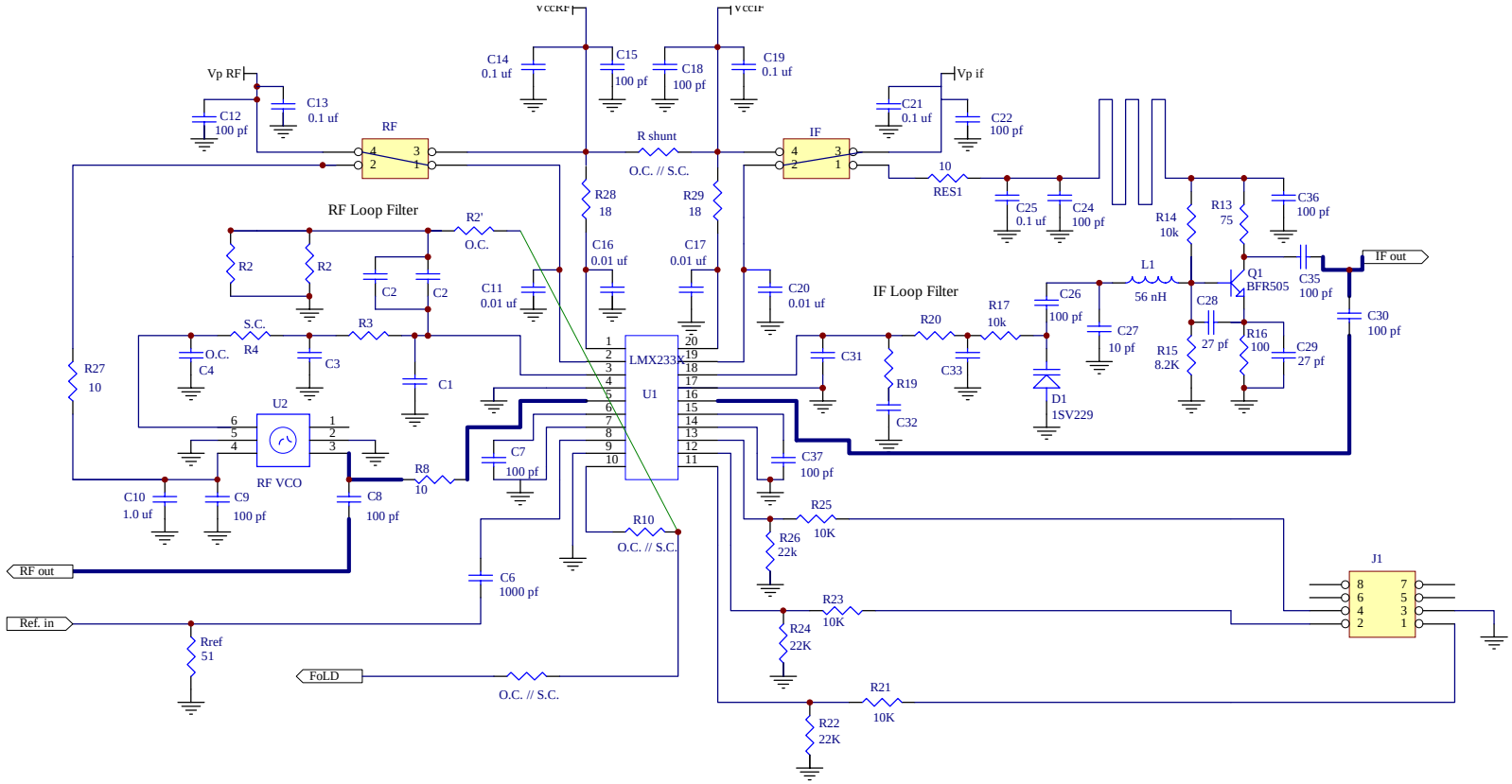
Figure 2: LMX2330A Evaluation Board Schematic



Dual PLL (20 Pin) Evaluation Board (3 Volt Operation)

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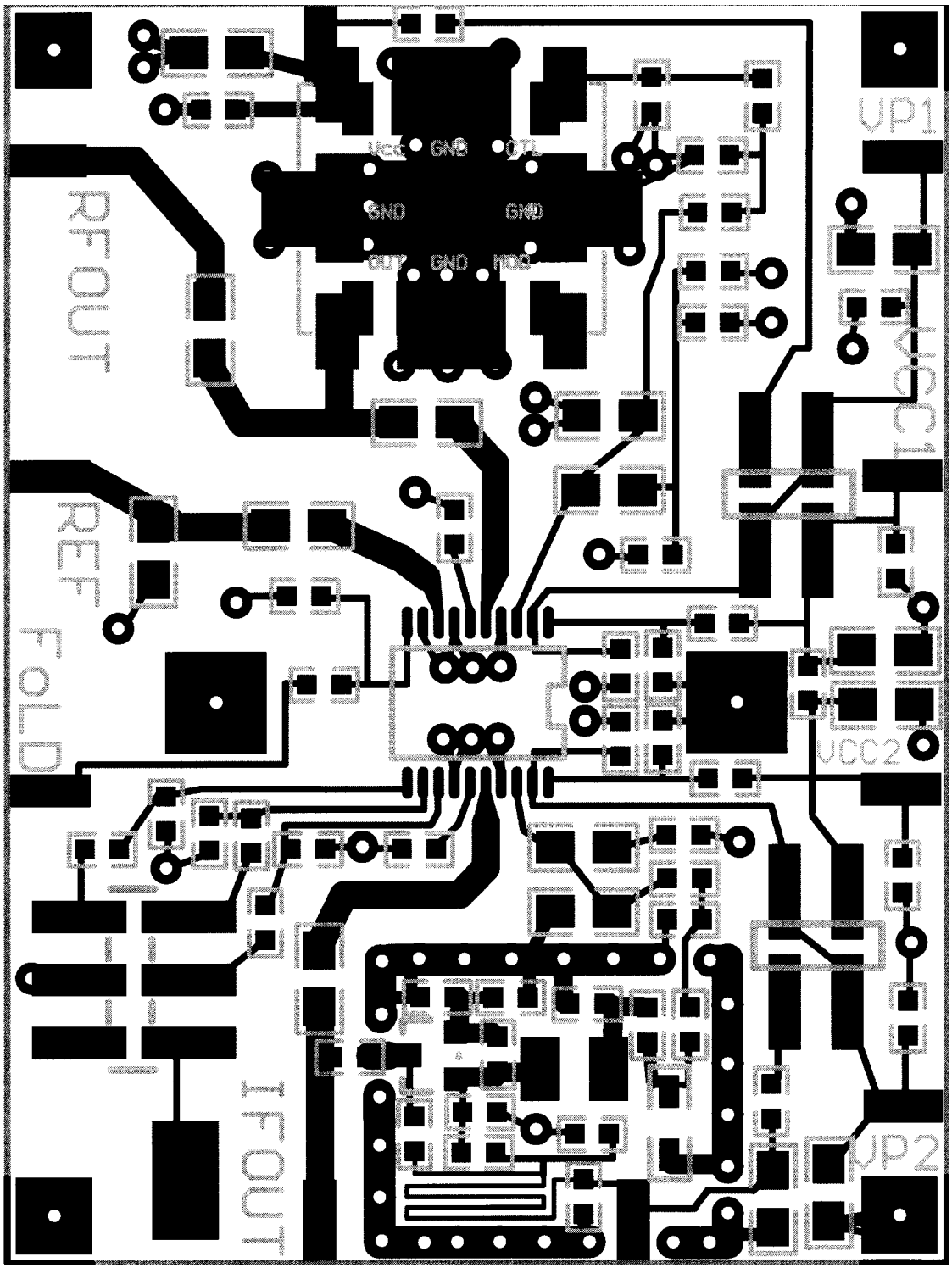
Figure 3: LMX2330A Evaluation Board Layout



LMX2330A Bill of Materials

Part	Used	PartType	Designators
1	5		C3 IF J1 R2' RF
2	1	.1uf	C32
3	5	0.01 uf	C1, C11, C16, C17, C20
4	1	0 ohm	R4
5	6	1uf	C10, C13, C14, C19, C21, C25
6	1	6.8K	R19
7	1	8.2K	R15
8	2	10	R8, R10, Res1
9	5	10K	R14, R17, R21, R23, R25
10	1	10 pf	C27
11	5	22K	R3, R20, R22, R24, R26
12	2	27 pf	C28, C29
13	1	2K	R2
14	1	51	Rref
15	1	56 nH	L1
16	1	75	R13
17	1	82pf	C33
18	1	100	R16
19	12	100 pf	C2, C7, C9, C12, C15, C18, C22, C24, C26, C30 C35, C36
20	2	180pf	C4
21	1	3300pf	C31
22	1	B12v105-1	Q1
23	1	ISV229	D1
24	1	LMX2330A	U1
25	1	Alps 926a	U2
27	2	O.C. // S.C.	R shunt
28	2	18	R28 R29

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