National Semiconductor

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SCAN EASE
SCAN Embedded Application Software Enabler

General Description

National Semiconductor SCAN EASE, a suite of software tools, enables ATPG or custom generated test vectors to be embedded within an IEEE 1149.1 compatible system, administers test control and provides remote access.

EmbedPrep—Embedded Test Preparation includes embedded test development tools that convert ATPG output files, like SVF or PAT, into Embedded Vector Format (EVF) for use with EmbedTest.

EmbedTest—Embedded Test application code includes high level code that controls the test flow and communications between the embedded system and a remote system test administrator. It includes function libraries for controlling IEEE 1149.1 compliant boundary scan chains (SCANLIB), and reading test vectors stored in EVF (EVFLIB). EmbedTest compiles to run on any microprocessor supporting ANSI-C.

EmbedComm—Embedded Test Communication provides a Windows® GUI for remote access to EmbedTest running on an embedded system.

Features

- Processor independent—runs on big/little endian and memory- and I/O-mapped architectures
- Compatible with Teradyne VICTORY™ ATPG and JTAG Technology BTPG™ tools (others supported upon request)
- Provides automated translation, application and evaluation of ATPG-generated tests in an embedded system environment
- Includes a Scan Function Library and National's Embedded Boundary Scan Controller SCANPSC100F device driver to support custom or non-ATPG generated vector applications
- Supports embedded test data log for diagnostic processing
- Includes Microsoft Windows GUI and serial communication code for system administration and remote testing
- Supports SCANPSC110F Hierarchical and Multidrop JTAG Addressable Port architecture

Order Number	Description
SCANEASEV100BSW	Basic Software License
SCANEASEV100CSW	Corporate License
SCANEASEV100MSW	Maintenance Contract

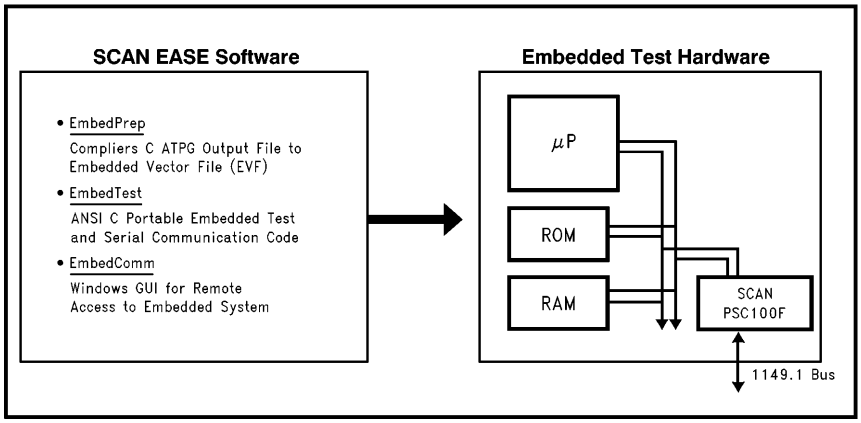

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FIGURE 1. SCAN EASE Enables ATPG Test Vectors to be Embedded

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Windows® is a registered trademark of MicroSoft Corporation.
BTPG™ is a trademark of JTAG Technologies.
VICTORY™ is a trademark of Teradyne, Inc.

Functional Description

SCAN EASE does much of the programming work required by programmers to convert a tester manufacturer's test vectors into embedded test vectors; manages and executes the test; and provides communications code to download and initiate tests remotely. SCAN EASE has a user-friendly Windows GUI interface to simplify test administration.

The test development process for embedded system test begins with generating tests using an off-the-shelf ATPG tool. A separate set of tests for each board type in the system is created during manufacturing test development. These tests can be reused for embedded test, too. National's SCAN EASE tools compile test vectors stored in Serial Vector Format (SVF) or Pattern Format (PAT) into EVF, a compact binary format appropriate for embedded applications.

Several of the board level EVF files can be concatenated to create a system level test. Partitioning tests enables EmbedTest to isolate and report pass/fail information to the partitioned level—board, module, etc.—without running diagnostic software. EVF test files can be placed in ROM for power-up self test or down loaded to RAM.

EmbedTest also provides a set of functions that enable communication between the embedded system and a serial interface for a system administrator or remote computer. EmbedTest commands, such as configuration, reporting test results, downloading new tests and uploading data logs, are performed over this serial interface.

Supporting Hardware

The SCANPSC100F Embedded Boundary Scan Controller is a 28-lead IC designed to provide a simple, efficient interface between a microprocessor and the 1149.1 Test Access Port (TAP) signals. Its 8-bit asynchronous interface connects directly to the local bus of many popular processors and allows the test clock (TCK) to run at a different clock speed than the local bus. The SCANPSC100F supports TCK frequencies up to 25 MHz.

Compatibility

Designed for portability and flexibility, both EmbedTest and EVF run on both big endian and little endian memory architectures; the SCANPSC100F can be either I/O-mapped or memory-mapped. This flexibility allows same code and test vectors to run on various machines simply by recompiling with a C-compiler for the target machine.

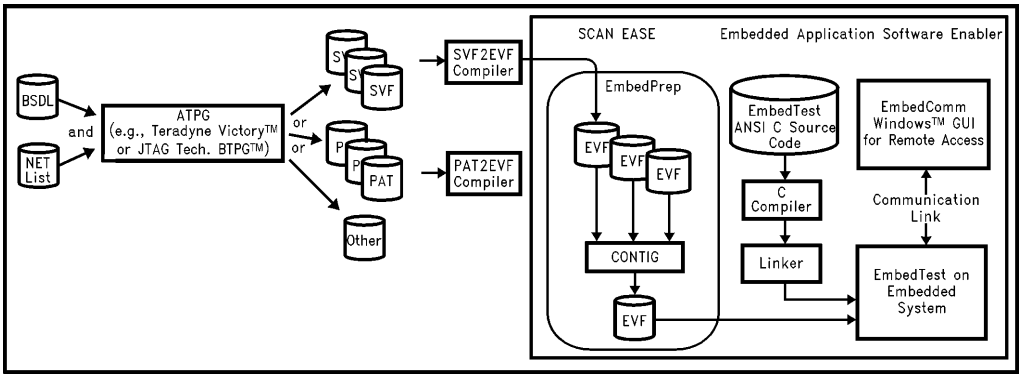

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FIGURE 2. SCAN EASE Works with Existing Board Test Vectors

System Level Test Support

Partitioning tests is important to achieve built-in fault isolation. A natural place to partition tests is at the board or module interface. Design boards with a 100% scannable interface to the system back plane by buffering all back plane signals with boundary scan compliant components like National's 18-bit wide SCAN Test Access Logic CMOS and ABT devices. A 100% scannable interface enables ATPG to generate 100% fault coverage on the back plane. The SCAN ABT Test Access Logic interface with power-up TRI-STATE® for live insertion allows board level tests to be performed without disturbing back plane signals, too.

The Hierarchical and Multidrop JTAG Addressable Port SCANPSC110F provides an interface from a single IEEE 1149.1 TAP to "local TAPs" on boards or modules that reside within a system. This enables boards to be pulled or added to the system without breaking the serial scan chain, and makes it possible to perform an interrogating infrastructure test to determine the system configuration before applying board-level tests. The SCANPSC110F facilitates partitioning of boards and modules within the system for improved fault isolation.

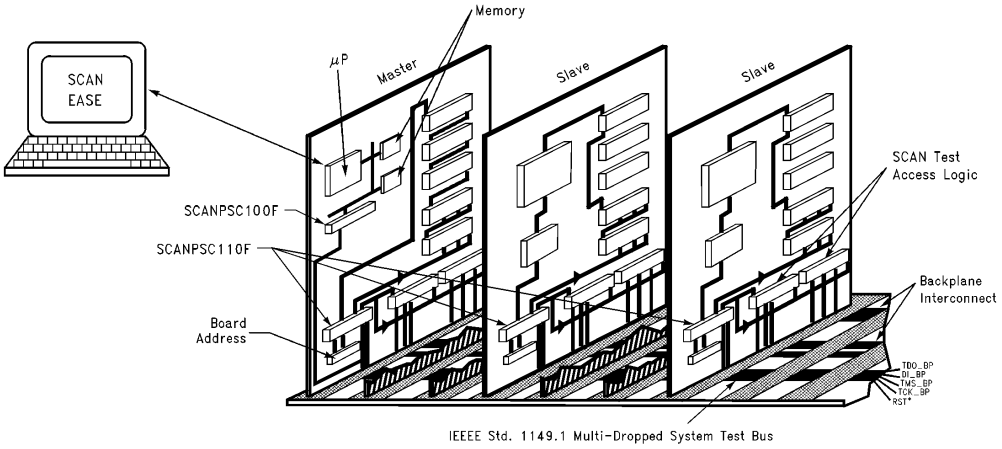

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FIGURE 3. Embedding SCAN EASE for System Level Test

More Detailed Information about SCAN EASE

An application note is available on National's Web Site (http://www.nsc.com), and through the National Technical Support Center (1-800-272-9959) to provide more detailed information on the SCAN EASE architecture and API (applications programming interface). The SCAN EASE product includes a reference manual to detail the EVF format, embedded code architecture and functions which comprise the SCAN EASE tool set.

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

http://www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 180-530 85 85
English Tel: +49 (0) 180-532 78 32
Français Tel: +49 (0) 180-532 93 58
Italiano Tel: +49 (0) 180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2308
Fax: 81-043-299-2408