Single Event Upset (SEU) Sensitivity Dependence of Linear Integrated Circuits (ICs) on Bias Conditions

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Abstract

The single event upset (SEU) sensitivity of certain types of linear microcircuits is strongly affected by bias conditions. For these devices, a model of upset mechanism and a method for SEU have been suggested.

1. INTRODUCTION

The history of the single event upset (SEU) study of linear integrated circuits (ICs) is relatively short. The first reporting of SEUs in linear ICs took place in 1993 [1]. This can be compared with the substantially longer history of the total ionizing dose (TID) investigation of linear ICs, including those involving electron irradiation [2,3]. However, the study of SEUs in linear ICs (which have also been called analog SEUs) has gained attention [4, 5, 6] in recent years partly due to the detrimental effects which may result from analog SEUs in space borne electronics systems. For example, battery charging circuits, which incorporate a voltage comparator followed by a D-type flip-flop, have terminated the charging process when the comparator is irradiated by heavy ions. Similar systems have been utilized in space to charge batteries with the use of solar panels. In other cases, analog SEUs may be tolerated, although they are a nuisance [7]. While previous studies of analog SEUs have included test results obtained for varying bias settings [4,5,6], the majority of the test results have been obtained with a relatively small number of input bias settings. Therefore, a substantial difference in the sensitivity of a test device type due to different bias conditions has not been reported. In order to better understand the upset mechanisms and to possibly mitigate the impact of SEUs on the system, we have exposed several types of linear ICs biased in varying conditions to heavy ions. This has extended the scope of SEU observations in linear ICs to include various quiescent input conditions. The current investigation has led to a finding in which SEU sensitivity may be reduced by controlling the quiescent input conditions in some types of linear ICs.

II TEST DEVICES

Test device types include voltage comparators, operational amplifiers, and other linear integrated circuits, all of which incorporate a difference amplifier circuit at the input section. The input section has been shown to be sensitive to heavy ions in similar circuits [1]. The test device types are shown in Table 1.

The LM119 voltage comparator incorporates npn transistors in the difference amplifier sections (D1, D2, and D3) and the level shift section (L) as shown in Figure 1. This is designed for high speed applications and it provides a response time of less than 100 nanoseconds. The positive and the negative inputs ($+v_{IN}$ and $-v_{IN}$) are directly tied to the transistors Q1 and Q2, respectively, in the D1 amplifier.

LM139 and LM111 voltage comparators incorporate pnp transistors in the front section, where the initial amplification takes place. These devices are of much older design and have a relatively slow time response. The response times for LM139 and LM111 are about 1.3 microseconds and 200 nanoseconds, respectively. A simplified circuit diagram for LM139 is shown in Figure 2. The Darlington difference amplifier is made up of four transistors (Q1, Q2, Q3 and Q4). The diodes (D1 and D2) at the input pins provide a quick recovery acting as an additional current source augmenting C1 or C3 for a low (less than 0.6 volts) to high voltage transition. LM111 consists of three difference amplifiers (D1, D2 and D3) as shown in Figure 3. It does not have the quick recovery diodes at the inputs. The voltage conversion (toward the output voltage, v_O) at the end section of the D3 circuits is (conceptually) similar to that shown in the "L" section in Figure 1. Also, the "SO" section matches that in Figure 1.

We do not show transistor level circuit schematics of the rest of the device types due to limited availability of space. However, a transistor level circuit schematic is often provided in the specification sheet of a device by the manufacturer. The AD9696 voltage comparator has a fast response time, which is on the order of tens of nanoseconds. The operational amplifiers Op-42 and LM108 are fabricated with different technologies. Op-42 incorporates a fast JFET (junction field effect transistor) input difference amplifier followed by circuits made up of npn transistors for fast response. LM108 incorporates the standard npn bipolar transistors in the first difference amplifier. However, the typical input bias current value of about 1 nano-Ampere for this device type is comparable to those for FET devices.

REF-02 is a bipolar voltage reference device, which incorporates a few difference amplifiers. One is to compensate for the temperature change while another is to monitor and to regulate the output. As such it may be affected by heavy ions. SG1549 is a bipolar current sense latch device consisting of a couple of voltage comparators as shown in Figure 4. The

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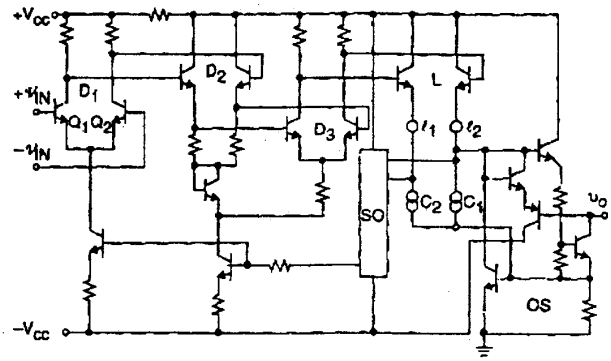
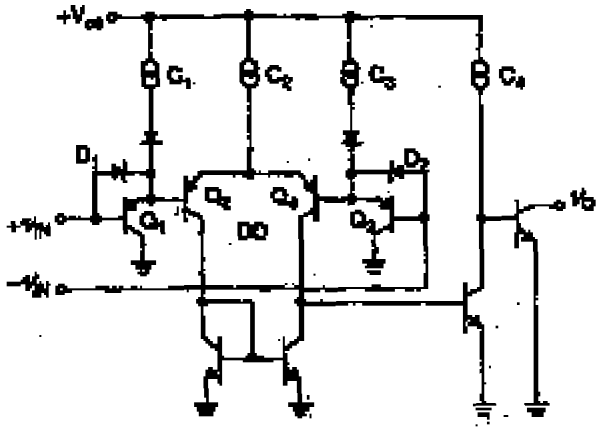


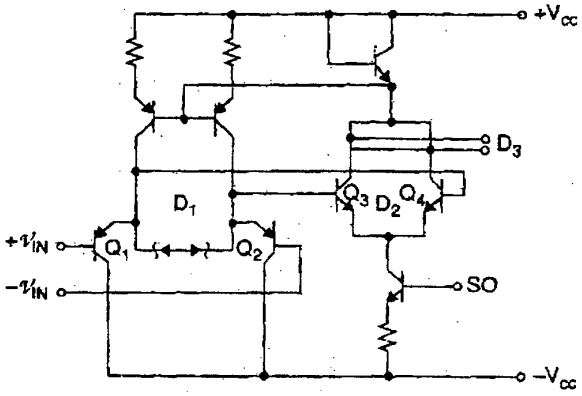
C_1, C_2	Current source
D_1, D_2, D_3	Difference amplifier
L_1, L_2	Level shift resistor
L	Level shift transistors
OS	Output stage (anti-saturation)
SO	Source for operating current
$+V_{IN}$	+ input voltage
$-V_{IN}$	- input voltage
$+V_{cc}$	Positive bias voltage
$-V_{cc}$	Negative bias voltage
V_O	Output voltage

Figure 1. Simplified circuit schematic for LM119 voltage comparator



C_1, C_2, C_3, C_4	Current source
D_1, D_2	Difference amplifier
DD	Darlington difference amplifier
$+V_{IN}$	+ input voltage
$-V_{IN}$	- input voltage
$+V_{cc}$	Positive bias voltage
$-V_{cc}$	Negative bias voltage
V_O	Output voltage

Figure 2. Simplified circuit schematic for LM139 voltage comparator



D_1, D_2, D_3	Difference amplifier
SO	Source for operating current
$+V_{IN}$	+ input voltage
$-V_{IN}$	- input voltage
$+V_{cc}$	Positive bias voltage
$-V_{cc}$	Negative bias voltage

Figure 3. Simplified circuit schematic for LM111 voltage comparator

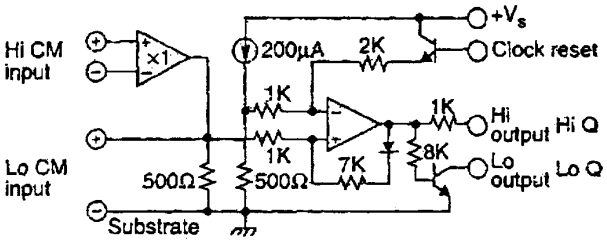


Figure 4. Block diagram for SG1549

Table 1 List of Linear ICs Considered for SEU Testing

Device ID	Manufacturer	Function	Date code
LM111	National	Voltage Comparator	9619
LM119	National	Voltage Comparator	9535
LM139	National	Voltage Comparator	9318
AD9696	Analog Devices	Voltage Comparator	9605
Op-42	Analog Devices	Operational Amplifier	9630
LM108	National	Operational Amplifier	9533
REF-02	Analog Devices	Voltage Reference	9305
SG1549	Silicon General	Current Sense Latch	9627

*All are fabricated with the bipolar technology.

major comparator in the middle of the diagram is made up of pnp transistors forming the Darlington difference amplifier. SG1549 is designed to monitor current for use with a pulse width modulator (PWM) in a power converter system [8].

III. TEST METHOD

Most analog SEUs appear as a disturbance in the output of the test device. The disturbance often has both positive and negative polarities, a wide range of pulse heights, and varying widths [1,4]. These SEUs are also called transients, since they disappear in time. However, their effects may be more lasting in various circuit systems affected by them. Such an example is provided in Section I.

During the testing, the irradiation site (where the device under test is located) is several feet (or more) away from the area where SEU detection (observation or counting of upsets) takes place. In order to compensate for the large attenuation of the output signals (especially for those which do not have high driving capability), we have added a simple resistor network. An example utilized for LM111 is shown in Figure 5. Since the oscilloscope ha a very high voltage gain, it is possible to observe the disturbance adequately by simply raising the gain as necessary. Often we use a storage scope (such as Tektronix TDS540 or TDS744A) to collect an instantaneous snap shot of the disturbance. This information includes the threshold voltage of the analog signal output, the pulse width, and the polarity of the disturbance. (Since the snap shots of these disturbances have been presented earlier [1,4,6], we do not show them here.) The same detection mechanism is used to collect many events in order to increase the SEU counts for better statistics. We occasionally insert a current driver or a logic gate (such as a flip-flop) at the output of LM111. then, by counting the output transitions of the flip-flop, we indirectly detect the analog SEU events. In some applications, this set-up is very convenient to use. However, we inevitably lose the fidelity of the SEU signals both in the time and the pulse height domains. In other words, we no longer observe the variations in the pulse height or width. Yet, we have achieved the objective of finding out how a digital circuit which receives signals from an analog IC may be affected. Therefore, we use both types of test circuits, which augment each other.

For devices other than voltage comparators, the test set-ups are still very similar to that shown in Figure 5. In order to measure the sensitivity of operational amplifiers the test device is replaced by an operational amplifier biased in a general condition as shown in Figure 6. We often tie $+V_{IN}$ to ground and $-V_{IN}$ to a set voltage.

SG1549 contains a couple of front-end amplifier circuits. The device senses the current at both the high and low voltage levels with internal voltage comparators. We have measured the sensitivity of both comparators in the device. However, for brevity we describe here only the procedures adopted for testing the lower comparator. In order to measure the sensitivity of the lower comparator, we short the two inputs to the upper comparator (see Figure 4) and provide a specific input voltage to the positive inputs for the 'LO CM INPUT'. The trigger threshold has been internally set at 100 mV. In other words, the output changes the state when the difference in the input voltages exceeds 100 mV. Here, we select three voltage levels, 50, 70, and 90 mV.

REF-02 is biased while maintaining the output resistor (R_Z in Figure 5) to 3.3 Kohm as shown in Figure 7. The inputs to the difference amplifier in this device type are not suited for controlled variations, since they are tied to the temperature sensors or the output voltage. Nevertheless we include this device type in our test samples, because we may observe measurable difference in SEU sensitivity for different temperature settings.

The SEU cross-section has been defined earlier in a manner acceptable to the radiation effects community [1,4,6]. We use the same definition. Namely, the SEU cross-section, σ, is defined, as for digital circuits, via the equation $\sigma = N/F \cos\theta$), where N is the number of upsets and ($F \cos\theta$) is the usual fluence/angle factor. It is crucial to note that N depends upon the value of the threshold.

We use N (67 MeV), Ne (90 MeV), Ar (180 MeV), Cu (290 MeV), Kr (380 MeV), and Xe (600 MeV) ions at the Lawrence Berkeley National Laboratory 88-inch cyclotron facility. The associated LET values of these ions are 3.2, 5.6, 15, 30, 41, and 63 MeV/[mg/cm^2)], respectively.

IV. TEST RESULTS

The SEU disturbances are pulses, which vary from very short pulses (<5 nanoseconds) of small pulse height (<50 mV) to those of long duration (>1 μs) with large pulse height (rail-to-rail). They are superimposed on the normal output voltage of the microcircuit. Some disturbances (or transients) are made up of more than one pulse. For example the main pulse of one microsecond width is followed by a second pulse of similar width, but relatively smaller pulse height, arriving just about the time when the main pulse has returned to the quiescent level. These double pulses are counted as one disturbance [1,4]. The trigger voltage threshold has been somewhat arbitrarily chosen (see Figure 5). When the +Vcc is +5 V and -Vcc is at the ground for LM111, the trigger threshold is set at +2.5 V.

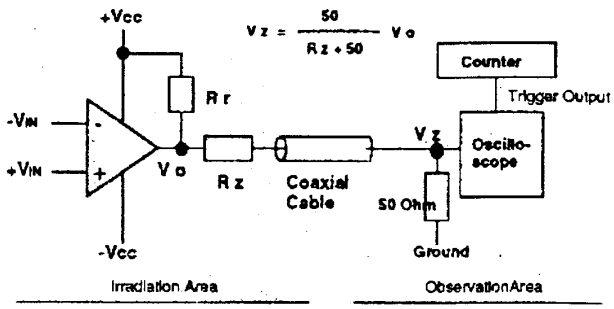


Figure 5. SEU test setup for a voltage comparator

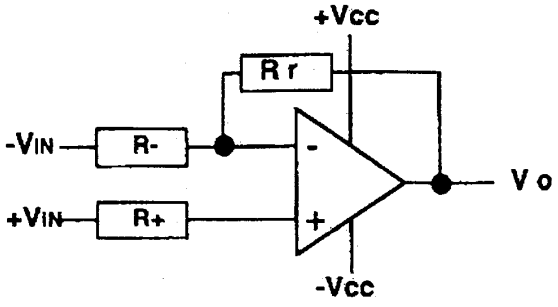


Figure 6. Bias configuration for an operational amplifier

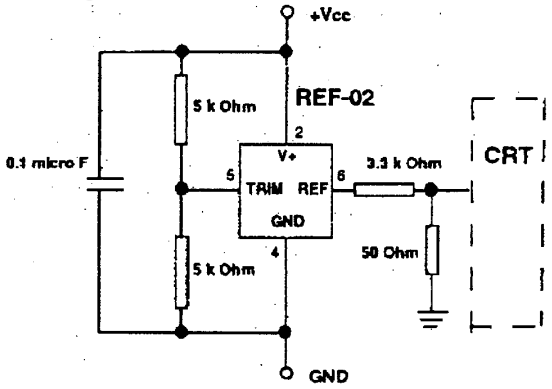


Figure 7. SEU test setup for REF-02

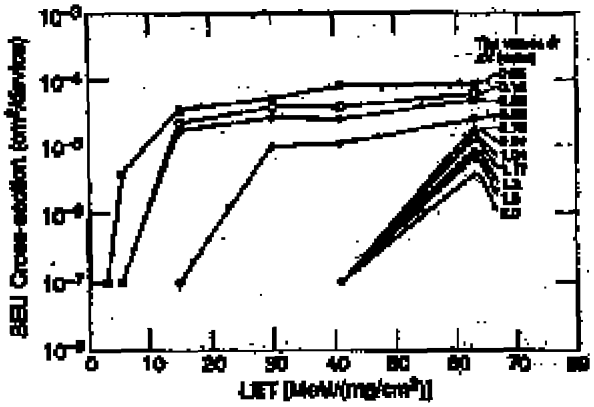


Figure 8. SEU test results for LM111 biased at +5 volts

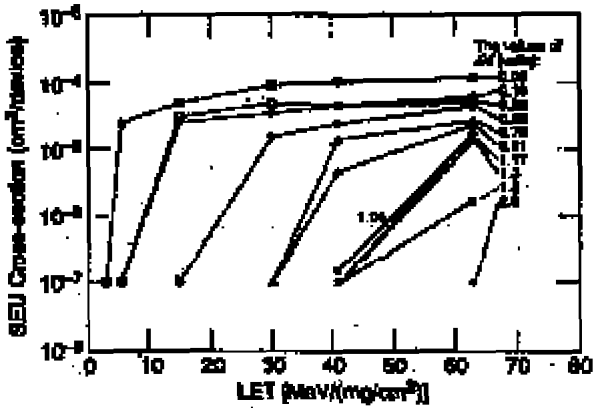


Figure 9. SEU test results for LM111 biased at +10 volts

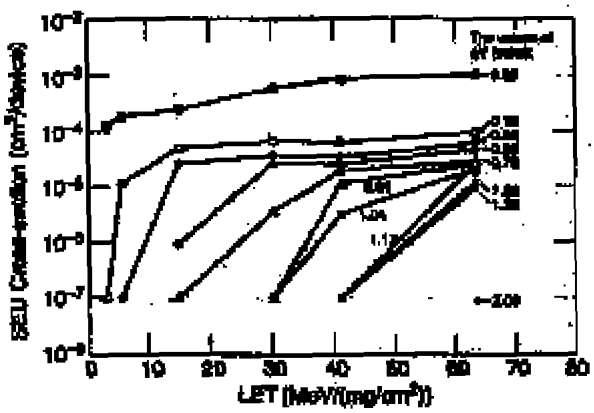


Figure 10. SEU test results for LM111 biased at +15 volts

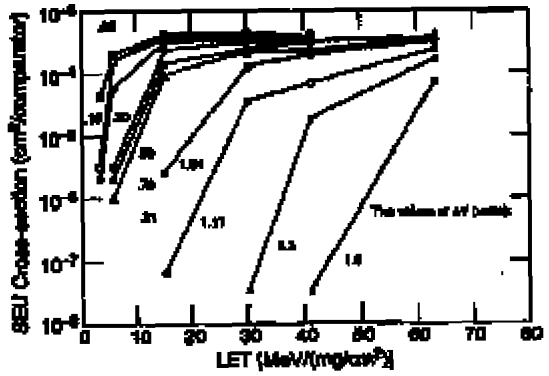


Figure 11. SEU test results for LM139 biased at +5 volts

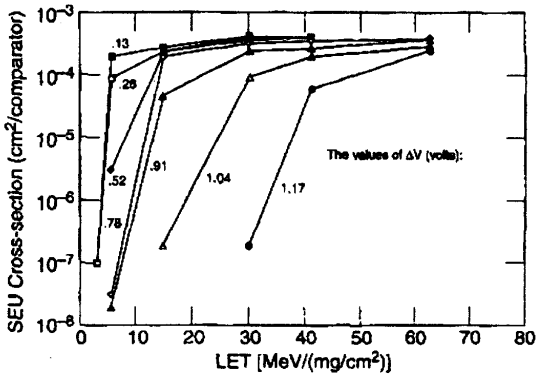


Figure 12. SEU test results for LM139 biased at +13 volts

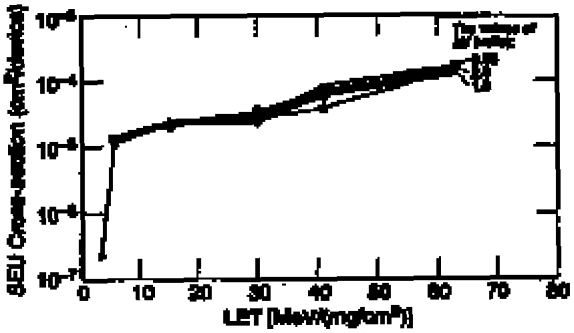


Figure 13. SEU test results for LM119 biased at ±15 volts

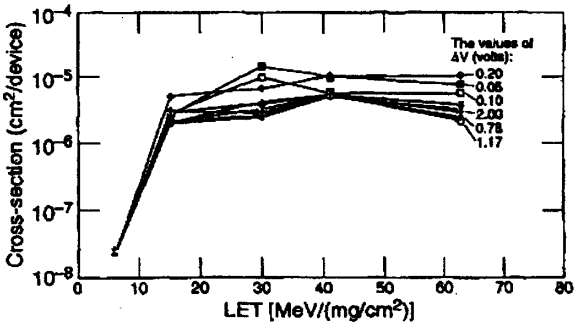


Figure 14. SEU test results for AD9696 biased at ±15 volts

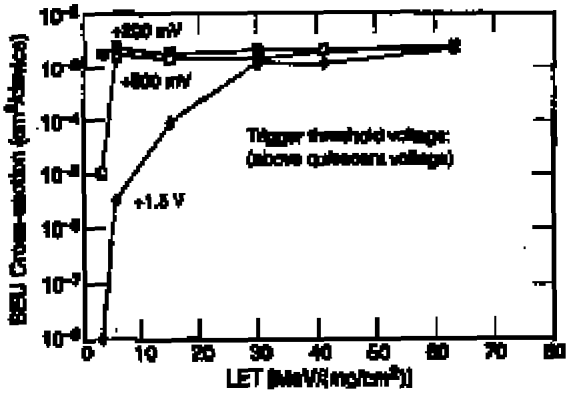


Figure 15. SEU test results for Op-42 biased at ±15 volts

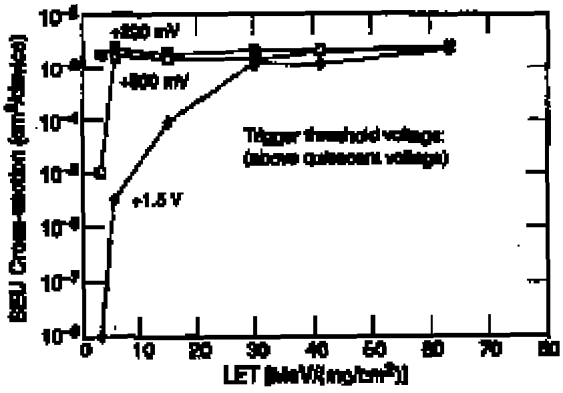


Figure 16. SEU test results for LM108 biased at ±15 volts

Table 2. Approximate threshold LET values in [MeV/(mg/cm2)] for various ΔV values.

ΔV (Volts)	LET_{th} (+Vcc = 5V)	LET_{th} (+Vcc = 10V)	LET_{th} (+Vcc = 15V)
0.05	3	3	<3
0.10	5	5	3
0.20	5	5	5
0.50	15	15	<15
.78	50	30	15
.91	50	30	30
1.04	50	40	30
1.17	50	50	40
1.3	50	50	40
1.5	50	50	40
2.0	50	60	60

While we increase +Vcc to +10V and then to +15V, we still maintain the trigger threshold at +2.5V. Since the output of LM111 is the "open collector" type, the present choice of the trigger threshold appears to be proper.

The SEU results for LM111 are shown in Figures 8, 9, and 10 for the bias voltage of (+Vcc = 5 volts and -Vcc = ground), (+Vcc = 10 volts and -Vcc = ground), and (+Vcc = 15 volts and -Vcc = ground), respectively. In each case the input voltage difference, ΔV [= $(+v_{IN})$ - (v_{IN})], was varied from 0.05 to 2.0 volts. The threshold LET values became large as ΔV was increased as shown in Table 2. The ratio of the number of positive going SEU pulses and negative going SEU pulses was close to unity.

LM139 comparators showed similar response to heavy ions. The test results for the two values of +Vcc are shown in Figures 11 and 12 for +Vcc = 5V and 13 V, respectively. We observed that the threshold LET values became larger as the difference between $+v_{IN}$ and $-v_{IN}$ increased.

We irradiated LM119 and AD9696 comparators for various input bias conditions. The results are shown in Figures 13 and 14, respectively. For these device types the threshold LET value did not change appreciably while the difference between $+v_{IN}$ and $-v_{IN}$ was varied.

Operational amplifiers Op-42 and LM108 were biased with input resistors R+ and R- (see Figure 6). In this "linear" range of response, the input voltages of the operational amplifiers were at "virtual ground". When $+v_{IN}$ and $-v_{IN}$ were varied, we did not observe any measurable differences in the sensitivity to SEU. Each transient had its own specific pulse height. Some pulse heights were as short as several mV, while others reached more than 1 volt. These pulse heights were measured when +Vcc was +15V and -Vcc was -15V. These results for OP-42 and LM108 are shown in Figures 15 and 16, respectively. For those tests, all pulses larger than the trigger threshold voltage were counted (see Figure 5).

A wide range of pulse heights was observed for REF-02. Since the quiescent output voltage was +5V, we varied the trigger voltage to 5.6, 6.3, and 10V for measuring positive going pulses and 4.4, 3.8, 2.5, and 1.6V for measuring negative going pulses. There were substantially more upsets with smaller pulse amplitudes (for example, -1v pulse superimposed on the 5 volts output) than those with larger amplitudes (for example, +4V pulse superimposed on the 5 volts output) as shown in Figure 17. These cross-sections were obtained with copper ions (LET = 30). The SEU cross-sections for the trigger threshold values of 1.6, 3.8, and 10V are shown in Figure 18 for other LET values.

For SG1549 current sense latch, the two outputs (Hi Q and Lo Q) were always the complement of each other (one was at 5V, while the other was at 0V). The SEU pulses rose very quickly (on the order of 100 nanoseconds) and returned to the quiescent value gradually (on the order of one microsecond). For three sets of "LO CM INPUT" values of 50, 70, and 90 mV), we obtained the SEU curves as shown in Figure 19. Since the output changes its state while "LO CM INPUT" exceeds 100mV, we limited our measurements to only three input values (all are below 100mV). The threshold LET values as well as the saturation values for these three inputs varied substantially. As can be seen in the figure, the smaller the ΔV (= Vi+ - Vi-), the larger the cross section.

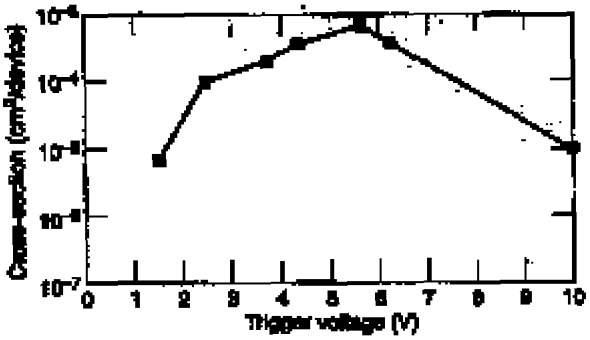


Figure 17. SEU test results for REF-02 with Cu ions

Figure 18. SEU test results for REF-02 for varying threshold voltage

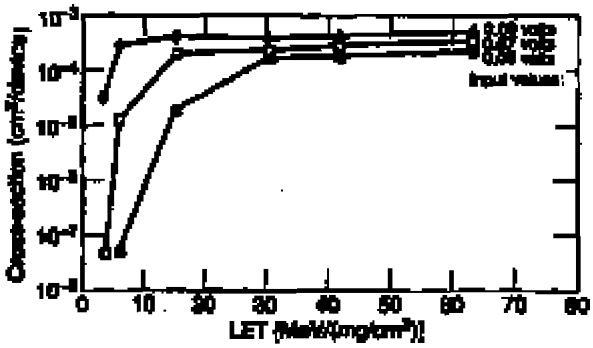


Figure 19. SEU test results for SG1549

V. DISCUSSIONS

Some device types showed a strong correlation between the input bias conditions and the SEU sensitivity, while others showed hardly any dependence as shown in Table 3. The first group of devices included the LM111 and LM139 voltage comparators and the current sense latch (*SG1549*). All these devices incorporated pnp transistors in the first stage difference amplifier. For these devices the voltage levels at the positive ($+v_{IN}$) and the negative ($-v_{IN}$) inputs directly affected the biasing condition of the input transistors. The SEU sensitivity depended on the input voltage difference ΔV [= ($+v_{IN}$) - ($-v_{IN}$)]. The smaller the ΔV [= ($+v_{IN}$) - ($-v_{IN}$)], the higher the SEU sensitivity, as shown in Figures 8 through 12. This type of result was "hinted at" in earlier investigations [1, 6]. However, no systematic observations had been made.

In order to further investigate this phenomenon for LM139, we carried out an irradiation with a finely focused pulsed laser beam [9]. While limiting the laser pulse energy to less than 4 pico-Joule (pJ), we looked for SEU sensitive regions in the whole die. This enabled us to find the exact locations of sensitive regions and to measure the relationship between the input voltage difference (ΔV) and the laser pulse energy in pJ, which was needed to cause an upset. There were only two sensitive regions (in the whole die), which were the base areas ($< 1 \times 10^{-4}$ cm^2) of the transistors Q1 and Q3. The relationship between the input voltage difference (ΔV) and the laser pulse energy is shown in Figure 20.

The base physically surrounded the associated emitter. Since the saturation cross-section for this device type was about 4×10^{-4} cm^2 (see Figures 11 and 12), we expected that a considerable charge diffusion took place. This increased the apparent sensitive regions that were derived during the heavy ion experiment.

The laser irradiation of LM111 showed that the most sensitive region for this device type was limited to the first difference amplifier (D1 in Figure 3). Since the input voltage difference (ΔV) did not affect the biasing of D2 and D3 in Figure 3, the above result was consistent with the results shown in Figures 8, 9 and 10.

Table 3. The effect of the input voltage difference on SEU Sensitivity

Device ID	Function	Dependence of ΔV on SEU
LM111	Voltage Comparator	Yes
LM119	Voltage Comparator	No
LM139	Voltage Comparator	Yes
AD9696	Voltage Comparator	No
OP-42	Operational Amplifier	No
LM108	Operational Amplifier	No
REF-02	Voltage Reference	Not Measured
SG1549	Current Sense Latch	Yes

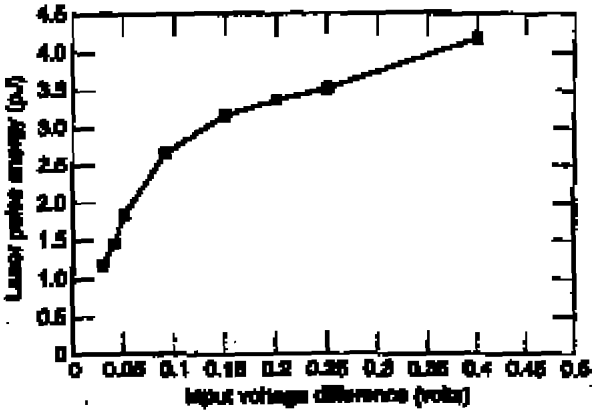


Figure 20. Laser test results for LM139
SEU threshold vs. input voltage difference (ΔV)

A mechanism of the transient formation for LM139 may be hypothesized. In order to cause an upset, actual charge collection takes place within the first difference amplifier as indicated by the laser test. Let us assume the following condition: ($+v_{IN}$) > ($-v_{IN}$) in Figure 2. Then, the output, vo, is close to +Vcc. When ΔV [=($+v_{IN}$) - ($-v_{IN}$) is very small (e.g., 50mV), a small deposited charge at the base of Q1 can increase the emitter current at Q1, momentarily exceeding that in Q3. This will cause the difference amplifier consisting of Q2 to Q4 to "flip" the polarity. In other words, more current passes through Q2 than Q4. The new condition may be "amplified" by the subsequent transistors in the circuit, resulting in an SEU at the output. The duration of the "flip" is strongly affected by the rest of the circuit. The original quiescent condition may resume after all deposited charge has been dispersed.

When ΔV becomes large, we need an additional charge to cause a temporary unbalance and to "flip" the state. Therefore, ions with larger LET values are needed to cause the effect. This is consistent with the shift in the threshold to high LET values (see Figures 11, 12, and 13). The dependence on the level of +Vcc or -Vcc was minimum as previously observed [1,4,6]. We have not carried out any computer circuit simulation with the aid of SPICE or other techniques. This is

because the input parameters for simulation have not been adequately observed.

The LM111 comparator showed similar response to ions as LM139. The smaller the input voltage difference, the stronger the sensitivity to SEU. We expect that very similar charge collection mechanisms are applicable for SEUs in this device type.

In LM119 and AD9696 comparators, npn transistors form the first difference amplifier. These are designed for high speed applications. Once again we can formulate a possible scenario, which explains the formation of transients at the output (see Figure 1) for LM119. A fast npn transistor responds to initiate a momentary unbalance. This is "amplified" by subsequent difference amplifiers causing an upset in the output. However, in these transistors the transition is not dependent on ΔV. In other words we have encountered two extreme conditions: Either no upset for LET value below 3 MeV/mg/cm^2) or upsets for LET values larger than 3 MeV/mg/cm^2). If the LET of an incident particle is large enough, the deposited charge is sufficient to cause an upset regardless of the input voltage difference, ΔV [=(+vI_N) - (-v_{IN})]. The saturation cross-sections for AD9696 tend to be somewhat larger when ΔV is smaller than a few hundred millivolts. On the other hand, no such trend has been found in LM119.

For the REF-02 device type, we could not obtain SEU results for which we could systematically change the input voltage difference. At room temperature, we observed a wide range of output pulse heights for REF-02. The smaller the SEU pulse height, the more frequently they appeared.

The front end of SG1549 is a difference amplifier made up of pnp transistors. These transistors are also used for LM111 and LM139 as discussed earlier. Again this device type showed the dependence of SEU cross-section on ΔV [=(+v_{IN}) - (-v_{IN})]. the devices were more sensitive when the externally applied input signal (+v_{IN}) was close to the internally applied signal (-v_{IN}), which is set at 100mv.

V. CONCLUSIONS

The linear ICs (sometimes called analog ICs) are sensitive to SEUs. Often, the most sensitive region is the first stage difference amplifier. for some device types (utilizing mostly pnp transistors) the SEU vulnerability at the input difference amplifier circuit depends on biasing; the smaller the input voltage difference, ΔV, the larger the SEU sensitivity. while the rest of the test device types (fabricated mostly with npn transistors or JFET) is still sensitive, the sensitivity is not strongly dependent on the bias condition.

The SEU pulses vary in their pulse heights from very small ones to the ones reaching the supply voltage (Vcc). Generally, the number of small pulse height events exceeds that of large pulse height events.

One obvious way to mitigate the SEUs for LM111, LM139, and SG1549 is to bias the devices while increasing the input voltage difference, ΔV, as much as possible. This ensures that these devices have a lower sensitivity to SEUs. On the other hand, another way to reduce the impact of SEUs is to connect the output of linear ICs to a device which is insensitive to pulses with lower amplitudes or to a device which attenuates the SEU pulses. This tends to stop the propagation of transients. Since pulse height varies in analog SEUs, the second approach will be useful in localizing the SEUs for most linear ICs.

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