Table of Contents – Published Papers

The following Applications Notes are available on National Semiconductor's web site at www.national.com/mil.

Dose Rate Response of Advanced CMOS Products (Applications Note AN-924)

Purpose: This paper investigates the dose rate radiation response of an Advanced CMOS product: the FACT 54AC299 8-Input Universal Shift/Storage Register with Common Parallel I/O pins. Data demonstrates the latchup-free capability of this FACT device type. It also shows the dose rate upset threshold level of the 54AC299.

Radiation Design Test Data for Advanced CMOS Product (Applications Note AN-925)

Purpose: Radiation test data is presented for different radiation environments as performed on National Semiconductor's FACT logic family. Over twenty device types have been evaluated by independent investigators, users, and by National.

Radiation Design Considerations Using CMOS Logic (Applications Note AN-926)

Purpose: Today's rapidly changing global political climate is significantly impacting the military strategies of Free World countries. Important decisions are being made regarding each country's defense and military equipment needs. Regardless of these on-going political changes, however, the threat of nuclear weaponry use remains a viable possibility. As long as a first-strike capability exists, radiation-hardened strategic and tactical systems will be designed.

Total Dose Testing of Advanced CMOS Logic at Low Voltage (Applications Note AN-927)

Purpose: This paper examines the impact of using an Advanced CMOS product in a low voltage (3.3 V_{DC}) application which is subjected to a total ionizing dose environment. Results from this investigation demonstrate a significant improvement in the total dose response of radiation-induced leakage current at 100 krads(Si) level. The improvement factor of low voltage (3.3 V_{DC}) was greater than 8x better than 5.0 V_{DC}.

SEU and Latchup Tolerant Advanced CMOS Technology (Applications Note AN-932)

Purpose: Selected microcircuits constructed in National Semiconductor's FACT technology were tested for heavy ion-induced Single Event Upset (SEU) and latchup. The devices showed no signs of heavy ion-induced latchup for LET values up to 120 MeV/(mg/cm^2). SEU LET thresholds varied within a rather narrow range of 40 MeV(mg/cm^2) to 60 MeV/(mg/cm^2). The test results suggest that FACT devices will exhibit higher tolerances to the cosmic ray environment than functionally similar microcircuits fabricated in HC/HCT, ALS, or LS technology.

Single Event Upset and Latchup Considerations for CMOS Devices Operated at 3.3V (Applications Note AN-989)

Purpose: A comparison of single event upset and latchup test results for devices operated at several bias levels, from 2.5V to 6V, is reported. Vulnerability to SEU increased with decreasing bias, whereas the opposite pattern was observed for SEL. The relationship between threshold SEU vulnerability and bias is not regular, which precludes the use of simple prediction schemes for obtianing the expected vulnerability at 3.3V form existing 5V data.

Notes