Logic Table of Contents

National Semiconductor will not guarantee the RHA performance of any product unless National Semiconductor has tested and certified the specific manufacturing lot.

Logic test reports are available on National Semiconductor's web site at www.national.com/mil.

Glossary of Logic-Specific Terms

Asynchronous: A mode of operation that does not require any specific timing relationship between different control inputs.

Buffer: A logic gate with high output drive capability, or fanout. Buffers are used where a single circuit must drive a large number of loads.

Comparator: A logic circuit that will compare two separate input signals and produce an output based on that comparison. A simple comparator is the Exclusive-NOR gate, which produces a high-level output only when its two inputs are identical.

Counter: A logic circuit that counts the number of input pulses it receives. Counters can be used for frequency division, counting, and sequencing digital operations. Common counter configurations are Binary, where the device counts from 0 to 15 and Decade, where the device counts from 0 to 9.

Currents: Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

Data Selector/Multiplexer: A logic circuit that will select one of several input signals and feed that signal onto a common bus line. It can be thought of as a multipole, multiposition switch with each switch pole representing one output and each switch position representing one input.

Decoder/Demultiplexer: A logic circuit that is the complement of the Data Selector/Multiplexer; that is, this circuit takes an input signal and feeds it to any one of several output lines depending on the information placed on its steering, or control, inputs.

Driver: Same as Buffer, above.

F100K 300 Series ECL: Having F100K ECL speed and performance, National's F100K 300 Series consumes up to 50% less operating power, guarantees MIL Class 2 (2,000V - 3,999V) ESD protection, and has a stable I/O over a wide range of voltages and temperatures.

FACT: FACT™ (Fairchild Advanced CMOS Technology) logic is manufactured on a thin Epi-CMOS process. Offers high performance at zero standby power.

- **54ACxxxx:** CMOS inputs and outputs; offers post-irradiation parametric limits to 100 krad(Si)
- **54ACTxxxx:** TTL inputs and CMOS outputs; offers post-irradiation parametric limits to 100 krad(Si)

FACT FCT: Extension of FACT logic for high-performance systems. Features include enhanced noise immunity, improved dynamic threshold, dynamic output drive capable of driving 75Ω transmission lines, latchup immunity, and MIL Class 2 ESD tolerance (2,000V - 3,999V).

FACT Quiet Series™ (FACT QS™): Extension of FACT logic for noise-sensitive applications. Features include reduced ground bounce, improved dynamic threshold, elimination of undershoot, elimination of latchup, and guaranteed MIL Class 2 ESD tolerance (2,000V - 3,999V).

- **54ACQxxxx:** CMOS inputs and outputs; offers post-irradiation parametric limits to 30 krad(Si)
- **54ACTQxxxx:** TTL inputs and CMOS outputs; offers post-irradiation parametric limits to 30 krad(Si)

Flip-Flop: A logic circuit that is used to store information. A flip-flop is called "bistable" since it has two stable states.

f_t Maximum Transistor Operating Frequency: The frequency at which the gain of the transistor has dropped by three decibels.

f_{max} Maximum Clock Frequency: The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic levels at the output with input conditions established that should cause changes of output logic level in accordance with the specification. Unless otherwise specified, this test is performed with no restrictions on input rise and fall times or duty cycle. *(Note: A minimum value is specified that is the highest frequency at which all devices are guaranteed to function correctly.)*

Gate: The basic building block of all logic circuits; an element whose output is a Boolean function of its inputs. The basic functions are the AND, OR, and NOT. By combining these functions, NAND, NOR, Exclusive-OR, and Exclusive-NOR gates are built.

GTO™: Graduated turn-on output; the proprietary circuitry added to FACT QS and FACT FCT products that controls edge rates, i.e., waveshaping.

I_{CC} Supply Current: The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst-case operation.

I_{CC} vs. V_{IN} Traces: Traces of I_{CC} vs. Vin show how the supply current changes with input voltage.

I_{CCD} (Dynamic I_{CC}): Determines the amount of current an IC will consume at frequency.

I_{CCH}: The current flowing into the V_{CC} supply terminal when the outputs are in the HIGH state.

I_{CCL}: The current flowing into the V_{CC} supply terminal when the outputs are in the LOW state.

ΔI_{CC}: Additional I_{CC} due to TTL HIGH levels forced on CMOS inputs.

I_{CCZ}: The current flowing into the V_{CC} supply terminal when the outputs are disabled (high impedance).

I_I, I_{IN} Input Current: The current flowing into or out of an input when a specified LOW or HIGH voltage is applied to that input.

$I_{I(HOLD)}$ Input Hold Current: Input current that holds the input at the previous state when the driving device goes to a high impedance state.

$I_{I(OD)}$ Input Over-Drive Current: Input current that is specified to switch a logic level which is held at previous state.

I_{IH} Input HIGH Current: The current flowing into an input when a specified HIGH voltage is applied.

I_{IL} Input LOW Current: The current flowing out of an input when a specified LOW voltage is applied.

Input Edge Rate: This test is performed to determine what minimum edge rate can be applied to an input and have the corresponding output transition with no abnormalities such as glitches or oscillations.

I_{OFF} Input/Output Power-Off Leakage Current: The maximum leakage current into or out of the input/output transistors when forcing the input/output from 0.0V to 5.5V with V_{CC} = 0.0V.

I_{OH} Output HIGH Current: The current flowing out of the output when it is in the HIGH state. For a turned-off open-collector output with a specified HIGH output voltage applied, the I_{OH} is the leakage current.

I_{OL} Output LOW Current: The current flowing into an output when it is in the LOW state.

I_{OS} Output Short Circuit Current: The current flowing out of a HIGH-state output when that output is short circuited to ground (or other specified potential).

I_{OZ} Output OFF Current: The current flowing into or out of a disabled TRI-STATE output when a specified LOW or HIGH voltage is applied to that output.

I_{OZH} Output OFF Current HIGH: The current flowing into a disabled TRI-STATE output with a specified HIGH output voltage applied.

I_{OZL} Output OFF Current LOW: The current flowing out of a disabled TRI-STATE output with a specified LOW output voltage applied.

Latch: A bistable element that latches, or holds, data which is present at its input at the time the Enable input goes to its inactive state. When the Enable input is active, the data present at the input is passed directly to the output, similar to the operation of a gate.

LSI (Large Scale Integration): Large subsystems or small systems integrated into a single microcircuit.

MSI (Medium Scale Integration): Small subsystems integrated into a single microcircuit.

Multiple (Simultaneous) Output Switching Propagation Delays: These tests are used to ensure compliance to the extended databook specifications and include active propagation delays, disable and enable times at 50pF output load.

Multiple Output Switching Skew: Performance data from the Multiple Output Switching propagation delay testing is analyzed to obtain information regarding output skew of an IC.

One Shot: Monostable multivibrator, a flip-flop that only has one stable state. When triggered by an input transient, it flips to its unstable state for a time period determined by an external R-C network connected to its timing inputs, and then returns to its stable state.

Open Collector: Output configuration that has no internal pull-up. This configuration enables outputs that are connected together (wired-OR) to assume opposite states without incurring damage.

Power-Up I_{CC} Traces: Shows how the supply current reacts to various input conditions during power up.

Schmitt Trigger: An input configuration that has a different threshold point depending on whether the input signal is rising or falling. This is especially useful in electrically noisy environments.

Shift Register: A series of flip-flops in which the data signal is shifted out of one flip-flop and into the succeeding flip-flop during an active transition on the clock input.

SSI (Small Scale Integration): The lowest level of complexity in integrated circuits.

Synchronous: A mode of operation where specific timing requirements must be met between control inputs before an indicated action can occur.

t_F Fall Time: The time interval between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from a defined high level to a defined low level. Common defined levels are from 90% of the signal amplitude to 10% of the signal amplitude.

t_h Hold Time: The interval immediately following the active transition of the timing pulse (usually the clock pulse) of following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized. *(Note: A minimum value is specified that is the smallest time interval above which all devices are guaranteed to function correctly.)*

Totem Pole: An output configuration that contains an internal pull-up structure, usually a transistor pull-up allowing higher output drive capability than is available with open collector outputs.

t_{PHL} Propagation Delay Time: The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_{PLH} Propagation Delay Time: The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHZ} Output Disable Time (of a TRI-STATE Output) from HIGH Level: The time between the 1.5V level on the input and a voltage 0.3V below the steady state output HIGH level with the TRI-STATE output changing from the defined HIGH level to a high impedance (OFF) state.

t_{PLZ} Output Disable Time (of a TRI-STATE Output) from LOW Level: The time between the 1.5V level on the input and a voltage 0.3V above the steady state output LOW level with the TRI-STATE output changing from the defined LOW level to a high impedance (OFF) state.

t_{PZH} Output Enable Time (of a TRI-STATE Output) to a HIGH Level): The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a HIGH level.

t_{PZL} Output Enable Time (of a TRI-STATE Output) to a LOW Level): The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a LOW level.

t_R Rise Time: The time interval between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from a defined low level to a defined high level. Common defined levels are from 10% of the signal amplitude to 90% of the signal amplitude.

Transceiver: A logic circuit that can transmit data onto a bus line and receive data off of the bus line using the same terminal as an input and output. The direction of signal flow is determined by logic levels present at a Direction Control input.

t_{rec} Recovery Time: The time between the 1.5V level on the trailing edge of an asynchronous input control pulse and the same level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

TRI-STATE: A registered trademark for a circuit configuration in which the device output can be switched "off" during which time the output presents a very high impedance to the bus it is connected to. This allows multiple outputs to be connected to a bus line while only one output drives the line, the other outputs being switched into their high impedance states.

t_s Setup Time: The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which

interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{TLH}, T_r Transition Time, or Rise Time: The time interval between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from a defined low level to a defined high level. Common defined levels are from 10% of the signal amplitude to 90% of the signal amplitude, or from 0.6V to 2.6V.

t_{TLL}, T_f Transition Time, or Fall Time: The time interval between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from a defined low level to a defined high level. Common defined levels are from 10% of the signal amplitude to 90% of the signal amplitude, or from 0.6V to 2.6V.

t_w Pulse Width: The time interval between specified voltage reference points on the leading and trailing edges of a pulse waveform. *(Note: A minimum value is specified that is the smallest time interval above which all devices are guaranteed to function correctly.)*

t_{WOUT} Output Pulse Width: The time interval between specified voltage reference points on the leading and trailing edges of an output waveform. *(Note: This is usually only specified for monostable elements.)*

USC™ (Undershoot Corrector): The proprietary circuitry added to FACT QS and FACT FCT to control signal excursion below ground.

V_{CC} Supply Voltage: The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

$V_{CD\ (Max.)}$ Input Clamp Diode Voltage: The most negative voltage at an input when a specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode, intended to clamp negative ringing at the input terminal.

V_{IH} Input HIGH Voltage: The range of input voltages that represents a logic HIGH in the system.

$V_{IH\ (Min.)}$ Minimum Input HIGH Voltage: The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.

V_{IHD} Dynamic Input HIGH Voltage: The minimum input voltage that is recognized as a HIGH level during a Multiple Output Switching (MOS) operation.

V_{IK} Input Clamp Diode Voltage: The voltage on an input (-) when a specified current is pulled from that input.

V_{IL} Input LOW Voltage: The range of input voltages that represents a logic LOW in the system.

$V_{IL\ (Max.)}$ Maximum Input LOW Voltage: The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.

V_{ILD} Dynamic Input LOW Voltage: The maximum input voltage that is recognized as a LOW level during Multiple Output Switching (MOS) operation.

V_{OH} Output HIGH Voltage: The voltage at an output conditioned HIGH with a specified output load and V_{CC} supply voltage.

$V_{OH\ (Min.)}$ Output HIGH Voltage: The minimum voltage at an output terminal for the specified output current I_{OH} and at the minimum value of V_{CC}.

V_{OL} Output LOW Voltage: The voltage at an output conditioned LOW with a specified output load and V_{CC} supply voltage.

$V_{OL\ (Max.)}$ Output LOW Voltage: The maximum voltage at an output terminal sinking the maximum specified load current I_{OL}.

V_{OLP} Ground Bounce: Maximum (peak) voltage induced on a static LOW output during switching of other outputs.

V_{OLV} Ground Bounce: Minimum (valley) voltage induced on a static LOW output during switching of other outputs.

Voltages: All voltages are referenced to the ground pin. Negative voltage limits are specified as absolute values (i.e., -10.0V is greater than -1.0V).

VT+ Positive-Going Threshold Voltage: The input voltage of a variable threshold device (i.e., Schmitt Trigger) that is interpreted as a VIH as the input transition rises from below VT- (Min.).

VT- Negative-Going Threshold Voltage: The input voltage of a variable threshold device (i.e., Schmitt Trigger) that is interpreted as a V_{IL} as the input transition falls from above VT+ (Max.).

Radiation Results – Logic Summary

FACT (AC/ACT Advanced CMOS) logic is National's premier RHA-qualified, guaranteed 100 krad(Si) (R-level) radiation-tolerant logic product line. These products provide these radiation response characteristics:

- Neutron: $>10^{14}$ n/cm^2
- Total Ionizing Dose: 100 krad(Si)
- Dose Rate Upset: 1.9 x 10^9 rad(Si)/s at V_{CC} = 4.0 Vdc
- Dose Rate Latchup: $>10^{10}$ rad(Si)/s at V_{CC} = 5.5 Vdc and +117˚C
- Single Event Upset: LET = 40 MeV/mg/cm^2; cross-section 2 x 10^{-4} cm^2 device
- Single Event Latchup: LET = 120 MeV/mg/cm (does not latchup at LET = 120 MeV/mg/cm^2)

FACT CMOS products have no rebound effect at the 100 krad(Si) level. Therefore, the MIL-STD-883E, Method 1019.5 test for this effect is not required and is only performed as an engineering test for new product or when a major process change occurs.

With National Semiconductor's FACT™ logic, the only degraded parameters are I_{CC} (standby current) and I_{OZ} (TRI-STATE leakage current). Up to 100 krad, all other DC and AC parameters remain within published pre-rad limits.

Low dose rate total ionizing dose testing has been performed on FACT AC/ACT logic. Results indicate an improvement in the total dose response with regard to I_{CC} (standby leakage current) or I_{OZ} (TRI-STATE leakage current) – the only parameters that are affected by total ionizing dose. No other parameters or circuit functionality are affected.

FACT AC/ACT product has the electrical capability to operate using V_{CC} = 2 to 6 Vdc. By reducing V_{CC} to low voltage (such as 3.3 Vdc), the total dose response, dose rate latchup, and single event latchup are improved while dose rate and single event upset are degraded. Trade-offs must be considered when reducing V_{CC} in a particular application.

FACT Quiet Series (ACQ/ACTQ) logic uses similar manufacturing processes as National's FACT family. The additional circuitry used in FACT QS products causes the total dose response to be slightly degraded (50 - 100 krad) with respect to the three radiation-sensitive parameters:

Logic Family	Low Power	High Performance	Radiation Resistant
FACT™	√	√	√
FACT Quiet Series™	√	√	√
HC	√	–	–
HCS	√	–	√
F100K 300 Series ECL	–	√	√
FAST™	–	√	–
ALS	–	–	–
LS	√	–	√

I_{CC}, Input Leakage Current (affects some devices), and I_{OZ}. Single event upset and the effective LET are less than FACT Logic due to the reduction of the gate oxide thickness and the smaller feature size of FACT QS technology. Single event latchup capability remains the same (LET >120MeV/mg/cm^2). Dose rate characterization has not been performed by National Semiconductor. The neutron radiation level is greater than 10^{14} n/cm^2.

FACT FCT logic uses the same 1.5µm technology as FACT Quiet Series. The total dose response varies according to function. Single event upset and single event latchup are similar to FACT QS product. Dose rate testing performed on the 54FCT244 and 54FCT245 indicate no latchup or burn-out at 5.6E9 rad(Si)/s. Worst-case dose rate upset was 4.7E8 rad(Si)/s. Neutron radiation capability is greater than 10^{14} n/cm^2.

National Semiconductor's **F100K 300 Series ECL** logic is manufactured using FAST-LSI technology. Total ionizing dose testing shows the total dose capability of ECL product varies from function to function. The RHA capability for ECL has a range of 100 krad(Si) to 300 krad(Si). Single event effects testing shows that no latchup occurs up to an LET = 80 MeV/mg/cm^2. SEU occurs at an LET greater than 3 MeV/mg/cm^2. No dose rate testing has been performed by National Semiconductor.

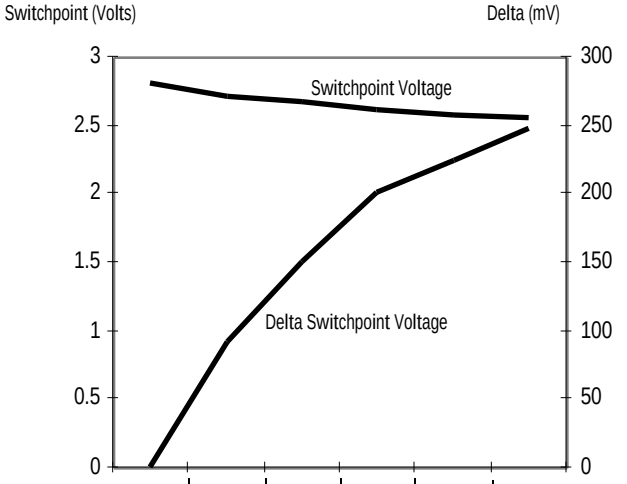
Total Dose Degradation of the Device's Switchpoint

An important design parameter for circuit designs is the switchpoint of a function. In the past, this parameter was not measured directly by an IC manufacturer, but was ver-

ified indirectly by measuring other parameters. The figure below shows the switchpoint of a 54AC08 Quad 2-Input AND Gate degrading very slowly with increasing total dose accumulation. The change in switchpoint value is less than 250mV and does not exceed switchpoint limits as established by using V_{OL} and V_{OH} measurements to validate these limits (1.85 V_{dc} and 3.65V_{dc}).

One variable that affects the circuit's switchpoint is the threshold voltage value of each "p" and "n" MOSFET. The figure below depicts the typical threshold voltage total dose radiation response for these CMOS transistors. It shows that the n-channel transistor degrades more slowly than the p-channel transistor. This degradation affects the edge rates of the function's output waveform. Because many different size transistors are used in the function's design, the switchpoint's degraded value represents the sum effect of the MOSFET's threshold voltage changes and other circuit parasitic effects as caused by the total dose environment. Therefore, when designing a radiation-hardened system, the switchpoint is more important than the individual MOSFET's total dose radiation response.

Switchpoint Degradation – 54AC08



Switchpoint	2.8	2.71	1.66	2.61	2.58	2.56
Sigma (+)	2.81	2.72	2.66	2.61	2.59	2.57
Sigma (-)	2.8	2.7	2.65	2.6	2.57	2.55
Delta (mV)	0	92	150	200	224	247

Inputs = High

Dose Rate = 129 rad(Si)/sec

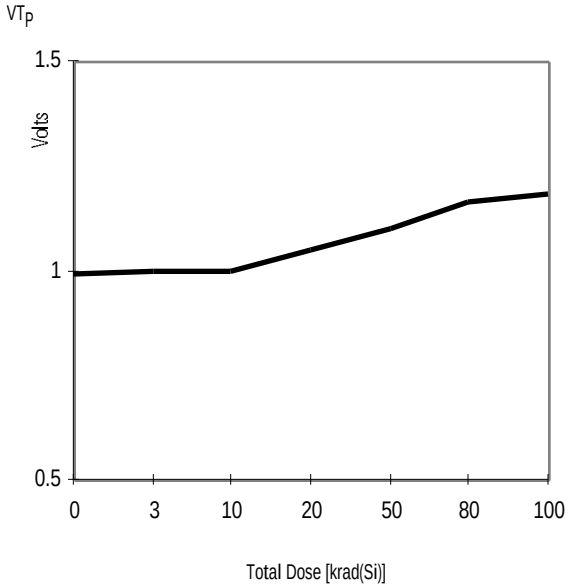
To control the process relative to radiation-induced defects, it is more important to understand individual transistor radiation responses at the IC fabrication level than at the system or circuit design level. As a MOSFET accumulates total dose, its threshold voltage changes due to the trapped charge generated in its gate oxide. The p-channel MOSFET is driven more toward the enhancement mode as total dose accumulation is increased. This generally results from trapped holes (positrons) in the gate oxide causing a more negative voltage level to turn ON the p-channel device. In the case of an n-channel CMOS transistor, as the total dose level is increased, the positive trap charge dominates at the lower values of accumulated total dose and the device is driven toward the depletion mode of operation. However, at a very high total dose level [300 - 450 krad(Si)], the threshold voltage begins to rebound and the device will start to become more "enhanced". This positive increase in the n-channel device threshold voltage results from the interface state generation dominating at the higher total dose level.

Trapped holes and interface states are competing effects. Trapped holes dominate at a high dose rate; interface states at a low dose rate. Other conditions which affect the generation of trapped holes and interface states are temperature and bias conditions.

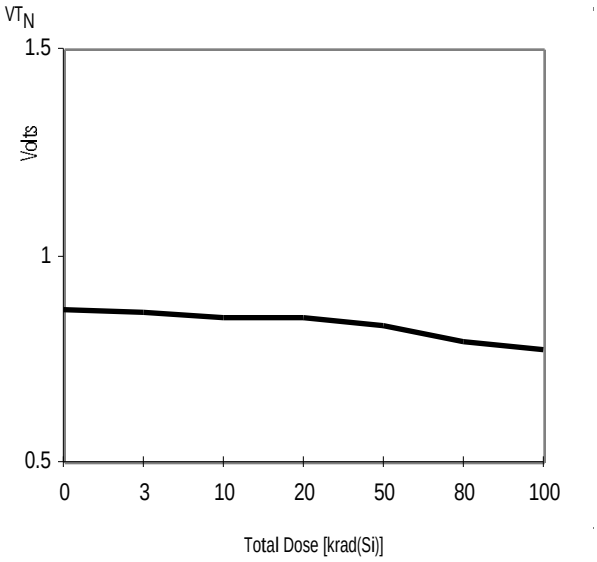
Radiation hard oxides are inefficient in generating trapped holes and interface states.

Thresholds (VT_N and VT_P) for FACT logic are shown below and on page 63.

FACT Thresholds – VT_P



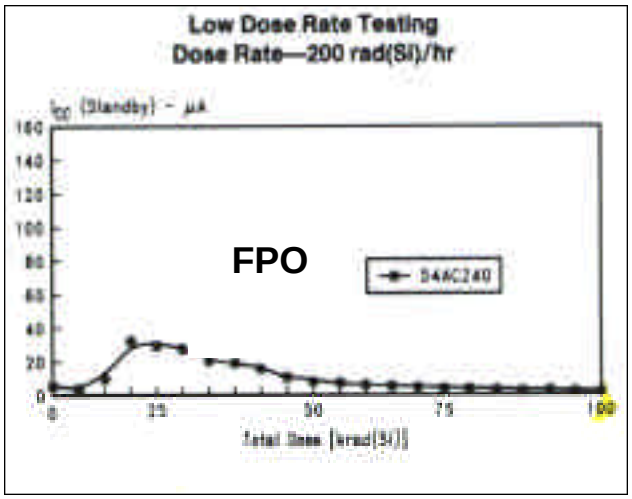
FACT Thresholds – VT_N



Low Dose Rate Irradiation Testing

Designing radiation-hardened space systems is difficult, especially when the radiation data is not representative of the environment. This is particularly true for the total ionizing dose that occurs in space. In space, the dose rate is very low (much less than 300 rad(Si)/hour) and the resulting radiation response is different from that simulated by MIL-STD-883, Method 1019, using the Cobalt-60 source. In general, the low dose rate condition dominates the space arena. However, there are certain situations in space where a system can experience a total dose level of 100 krad(Si) within one hour.

In a low dose rate condition, interface state generation manifests itself as the dominant mechanism for causing failure. The figure *(above right)* shows the typical response of a FACT 54AC240 Octal Buffer/Line Driver in a low dose rate Cobalt-60 test. The dose rate was 0.055 rad(Si)/sec. It took 522 hours to complete 110 krad(Si) total dose level. When this test result was compared with the high dose rate test results, the magnitude of the I_{CC} standby leakage current was reduced by a factor of 10 times. The current peak occurred at a much lower total dose level than at the high dose rate condition. The same response occurs for I_{OZ} (TRI-STATE leakage current) in a low dose rate environment. These are the only two parameters affected by total ionizing dose effects. Up to the 200 krad(Si) total dose level, FACT products are not severely affected by interface generation.

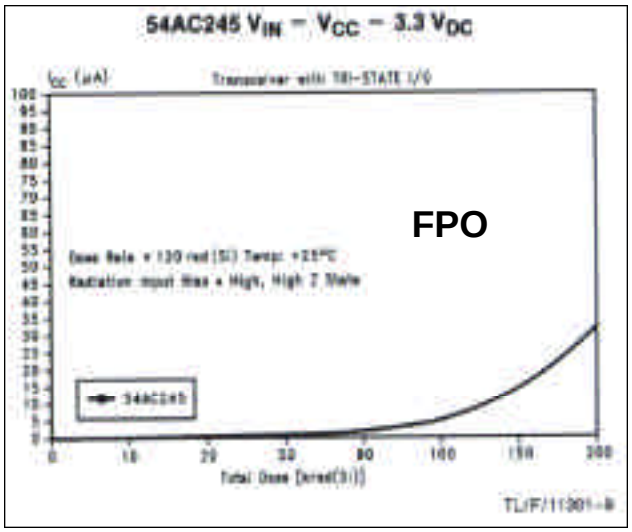


No other electrical parameter or circuit functionality is affected.

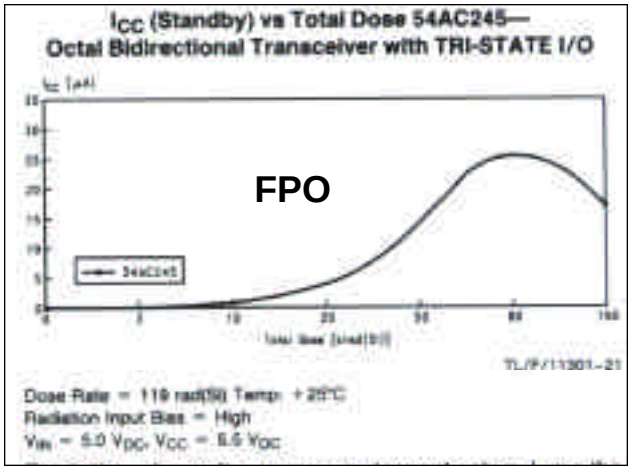
Low-Voltage Total Ionizing Dose Radiation Response

With the arrival of VHSIC technology and its insertion into military and space systems, low-voltage power supplies are becoming very popular. Low-voltage power systems are those supplies with 3.0V to 3.3V DC range. Such reduction in voltage levels has an impact on the radiation response of a system or integrated circuit.

Total dose testing has been conducted on the FACT 54AC245 Bidirectional Transceiver with TRI-STATE Input/Output. This device was irradiated by a Cobalt-60 source with 3.3V DC bias conditions. The results showed a significant improvement in the reduction of I_{CC} (standby) leakage current as compared with a radiation response using 5.5V DC bias conditions. The figure on



page 63 shows the standby leakage current response to total dose level of 200 krad(Si) at a dose rate of 119 rad(Si)/sec using low biasing voltage of 3.3V DC.



The figure above shows the total ionizing dose response at a dose rate of 120 rad(Si)/sec using 5.5V DC bias conditions.

Employing a low voltage power system not only reduces the magnitude of the radiation-induced leakage current, but also minimizes the threshold voltage shifts and the total dose enhancement of the "hot electron" effect. Dose rate and SEP (Single Event Phenomena) latchup performance are also improved.

Care must be exercised when using a low-voltage power system in a radiation environment. While improvements are observed as previously mentioned, there are trade-offs to be considered, particularly concerning non-radiation performance. However, one troublesome issue in the radiation environment is radiation-induced upset due to dose rate of SEP. As supply voltages are reduced, this function becomes likely to upset.

When there is full understanding of the total radiation environment as well as each system's particular design, low-voltage supply is a viable choice.

For additional information, please refer to National Semiconductor's Applications Note #AN-927 entitled *Total Dose Testing of Advanced CMOS Logic at Low Voltage.* This Applications Note is referenced in this Owner's Manual on page 91.

Dose Rate Test Results

Analysis of upset test data on the FACT 54AC299 8-Bit Universal Shift Register indicates that minimum upset threshold levels occurred under the worst-case conditions

54AC299 Dose Rate Upset Summary, Active Outputs

	Static Condition		Dynamic Condition	
V_{CC} S/N	4.0V [E9] rad(Si)	5.0V [E9] rad(Si)	4.0V [E9] rad(Si)	5.0V [E9] rad(Si)
50ns Upset Threshold				
11	6.11	8.44	5.66	–
12	6.54	8.50	4.65	–
13	6.29	7.99	4.74	–
14	6.39	8.02	5.34	–
15	5.69	8.26	4.65	–
16	5.42	8.11	4.85	–
17	6.35	8.13	4.87	–
18	6.11	8.10	4.79	–
19	5.99	7.84	4.40	–
20	6.29	7.68	4.94	–
Minimum	5.42	7.68	4.40	–
Maximum	6.54	8.50	5.66	–
Mean	6.11	8.11	4.89	–
1µs Upset Thresholds				
21	–	–	1.90	2.27
22	–	–	1.93	2.46
23	–	–	1.99	2.40
24	–	–	2.08	2.66
25	–	–	2.10	2.57
26	–	–	1.94	2.66
27	–	–	1.99	2.64
28	–	–	2.11	2.42
29	–	–	2.11	2.32
30	–	–	2.22	2.44
Minimum	–	–	1.90	2.27
Maximum	–	–	2.22	2.66
Mean	–	–	2.04	2.48

Latchup Test Results Static and Dynamic Condition

Radiation Pulse Width	Temperature			
	+25°C	+80°C	+100°C	+116°C
50ns	No latchup	No latchup	No latchup	No latchup
1µs	No latchup	No latchup	No latchup	No latchup

of a wide pulse (1µs), lowest V_{CC} voltage (4.0V DC), and the device under test (DUT) in the dynamic operating mode.

Measured minimum upset levels were 1.90 to 2.22 x 10^9 rad(Si)/sec. Narrow pulse (50ns) data demonstrated radiation upset levels from 4.40 to 5.66 x 10^9 rad(Si)/sec under dynamic operation.

The lowest threshold (for transient output as well as for internal upset) occurred with the outputs in the HIGH state and the radiation pulse occurring on the rising clock edge.

Power supply surge currents were associated with these radiation upset levels. Peak surge current values ranged between 300mA and 1000mA. The table on this page shows data for narrow pulse and wide pulse upset testing. While considerable effort was made to reduce and eliminate inductance, the final upset threshold levels may still be partially due to inductive effects, both internal and external to the 54AC299. Upset threshold levels in the high impedance (disabled) state of the DUT consist of:

- A state change in the internal storage elements
- Transient voltages at the I/O pins which could be falsely detected by interfacing circuitry as a change in logic state

The magnitude and duration of the transient voltages on the I/O pins in the disabled state were dependent on the output loading on these pins. Transient response was always positive-going with its amplitude rising with the increasing dose rate. These test results demonstrate that the transient characterization of the disabled state is complex without specific loading conditions and/or upset criteria being defined.

Using more resistive loading than reactive loading on I/O pins reduced the disabled sate recovery time. Disabled state testing also showed that the internal upset level was unaffected whether the output pin was active or disabled.

Upon completion of radiation upset testing, latchup and survivability tests were performed at +25˚C, +80˚C, +100˚C, and +166˚C for V_{CC} = 4.5V DC, 4.0V DC, and 5.5V DC, respectively. These results indicated no latchup occurred for either narrow pulse (50ns) or wide pulse (1ms) radiation. The radiation test level for narrow pulse was 10^{10} rad(Si)/sec at +25˚C. Due to heating of the circuit, the highest radiation level was limited at +116˚C to 7.5 x 10^9 rad(Si)/sec.

After completing latchup and survivability tests, verification of latchup windows was performed. Test results indicate no existence of latchup windows under worst-case conditions for narrow and wide pulse radiation. See pages 66 and 67 for dose rate characterization data.

For additional information, please refer to National Semiconductor's Applications Note #AN-924 entitled *Dose Rate Response of Advanced CMOS Products.* This Applications Note is referenced in this Owner's Manual on page 91.

Single Event Phenomena (SEP) Test Results

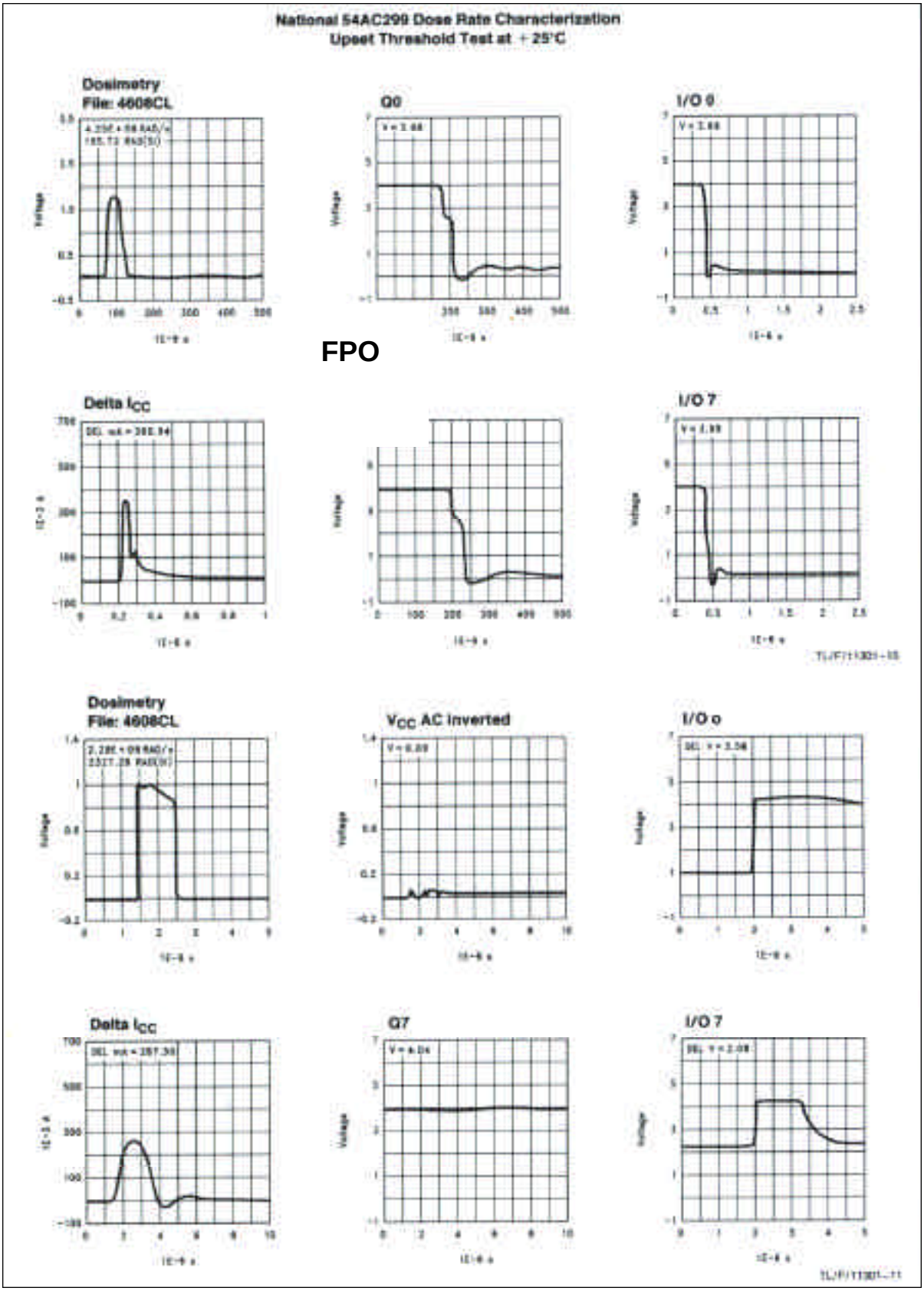
Space system designers require single event radiation test data. Independently performed single event radiation of FACT and other manufacturers' products was completed at the Lawrence Berkeley Laboratory's 88-inch cyclotron facility. Six types of heavy ion beams were employed to test the resilience of FACT (both AC and ACT versions) and other logic devices: xeon (603MeV), krypton (308meV), copper (90MeV), argon (180MeV), neon (90MeV), and nitrogen (67MeV).

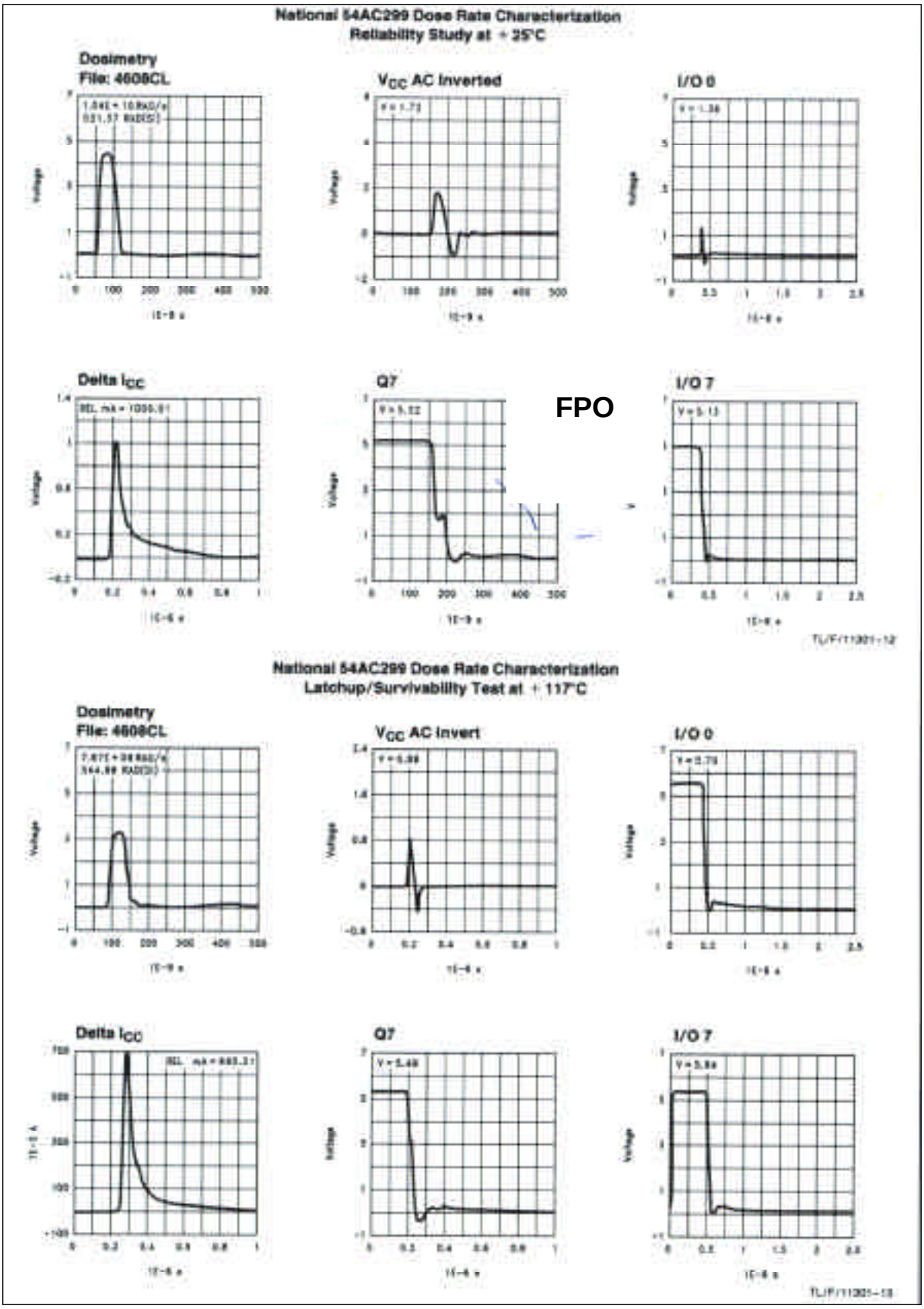
FACT test results were compared with similar functions in different technologies, such as AHC, HC, ALS, and LS. Tests demonstrated that FACT logic has higher resistance in the SEP cosmic ray environment than functionally equivalent devices in other process/design technologies.

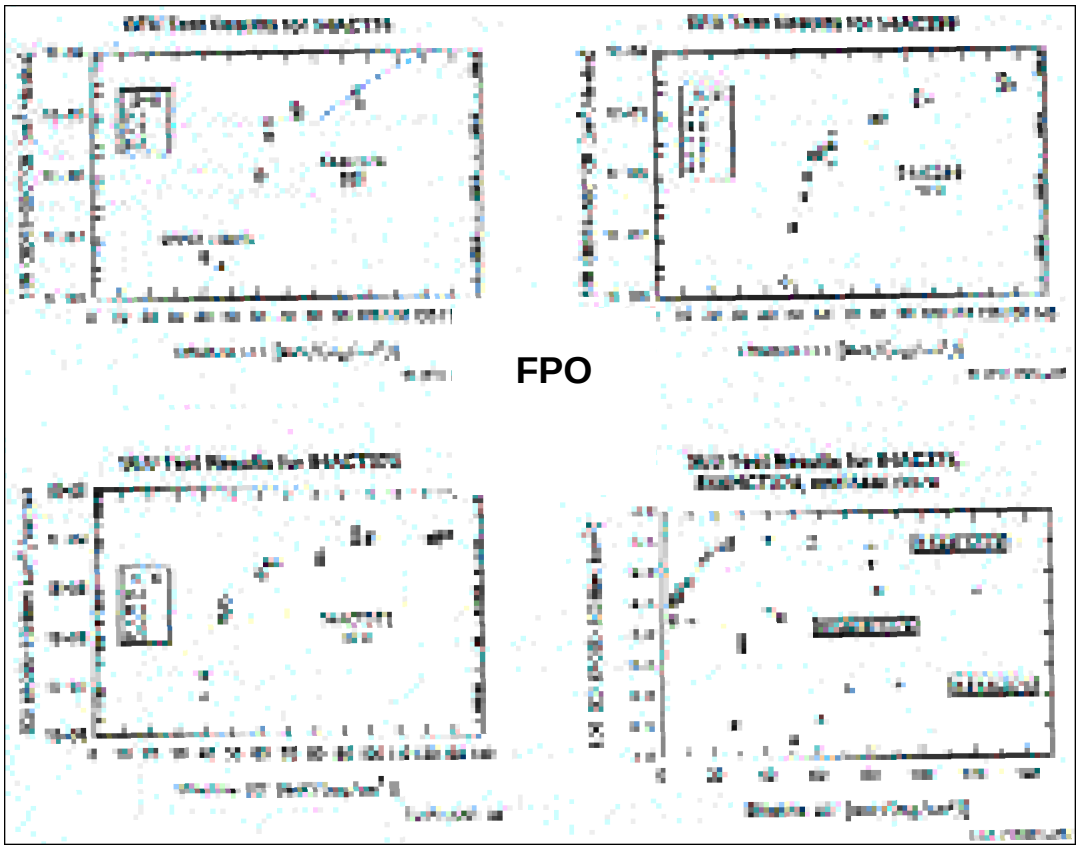
- FACT devices that were manufactured using National's JAN Class S Epi process (8µm) did not latchup for LET (Linear Energy Transfer) values between 40MeV to 120MeV/[(mg/cm^2)^2]. CMOS and

Summary of SEU Susceptibilities for FACT Logic

Device	Data Code	LET Threshold [MeV/((mg/cm^2)^2)]	Saturation Cross-Section (cm^2/device)
54AC163	8909	40	2 X 10^{-5}
54AC174	8922	55	3 X 10^{-5}
54AC299	8922	48	3 X 10^{-5}
54AC374	8840	50	2 X 10^{-6}
54ACT174	8920	60	9 X 10^{-5}
54ACT373	8948	40	2 X 10^{-4}


National 54AC299 Dose Rate Characterization
Upset Threshold Test at +25°C
Dosimetry
File: 4608CL
Q0
I/O 0
FPO
Delta ICC
I/O 7
Dosimetry
File: 4608CL
VCC AC Inverted
I/O o
Delta ICC
Q7
I/O 7


National 54AC299 Dose Rate Characterization
Reliability Study at + 25°C
Dosimetry
File: 4608CL
VCC AC Inverted
I/O 0
Delta ICC
Q7
FPO
I/O 7
TL/F/11301–12
National 54AC299 Dose Rate Characterization
Latchup/Survivability Test at + 117°C
Dosimetry
File: 4608CL
VCC AC Invert
I/O 0
Delta ICC
Q7
I/O 7
TL/F/11301–13

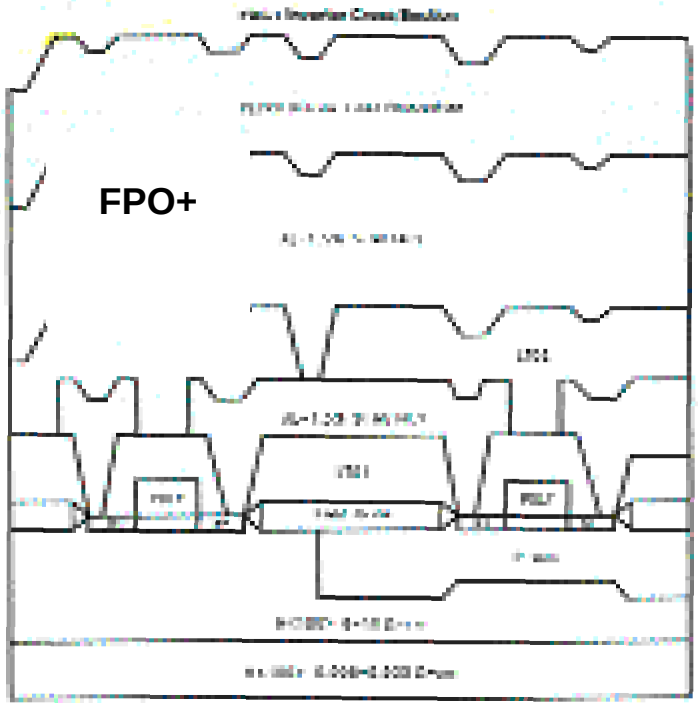


other devices manufactured on thick Epi layers (greater than 10µm) are suspect to latchup at these levels.

- Since no latchup was detected, an upper limit of the latchup cross-section was assigned at 10^{-9} cm^2/device for LET = 120MeV/[(mg/cm^2)^2].
- Latchup was detected in non-Epi processes.
- Testing demonstrated that FACT logic possesses large SEU LET threshold values in a range of 40 - 60 /[(mg/cm^2)^2].

FACT logic's high SEU LET threshold is much higher than most space-orbital flights will encounter. This means a reduction or elimination of circumvention circuits or EDAC methods for those systems that employ FACT product. This provides system designers with a solution that is cost effective and increases the level of SEP resistance.

For additional information, please refer to National Semiconductor's Applications Notes #AN-932 *(SEU and Latchup Tolerant Advanced CMOS Technology)* and #AN-989 *(Single Event Upset and Latchup Considerations for CMOS Devices Operated at 3.3V)*. Applications Notes are referenced in this Owner's Manual on page 91.



FACT Logic (AC and ACT)

FACT is the optimum logic family for radiation-resistant designs, providing low power, high performance, and radiation resistance to cost-effectively reduce weight and board space. FACT products are ideally suited for use in logic-based systems and for interfacing with ASIC designs in all applications requiring radiation-resistant devices.

FACT logic's resistance to ionizing radiation is attributable to a thin gate oxide, p-well design, and low temperature fab processing. Its Epi (epitaxial layer) and low resistivity substrate provide inherent latchup resistance under dose rate and SEP conditions. The FACT product portfolio spans the complexity gamut from the simplest SSI functions to high-speed octal buffers and drivers, as well as LSI functions. Guaranteed MIL-Class 3 (greater than 4,000 volts) electrostatic discharge (ESD) production is typical for all FACT functions. All FACT products are manufactured in a DSCC-certified QML wafer fabrication facility.

- FACT products are insensitive to neutron radiation up to 10^{14} neutrons/cm^2.
- Single Event Phenomena latchup is not a problem
- FACT AC/ACT RHA products are guaranteed to 100 krad(Si) with post irradiation parametric limits (PIPL).
- Low voltage (3 volts) parameters for 54ACxxx products begin to degrade between 300 - 500 krad(Si), depending on part type; for 54ACTxxx, 250 - 500 krad(Si). Normal (4.5V - 5.5V) functionality failures for some devices occur after 1 Mrad(Si).
- I_{CC} (standby current), I_{OZ} (TRI-STATE standby current), and I_{CCT} (54ACTxxx products) are the only DC parameters that are radiation sensitive and that may require change from National's MDS limits.
- All other parameters are within +25˚C Table 1 limits.
- Testing results vary from part type to part type due to inherent differences in internal device circuitry.

Total Dose Test Results

FACT logic provides high resistance in all radiation environments. For total ionization dose, its 100 krad(Si) capability provides the same post-irradiation drive as its pre-radiation value with propagation time deltas of less than 0.5ns (typical) at high dose rate levels. At lower space dose rates, FACT logic is superior to other logic families. FACT is resistant to total ionization radiation because of its thin gate oxide and low temperature processing.

NOTE: National only subjects its QML--certified FACT wafers to radiation testing.

National continues to qualify FACT devices to RHA (Radiation Hardness Assurance) standards. Select FACT QML devices bear an "R" designation as part of the JM38510 Slash Sheet number, denoting RHA certification to 100 krad(Si).

Rebound Testing Eliminated for FACT-RHA Products

The "Rebound Effect" (also known as Super Recovery) was reported in the early 1980s. As this effect became better understood, test techniques were developed and included in MIL-STD-883, Method 1019, Ionizing Radiation (Total Dose) Test Procedure for microcircuits. The Rebound Effect is an issue of a high total dose level that affects the CMOS n-channel MOSFET, is time dependent, and continues to increase its radiation degradation well after exposure to radiation has ceased. Because the Rebound Effect contributes to device failure in a low dose rate environment, it is a major concern of space system manufacturers.

The Rebound Effect is a failure mode for the CMOS threshold voltage parameter. More specifically, the n-channel threshold voltage shifts due to the total ionizing dose damage of the gate oxide. Rather than physical damage, there is ionization damage (i.e., generation of positive-trap oxide charges in the gate oxide).

Generation of radiation-induced interface traps in the gate oxide produce the Rebound Effect. As a result, two competing effects in the gate oxide cause modification in the n-channel threshold voltage. For the n-channel MOSFET, the positive oxide charge generates the threshold voltage to shift in the negative direction while interface traps cause the threshold voltage shift in the positive direction. Rebound is the recovery of the n-channel transistor's threshold voltage beyond its original designed value at pre-irradiation. The result is generated

by the annealing of the radiation-induced positive trapped oxide charges, thereby leaving interface traps in the gate oxide. The build-up of interface traps occurs at the SiO_2/Si interface and increases in density during irradiation and post-irradiation. The interface traps that occur in an n-channel device are negatively charged while the opposite is true for a p-channel device. Shown *(right)* is a typical example of a CMOS n-channel device showing threshold shift as a function of total dose.

As a result of the Rebound Effect, this presents a long-term reliability failure mode for space systems that have long life expectancy. At some point, the n-channel devices no longer functions due to excessive threshold voltage shift. The low dose rate of space allows the interface traps to dominate due to the self-annealing of positive trapped oxide changes.

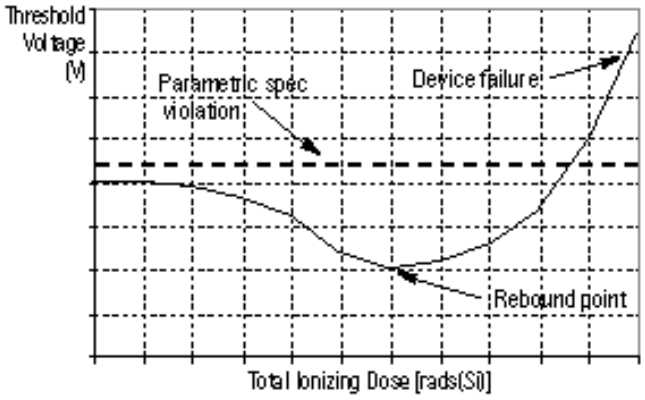
To address the Rebound Effect and its failure mode for selected CMOS technologies, the radiation community installed test techniques in MIL-STD-883, Method 1019. The test requires an additional 50% radiation overstress above the required total dose level. This irradiation was then followed by a one-week anneal under bias at +100˚C. Upon the completion of this thermal biased anneal, Group A electrical tests are performed to check for failures in functionality, propagation times, output drive current, output voltage, and out-of-state logic conditions.

Over the ensuing years, it has been learned that the Rebound Effect is dependent upon:

- Fabrication process
- Temperature at radiation and post-irradiation
- Bias conditions (bias voltage and bias circuit)
- Dose rate
- Total dose level

In order to eliminate the Rebound Test, National Semiconductor performed a design-of-experiments study that used burned-in FACT product. This test plan required Rebound Testing on at least one part type from each logic function group of the FACT family. Following are the devices that received JAN S burn-in and Rebound Testing:

- Gates: 54AC08, 54AC10, 54AC32
- Multiplexers: 54AC138, 54AC139
- Counter: 54AC161
- Buffer/Driver: 54AC244
- Transceiver: 54AC245
- Register: 54AC299
- D Flip-Flop: 54AC374 (two wafers, same lot)



Resulting Rebound Test data passed all of the required criteria as stated for acceptability. None failed the test. Contributing reasons for FACT product passing this test are:

- The gate oxide is thin enough to reduce the quantity of generated interface traps.
- At the RHA-qualified level of 100 krad(Si), the gate oxide of FACT product does not contain sufficient interface traps to cause failure — even with 50% radiation overstress. A higher total ionizing dose level is required before rebound testing would fail.

Additionally, 1992 - 1994 Rebound Test data on these unburned-in parts recorded no rebound failures:

- Gates: 54AC08 (two different wafers, same lot), 54AC10, 54AC14, 54AC20, 54AC86
- Multiplexers: 54AC138, 54AC139
- Counter: 54AC161
- Buffer/Driver: 54AC244
- Transceiver: 54AC245
- Register: 54AC299
- D Flip-Flop: 54AC374

Based upon the most recent DOE study and five years of historical rebound data, National is permitted to eliminate this requirement per MIL-STD-883E, Method 1019.5, paragraph 3.12.1.b, step 5. However, National will implement Rebound Testing as an Engineering Test or as a major change occurs (form, fit, function). National's present methodology is sufficient to indicate parametric drift or functionality issues that would support the need for the more comprehensive Rebound Test. National's FACT logic products are RHA qualified to 100 krad(Si) level and have a gate oxide thickness of 250Å ± 15Å.

Realistic Test Results for Low Dose Rate Applications

It was long recognized that MIL-STD-883E, Method 1019.4 did not accurately predict a microcircuit's low dose rate irradiation response. In particular, standby leakage (I_{CC}) and/or TRI-STATE® leakage currents were inaccurately represented. Test Method 1019.4 used a stated dose rate range of 50 - 300 rad(Si)/s which generated induced radiation leakage current values that were often high, unrealistic, and overly pessimistic. The Method's required dose rates were 10,000 to 60,000 times greater than those actualized in a space environment.

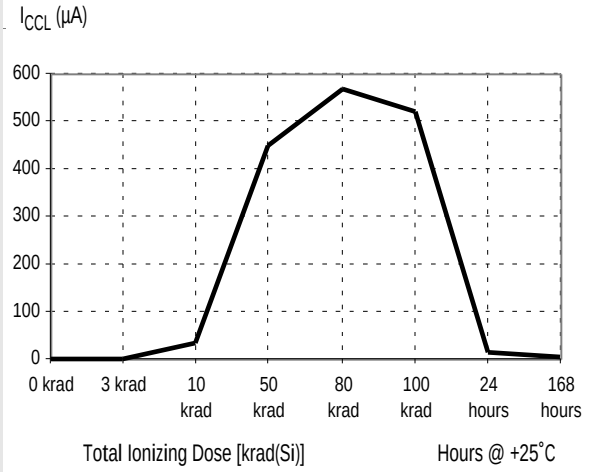
As a result of this high dose rate testing, many RHA products failed unnecessarily due to the inadequacy of this test method to simulate the low dose rate of space.

To address this overly pessimistic high dose rate irradiation testing, Sandia National Laboratories developed and recommended a new approach. as a standard in the 1991 and 1992 *IEEE Transactions on Nuclear Science*. National Semiconductor implemented this approach into a Design-of-Experiments (DOE) that was cost-effective, efficient, highly reliable, and simulated a low dose rate environment. This DOE used a one-week (168 hours), +25˚C (room temperature), biased anneal for FACT-RHA-qualified product. This approach:

- Better simulated the low-dose rate encountered in space (e.g., a more realistic approach)
- Was cost effective and efficient since it still allowed use of high dose rate irradiation while maintaining the same high reliability for RHA product

The new low dose rate irradiation approach helped to determine the acceptance or rejection of FACT-RHA product based on already established post-irradiation parametric limits in the slash sheet (JAN38510-xxxxx) or SMD (5962-xxxxx) documents.

FACT-RHA 54AC00
Standby Leakage Current vs. Total Ionizing Dose



New Low Dose Rate Irradiation Approach

- Establishes a more realistic total dose test method for the space environment
- Does not compromise existing radiation reliability levels
- Is cost effective
- Has been adopted by government agencies, and is recommended in radiation testing guideline (ASTM-F1892) as well as MIL-STD-883E, Method 1019.5

Original Design-of-Experiment

Phase I: This phase performed radiation total dose testing using the new low dose rate irradiation approach, and compared it with results obtained using a low dose rate Cobalt-60 source of 13.9 mrad(Si)/s (University of Massachusetts, Lowell). Both methods produced similar results, e.g., the new method was acceptable as a pass/fail test.

Phase II: This DOE determined the selectivity and sensitivity of the new method. RHA products were chosen that were declared acceptable by the new method, but had high leakage current values after irradiation (between 500µA - 700µA). Results showed less degradation than was expected. Therefore, the new proposed method was more conservative (factor of 3x).

RHA-Qualified FACT Logic – Test Results

FACT AC RHA Products

Product	JM38510/SMD Part Number	Parameter	RHA-M 3 krad(Si)	RHA-D 10 krad(Si)	RHA-P 30 krad(Si)	RHA-L 50 krad(Si)	RHA-R 100 krad(Si)	+25°C Anneal
54AC00	38510R75001	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC02	38510R75101	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC04	38510R75701	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC05	5962R9059001	I_{CCL}	50µA	100µA	700µA	700µA	700µA	700µA
		I_{CCH}	50µA	100µA	700µA	700µA	700µA	700µA
		I_{OHC}	15µA	50µA	100µA	100µA	100µA	100µA
54AC08	38510R75203	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC10	38510R75002	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC11	38510R75204	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC14	38510R75702	I_{CCL}	60µA	320µA	1.5mA	1.5mA	1.5mA	1.5mA
		I_{CCH}	60µA	320µA	1.5mA	1.5mA	1.5mA	1.5mA
54AC20	38510R75003	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC32	38510R75201	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC74	38510R75302	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC86	38510R75202	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC109	38510R75304	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC125	5962R9325301	I_{CCL}	15µA	100µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	100µA	700µA	700µA	700µA	700µA
		I_{CCZ}	15µA	100µA	700µA	700µA	700µA	700µA
		I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
		I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54AC138	38510R75802	I_{CCL}	15µA	100µA	1.7mA	1.7mA	1.7mA	1.7mA
		I_{CCH}	15µA	100µA	1.7mA	1.7mA	1.7mA	1.7mA
54AC139	38510R75803	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC153	38510R76202	I_{CCL}	50µA	200µA	1mA	1mA	1mA	1mA
		I_{CCH}	50µA	200µA	1mA	1mA	1mA	1mA
54AC157	38510R76203	I_{CCH}	15µA	100µA	700µA	700µA	700µA	700µA
		I_{CCL}	15µA	100µA	700µA	700µA	700µA	700µA

FACT AC RHA Products (cont.)

Product	JM38510/SMD Part Number	Parameter	RHA-M 3 krad(Si)	RHA-D 10 krad(Si)	RHA-P 30 krad(Si)	RHA-L 50 krad(Si)	RHA-R 100 krad(Si)	+25˚C Anneal
54AC161	38510R76302	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC163	38510R76304	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC169	5962R9160301	I_{CCL}	15µA	100µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	100µA	700µA	700µA	700µA	700µA
54AC174	38510R75307	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC175	5962R8955201	I_{CCL}	15µA	100µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	100µA	700µA	700µA	700µA	700µA
54AC191	38510R76305	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC240	38510R75703	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCZ}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{OZL}	-1µA	-3µA	-20µA	-20µA	-20µA	20µA
		I_{OZH}	1µA	3µA	20µA	20µA	20µA	20µA
54AC241	38510R75704	I_{CCL}	50µA	240µA	1.2mA	1.2mA	1.2mA	1.2mA
		I_{CCH}	50µA	240µA	1.2mA	1.2mA	1.2mA	1.2mA
		I_{CCZ}	50µA	240µA	1.2mA	1.2mA	1.2mA	1.2mA
		I_{OZL}	-1µA	-3µA	-20µA	-20µA	-20µA	-20µA
		I_{OZH}	1µA	3µA	20µA	20µA	20µA	20µA
54AC244	38510R75705	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCZ}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{OZL}	-1µA	-3µA	-20µA	-20µA	-20µA	-20µA
		I_{OZH}	1µA	3µA	20µA	20µA	20µA	20µA
54AC245	38510R75503	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCZ}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{OZL}	-1µA	-3µA	-20µA	-20µA	-20µA	-20µA
		I_{OZH}	1µA	3µA	20µA	20µA	20µA	20µA
54AC257	38510R76207	I_{CCL}	15µA	200µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	200µA	700µA	700µA	700µA	700µA
		I_{CCZ}	15µA	200µA	700µA	700µA	700µA	700µA
		I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
		I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54AC273	38510R75601	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA

FACT AC RHA Products (cont.)

Product	JM38510/SMD Part Number	Parameter	RHA-M 3 krad(Si)	RHA-D 10 krad(Si)	RHA-P 30 krad(Si)	RHA-L 50 krad(Si)	RHA-R 100 krad(Si)	+25˚C Anneal
54AC299	38510R76506	I_{CCL}	25µA	200µA	700µA	700µA	700µA	700µA
		I_{CCH}	25µA	200µA	700µA	700µA	700µA	700µA
		I_{CCZ}	25µA	200µA	700µA	700µA	700µA	700µA
		I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
		I_{OZL}	25µA	25µA	25µA	25µA	25µA	25µA
54AC373	38510R75403	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCZ}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{OZL}	-1µA	-3µA	-20µA	-20µA	-20µA	-20µA
		I_{OZH}	1µA	3µA	20µA	20µA	20µA	20µA
54AC374	38510R75602	I_{CCL}	15µA	100µA	1.2mA	1.2mA	1.2mA	1.2mA
		I_{CCH}	15µA	100µA	1.2mA	1.2mA	1.2mA	1.2mA
		I_{CCZ}	15µA	100µA	1.2mA	1.2mA	1.2mA	1.2mA
		I_{OZL}	-1µA	-3µA	-20µA	-20µA	-20µA	-20µA
		I_{OZH}	1µA	3µA	20µA	20µA	20µA	20µA
54AC520	5962R9091601	I_{CCL}	15µA	300µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	300µA	700µA	700µA	700µA	700µA
54AC521	5962R9098501	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
54AC541	38510R75711	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCZ}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{OZH}	1µA	3µA	20µA	20µA	20µA	20µA
		I_{OZL}	-1µA	-3µA	-20µA	-20µA	-20µA	-20µA
54AC574	38510R75604	I_{CCL}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCH}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{CCZ}	15µA	75µA	700µA	700µA	700µA	700µA
		I_{OZH}	1µA	3µA	20µA	20µA	20µA	20µA
		I_{OZL}	-1µA	-3µA	-20µA	-20µA	-20µA	-20µA

FACT ACT RHA Products

Product	JM38510/SMD Part Number	Parameter	RHA-M 3 krad(Si)	RHA-D 10 krad(Si)	RHA-P 30 krad(Si)	RHA-L 50 krad(Si)	RHA-R 100 krad(Si)	+25˚C Anneal
54ACT00	5962R8769901	I_{CCL}	75µA	300µA	1mA	1mA	1mA	1mA
		I_{CCH}	75µA	300µA	1mA	1mA	1mA	1mA
		I_{CCT}	1mA	1mA	3mA	3mA	3mA	3mA
54ACT74	5962R8752501	I_{CCL}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCH}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA

FACT ACT RHA Products (cont.)

Product	JM38510/SMD Part Number	Parameter	RHA-M 3 krad(Si)	RHA-D 10 krad(Si)	RHA-P 30 krad(Si)	RHA-L 50 krad(Si)	RHA-R 100 krad(Si)	+25˚C Anneal
54ACT109	5962R8853401	I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
54ACT138	5962R8755401	I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
54ACT151	5962R8875601	I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
54ACT157	5962R8968801	I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
54ACT161	5962R9172201	I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
54ACT163	5962R9172301	I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
54ACT240	5962R8775901	I_{CCL}	300µA	1mA	2mA	2mA	2mA	2mA
		I_{CCH}	300µA	1mA	2mA	2mA	2mA	2mA
		I_{CCZ}	300µA	1mA	2mA	2mA	2mA	2mA
		I_{CCT}	1mA	1mA	3mA	3mA	3mA	3mA
		I_{OZL}	-3µA	-10µA	-20µA	-20µA	-20µA	-20µA
		I_{OZH}	3µA	10µA	20µA	20µA	20µA	20µA
54ACT244	5962R8776001	I_{CCL}	300µA	1mA	2mA	2mA	2mA	2mA
		I_{CCH}	300µA	1mA	2mA	2mA	2mA	2mA
		I_{CCZ}	300µA	1mA	2mA	2mA	2mA	2mA
		I_{CCT}	1mA	1mA	3mA	3mA	3mA	3mA
		I_{OZL}	-3µA	-10µA	-20µA	-20µA	-20µA	-20µA
		I_{OZH}	3µA	10µA	20µA	20µA	20µA	20µA
54ACT245	5962R8766301	I_{CCL}	300µA	1mA	3mA	3mA	3mA	3mA
		I_{CCH}	300µA	1mA	3mA	3mA	3mA	3mA
		I_{CCZ}	300µA	1mA	3mA	3mA	3mA	3mA
		I_{CCT}	1.6mA	1.6mA	3mA	3mA	3mA	3mA
		I_{OZL}	-3µA	-10µA	-20µA	-20µA	-20µA	-20µA
		I_{OZH}	3µA	10µA	20µA	20µA	20µA	20µA
54ACT574	5962R8960101	I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCZ}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
		I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA

FACT Logic Products Proposed for RHA Qualifications – Test Results

FACT AC Products

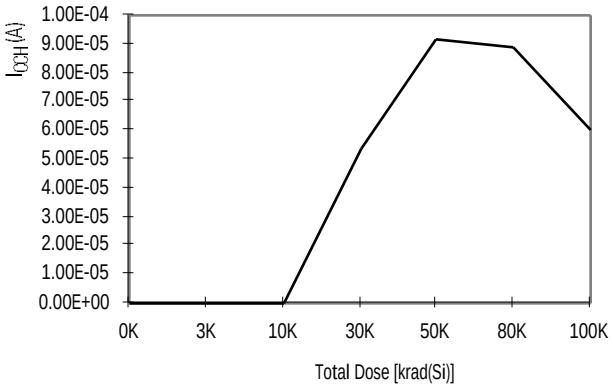
Product	Parameter	3 krad(Si)	10 krad(Si)	30 krad(Si)	50 krad(Si)	100 krad(Si)	+25°C Anneal
54AC151	I_{CCL}	50µA	200µA	700µA	700µA	700µA	700µA
	I_{CCH}	50µA	200µA	700µA	700µA	700µA	700µA
	I_{CCZ}	15µA	300µA	700µA	700µA	700µA	700µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54AC540	I_{CCL}	15µA	300µA	700µA	700µA	700µA	700µA
	I_{CCH}	15µA	300µA	700µA	700µA	700µA	700µA
	I_{CCZ}	15µA	300µA	700µA	700µA	700µA	700µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54AC646	I_{CCL}	25µA	200µA	700µA	700µA	700µA	700µA
	I_{CCH}	25µA	200µA	700µA	700µA	700µA	700µA
	I_{CCZ}	25µA	200µA	700µA	700µA	700µA	700µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54AC2525	I_{CCLQ5}	50µA	200µA	700µA	700µA	700µA	700µA
	I_{CCHQ5}	50µA	200µA	700µA	700µA	700µA	700µA

FACT ACT Products

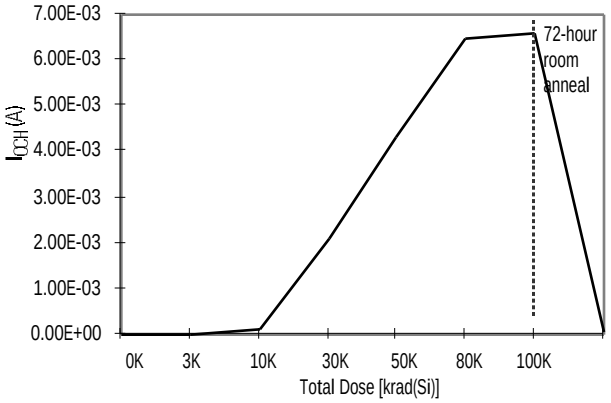
Product	Parameter	3 krad(Si)	10 krad(Si)	30 krad(Si)	50 krad(Si)	100 krad(Si)	+25˚C Anneal
54ACT174	I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCT}	1.6µA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
54ACT241	I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCZ}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{ZOH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54ACT257	I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCZ}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{ZOH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54ACT573	I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCZ}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{ZOH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54ACT825	I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCZ}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCT}	100µA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA

Typical Total Dose Response for FACT Logic
Worst-Case Bias Conditions

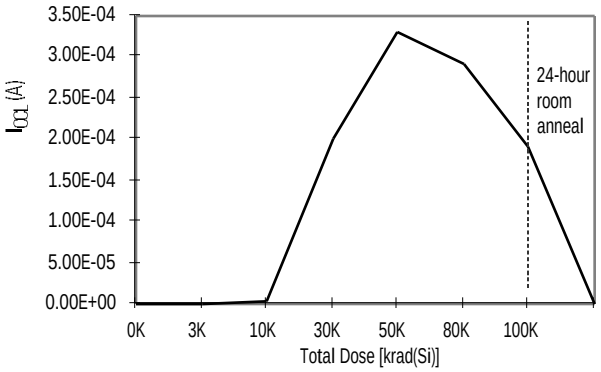
Typical FACT Gate Total Dose Response
54AC14: I_{CCH} (A) with Inputs = HIGH (max.)



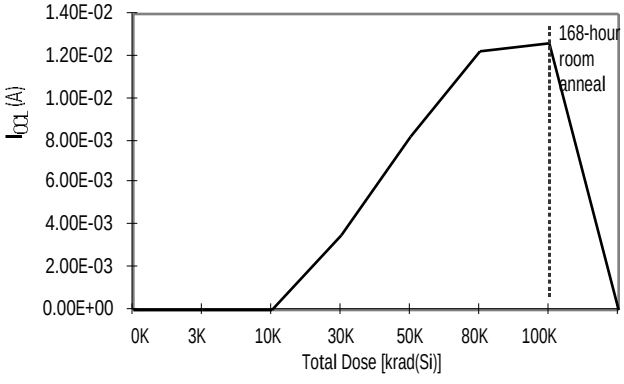
Typical FACT Buffer Total Dose Response
54AC244: I_{CCH} (A) with Inputs = HIGH (max.)



Typical FACT Octal Total Dose Response
54AC244: I_{CCL} (A) with Inputs = HIGH (max.)



Typical FACT Flip-FLop Total Dose Response
54AC257: I_{CCL} (A) with Inputs = HIGH (max.)



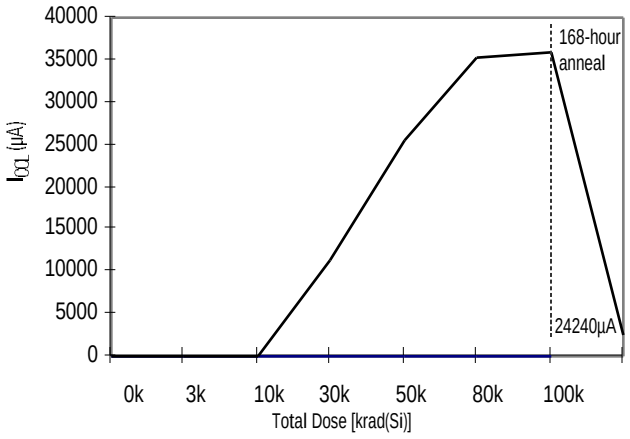
FACT Quiet Series Logic (ACQ and ACTQ)

Offering the lowest high-frequency emissions for high-speed technologies, FACT Quiet Series logic should be considered in any space system.

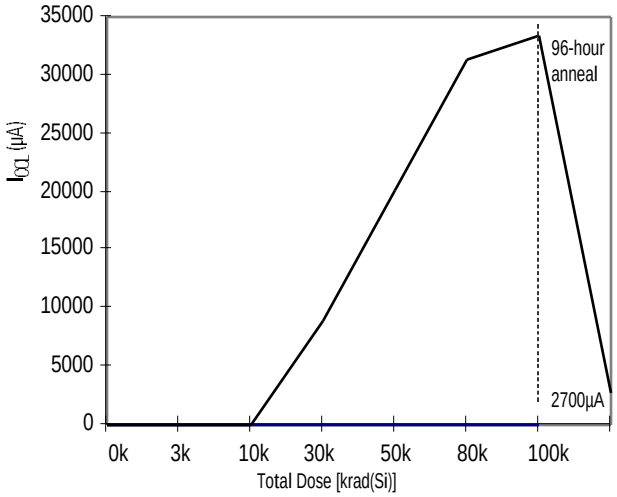
- Ideal ACMOS solution for noise-sensitive applications and asynchronous octal sockets. FACT Quiet Series (FACT QS) reduces EMI, ground bounce, undershoot, and other noise issues as well as increases dynamic threshold. This same circuitry is also incorporated in National Semiconductor's FACT FCT products.
- FACT QS circuitry retains standard pinout.
- 15% greater speed than standard FACT logic without increased power consumption.
- Design improvements greatly enhance performance and reliability, including output pin-to-pin propagation delay skew, higher electrostatic discharge (ESD) immunity, and higher latchup immunity. For clock distribution or for skew to similar output edges, the output skew is typically less than 500ps; worst case, 1ns. For bus applications or for skew to any output edge, skew is less than 800ps. For clock drivers where duty cycle is important, $t_{PLH} - t_{PHL}$ is within ± 500ps.
- MIL Class 3 (4,000V and greater) ESD immunity is guaranteed on most functions. Typical ESD immunity is 6,000V.
- Propagation delays as well as setup and hold times are specified identically to or faster than standard FACT.
- Epitaxial silicon essentially eliminates latchup possibility. FACT QS latchup immunity is tested to 300mA on the inputs and up to 1A on the outputs. Latchup immunity is specified at 300mA minimum at +125˚C.

Single event latchup for FACT Quiet Series products is identical with that of FACT logic. However, differences exist in single effects upset results due to the thinner gate oxide of FACT QS products.

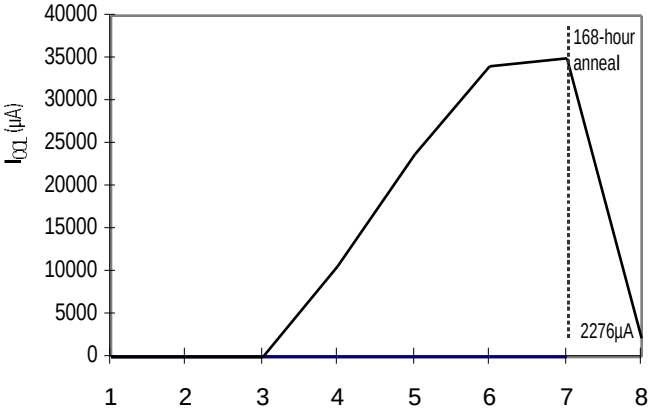
54ACTQ245 Total Dose Response: I_{CCL} (µA)



54ACTQ244 Total Dose Response: I_{CCL} (µA)



54ACTQ374 Total Dose Response: I_{CCL} (µA)



RHA-Qualified FACT QS Logic – Test Results

FACT Quiet Series ACTQ RHA Products

Product	JM38510/SMD Part Number	Parameter	RHA-M 3 krad(Si)	RHA-D 10 krad(Si)	RHA-P 30 krad(Si)	RHA-L 50 krad(Si)	RHA-R 100 krad(Si)	+25˚C Anneal
54ACTQ08	5962R8954702	I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	
		I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
54ACTQ32	5962R8973601	I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
54ACTQ245	5962R9218701	I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{IH}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
		I_{IL}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
		I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
		I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54ACTQ273	5962R8973501	I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
54ACTQ374	5962R9218901	I_{CCH}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCL}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCZ}	100µA	1mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
		I_{IH}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
		I_{IL}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
		I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
		I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA

FACT QS Logic Products Proposed for RHA Qualifications

FACT Quiet Series ACQ Products

Product	Parameter	3 krad(Si)	10 krad(Si)	30 krad(Si)	50 krad(Si)	100 krad(Si)	+25˚C Anneal
54ACQ240	I_{CCH}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCL}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCZ}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{IL}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{IH}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54ACQ245	I_{CCH}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCL}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCZ}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{IL}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{IH}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54ACQ373	I_{CCH}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCL}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCZ}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{IL}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{IH}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54ACQ374	I_{CCH}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCL}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCZ}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{IL}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{IH}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54ACQ573	I_{CCH}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCL}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCZ}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{IL}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{IH}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA

FACT Quiet Series ACTQ Products

Product	Parameter	3 krad(Si)	10 krad(Si)	30 krad(Si)	50 krad(Si)	100 krad(Si)	+25˚C Anneal
54ACTQ240	I_{CCH}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCL}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{IL}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{IH}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54ACTQ241	I_{CCH}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCL}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{IL}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{IH}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54ACTQ244	I_{CCH}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCL}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{IL}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{IH}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54ACTQ373	I_{CCH}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCL}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{IL}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{IH}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54ACTQ573	I_{CCH}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCL}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{IL}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{IH}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA
54ACTQ574	I_{CCH}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCL}	100µA	1.0mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{CCT}	1.6mA	1.6mA	3.5mA	3.5mA	3.5mA	3.5mA
	I_{IL}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{IH}	0.1µA	0.1µA	1.0µA	1.0µA	1.0µA	1.0µA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA	-25µA

FACT FCT Logic

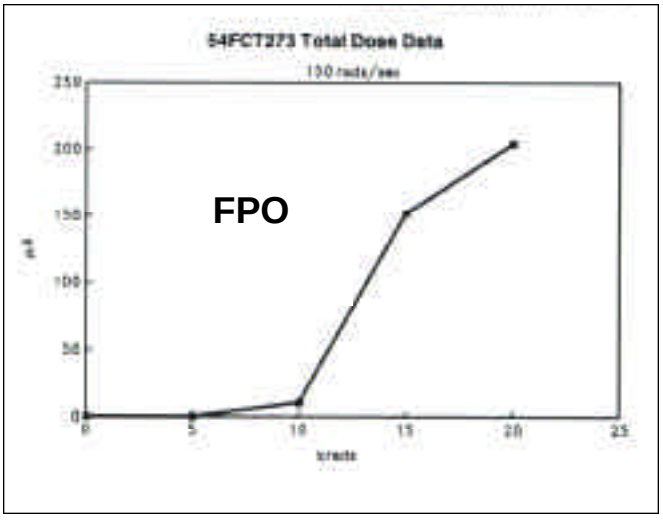
Dual-marked as MIL-STD-883E and SMD, FACT FCT logic devices help military and aerospace designers get the most out of their high-performance systems. For high-speed VME bus applications at low CMOS power consumption levels, this is the family of choice.

- Enhanced noise immunity for improved undershot (typically less than 0.5V) and ringing characteristics – lower than competitive FCT products. By reducing voltage swing for less device-generated noise, this minimized undershoot also protects the inputs of RAMs, PLDs, and interface devices.
- The split ground bus isolates input ground from output ground for improved dynamic threshold.
- Guaranteed current latchup immunity of 100mA at +125˚C; typical, 1A.
- Guaranteed MIL Class 2 (2,000V to 3,999V) ESD tolerance. Typical FACT FCT ESD tolerance is 6,000V.
- Fabricated using the same process technology as the FACT family.
- Pin-compatible replacement for competitive FCT devices. SCDs may include processing to Level S and radiation-resistant specifications.

FACT FCT Dose Rate Response

Dose Rates rad(Si)/sec	54FCT244	54FCT245
1.1E8	No latchup or burnout	
3.1E8		
4.7E8		
1.1E9		
5.6E9		
54FCT244 upset at 1.1E9 rad(Si)/sec		
54FCT245 upset at 4.7E8 rad(Si)/sec		

Data courtesy of Raytheon Corporation



F100K 300 Series ECL Logic

Performing at clock speeds of up to 400MHz, National's F100K 300 Series' 750ps (typical) switching speeds allow mil/aero designers to eliminate speed bottlenecks in systems such as satellite communications, digital signal processing, radar, avionics, navigation, telecommunications, and portable instrumentation. All F100K 300 Series devices are plug-pin compatible replacements for existing 100 Series sockets and easily interface with all ECL I/O devices (ASICs, PALs, and SRAMs).

The FAST-LSI process is used for National's F100K 300 Series products. Similar to the FAST-Z process used with National's now obsolete F100K 100 Series, it has many advantages that helped achieve the lower power consumption, higher ESD tolerance, and wider voltage range of the 300 Series. These improved ECL features make F100K 300 Series ECL devices attractive candidates for space projects.

Product Testing

National's F100K 300 Series ECL has undergone preliminary investigation to determine its minimum radiation hardness level. Total dose irradiation tests have been performed on the:

- The lowest power, easiest-to-use ECL logic to be fully compliant to MIL-STD-883 and available as an SMD
- Specified parametric testing across the entire military temperature range
- AC and DC performance specified over the entire -4.2V to -5.7V voltage range for easy interface with 100K ECL I/O devices and upgrades for systems employing 10K and 10KH logic
- ESD protection is guaranteed at MIL Class 2 (2,000V to 3,999V); typical immunity is 4000V
- Devices typically consume 30% to 50% less power per gate than functionally equivalent F100K 100 Series devices
- Full voltage and temperature compensation is guaranteed

Glossary of ECL Logic-Specific Terms

AC Switching Parameters

f_{COUNT} (Count Frequency/Toggle Frequency/Operating Frequency): The maximum repetition rate at which clock pulses may be applied to sequential circuit. Above this frequency the device may cease to function.

t_h (Hold Time): The interval immediately following the active transition of the timing pulse (usually the clock ulse) or following the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its continued recognition.

t_{PLH} (Propagation Delay Time): The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} (Propagation Delay Time): The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined HIGH level to the defined LOW level.

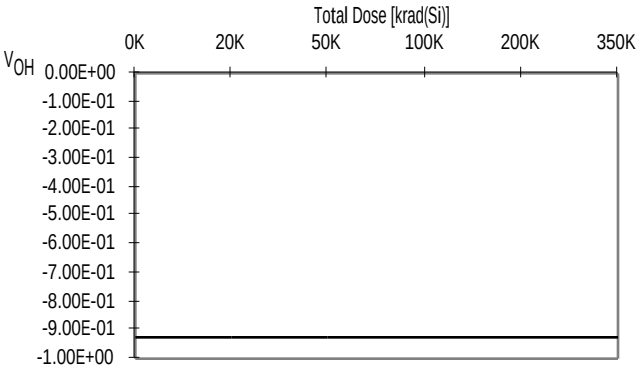
t_S (Setup Time): The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its recognition.

t_S (Release Time): The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the master set or reset must be released (inactive) to ensure valid data is recognized.

t_{TLH} (Transition Time, LOW to HIGH): The time between two specified reference points on a waveform which is changing from LOW to HIGH.

t_{THL} (Transition Time, HIGH to LOW): The time between two specified reference points on a waveform which is changing from HIGH to LOW.

100325: V_{OH} with Inputs = LOW (max.)

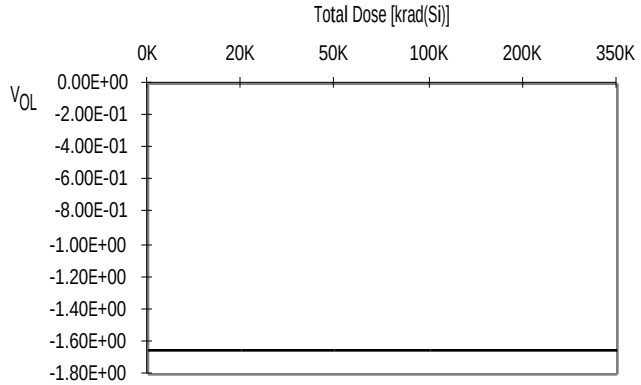


- **F100355 Low Power Quad Multiplexer/Latch** – The F100355 contains four transparent latches, each of which can accept and store data from two sources. This device was chosen to represent the pure F100K 300 Series ECL circuitry, i.e., ECL input to ECL output.
- **F100325 Low Power Hex ECL-to-TTL Translator** – This device was chosen to represent mixed ECL/TTL circuitry, in this case converting ECL F100K logic levels to TTL logic levels.

Since ECL uses such high current, there is no "leakage" parameter which can be used to monitor radiation response (i.e., CMOS uses I_{CC}). Therefore, the input threshold (or internal reference voltage) is considered to be the most sensitive parameter to observe for radiation effects.

The following graphs represent plots of V_{OLC} and V_{OHC} versus total dose radiation exposure. V_{OLC} and V_{OHC} are the "corner point" output level tests, performed using threshold value inputs such as V_{IH} (mini-

100336: V_{OL} with Inputs = LOW (max.)



t_{pw} (Pulse Width): The time between 50 percent amplitude points on the leading and trailing edges of a pulse.

t_{PHZ} (Output Disable Time of a TRI-STATE Output from High Level): The time between the 1.5V level on the input and a voltage 0.3V below the steady state output HIGH level with TRI-STATE output changing from the defined HIGH level to a high impedance (OFF) state.

t_{PLZ} (Output Disable Time of a TRI-STATE Output from LOW Level): The time between the 1.5V level on the input and a voltage 0.3V above the steady state output LOW level and with the TRI-STATE output changing from the defined LOW level to a high impedance (OFF) state.

tPZH (Output Enable Time of a TRI-STATE Output to a HIGH Level): The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a HIGH level.

t_{PZL} (Output Enable Time of a TRI-STATE Output to a LOW Level): The time between the 1.5V levels of the input and output waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a LOW level.

Currents

Positive current is defined as conventional current flow *into* a device lead. Negative current is defined as conventional current flow *out* of a device lead.

I_{EE} (Power Supply Current): The current required by each device from the V_{EE} supply. This value represents only the internal current required by the specified device, and does not include the current required for loads or terminations.

I_{TTL} (Supply Current): The current flowing into the V_{TTL} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst-case operation.

I_{IH} (Input Current HIGH): The current flowing into a device lead with the specified V_{IH} applied to the input. This value represents the worst-case DC input load that a device presents to a driving element.

I_{IL} (Input Current LOW): The current flowing into a device lead wit the specified V_{IL} applied to the input.

I_{OH} (Output HIGH Current): The current flowing out of the output when it is in the HIGH state. For a turned-off open-collector output

with a specified HIGH output voltage applied, the I_{OH} is the leakage current.

I_{OL} (Output LOW Current): The current flowing into an output when it is in the LOW state.

I_{OS} (Output Short Circuit Current): The current flowing out of a HIGH-state output when that output is short circuited to ground (or other specified potential.

I_{OZH} (Output OFF Current HIGH): The current flowing into a disabled TRI-STATE output with a specified HIGH output voltage applied.

I_{OZL} (Output OFF Current LOW): The current flowing out of a disabled TRI-STATE output with a specified LOW output voltage applied.

Voltages

All voltage values are referenced to V_{CC} (or ground) which is the most positive potential in an ECL system.

V_{BB} (Bias Voltage): The internally generated reference voltage which is used to set the input and output threshold levels.

V_{CC} (Circuit Ground): This is the most positive potential in the ECL system and it is used as the reference level for other voltages.

V_{CCA} (Separate Circuit Ground): The circuit ground for the buffered current switch. Outside the package, the V_{CC} and V_{CCA} leads should be connected to the common V_{CC} distribution. Internally, the separation of V_{CC} and V_{CCA} insures that any change in load currents during switching does not cause a change in V_{CC} through the small but finite inductance of the V_{CCA} bond wire and package lead.

V_{CS} (Current Source Voltage): The internally generated potential used to control the level of the active current source.

V_{EE} (Power Supply Voltage): This potential is the system power supply voltage and it is the most negative potential in the system.

V_{EES} (Substrate V_{EE}): These pins (on the PCC package only) provide extra thermal conduction paths, therefore reducing thetaJA. These pins must be connected to the V_{EE} plane or not connected at all.

V_{TTL} (Supply Voltage): The range of the TTL power supply voltage over which the device is guaranteed to operate within the specified limits.

V_{IH} (Input Voltage HIGH): The range of input voltages that represents a logic HIGH level in the system.

$V_{IH\ (Max.)}$: The most positive V_{IH}.

$V_{IH\ (Min.)}$: The most negative V_{IH}. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} (Input Voltage LOW): The range of input voltages that represents a logic LOW level in the system.

$V_{IL\ (Max.)}$: The most positive V_{IL}. This value represents the guaranteed input LOW threshold for the device.

$V_{IL\ (Min.)}$: The most negative V_{IL}

V_{OH} (Output Voltage HIGH): The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a HIGH level at the output.

$V_{OH\ (Max.)}$: The most positive V_{OH} under the specified input and loading conditions.

$V_{OH\ (Min.)}$: The most negative V_{OH} under the specified input and loading conditions.

V_{OHC}: The output HIGH corner point or guaranteed HIGH threshold voltage with the inputs set to their respective threshold levels.

V_{OL} (Output Voltage LOW): The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a LOW level at the output.

$V_{OL\ (Max.)}$: The most positive V_{OL} under the specified input and loading conditions.

$V_{OL\ (Min.)}$: The most negative V_{OL} under the specified input and loading conditions.

V_{OLC}: The output LOW corner point or guaranteed LOW threshold voltage with the inputs set to their respective threshold levels.

V_{NH} (HIGH Level Noise Margin): Noise margin between the output HIGH level of a driving circuit and the input HIGH threshold level of its driven load. A conservative value for V_{NH} is the difference between V_{OHC} and $V_{IH\ (Min.)}$.

V_{NL} (LOW Level Noise Margin): Noise margin between the output LOW level of a driving circuit and the input LOW threshold level of its driven load. A conservative value for V_{NL} is the difference between $V_{IL\ (Max.)}$ and V_{OLC}.

mum) and V_{IL} (maximum). For both devices, there is essentially no shift in the output levels from the radiation exposure.

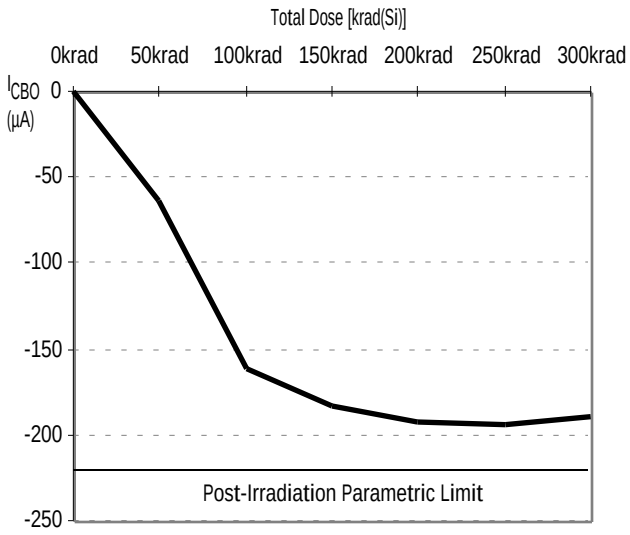
NOTE: The 100325 is unique as it has positive TTL-level outputs as well as an external ECL-level V_{BB} (the reference voltage) output. To plot V_{BB}, the absolute value was used.

These results are preliminary and based on limited testing of two device functions. It is strongly recommend that total dose radiation-hardened-assured F1003xx ECL product be purchased only on a wafer-by-wafer basis.

ECL and Single Event Effects

National Semiconductor's Emitter-Coupled Logic (ECL) family was evaluated for Single Event Upset (SEU) and Single Event Latchup (SEL) responses. Two parts were investigated: 100331 Low Power Triple D Flip-Flop and 100341 Low Power 8-Bit Shift Register. The F100K 300 Series ECL family is the latest ECL product being fabricated using the advanced isoplanar technology called FAST-LSI. While ECL technology in general consumes more power than CMOS technology, the 300 Series has been designed to consume less power than other ECL processes.

100314 Radiation Response – I_{CBO}



The SEE testing indicated that the parts did not latchup to an LET > 70MeV/mg/cm^2 and SEU testing showed an LET = 3 to 5 MeV/mg/cm^2. The sensitivity to SEU is a result of the ECL devices are continuously in a non-saturated state. For additional information, please see the paper entitled *Ion-Induced Charge Collection and SEU Sensitivity of Emitter-Coupled Logic (ECL) Devices* on page 93 of this Owner's Manual.

F100K 300 Series ECL Products – Test Results

Product	Parameter	3 krad(Si)	10 krad(Si)	50 krad(Si)	100 krad(Si)	300 krad(Si)	+25°C Anneal
100302	All Parameters	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad			Not applicable
100304	All Parameters	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad		Not applicable
100307	All Parameters	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad		Not applicable
100313	All Parameters	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad		Not applicable
100314	I_{CB0}	-250µA	-250µA	-250µA	-250µA	-250µA	Not applicable
100315	I_{CB0}	-250µA	-250µA	-250µA			Not applicable
100325	All Parameters	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Not applicable
100331	All Parameters	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Not applicable
100336	All Parameters	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad		Not applicable
100351	All Parameters	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad		Not applicable

SCAN System & Board Test Logic (IEEE 1149.1)

National Semiconductor's SCAN (Serial Controlled Access Network) products add system and/or board testability while lowering the lifetime cost of ownership for military/aerospace systems. All SCAN products conform to the IEEE 1149.1 standard as established by the Joint Test Action Group (JTAG). By including SCAN products, a system manufacturer can detect design errors, manufacturing mistakes, and defective components while reducing tester time, increasing quality, and reducing time to market.

SCAN products support design for testability. With newer technologies being developed every 18 to 24 months, testability is becoming a major problem since it impacts productivity and future technological advances in other areas of the process. By using National's SCAN product software (SCANEASE), IEEE Standard 1149.1 board designs will provide significant advantages over competitive options.

National's radiation-tolerant CMOS SCAN products are manufactured on the 1.5µm CMOS FACT process. The expected radiation tolerance for CMOS SCAN product is between 30 to 50 krad(Si) for total ionizing dose. Built on the identical CMOS-epi wafer as FACT logic, CMOS SCAN products exhibit the same latchup immunity in the dose rate and single event upset environments. Dose rate upset and single event upset vary from function to function. Neutron levels up to 10E14 n/cm^2 do not effect CMOS products.

SCAN Logic Products Proposed for RHA Qualifications

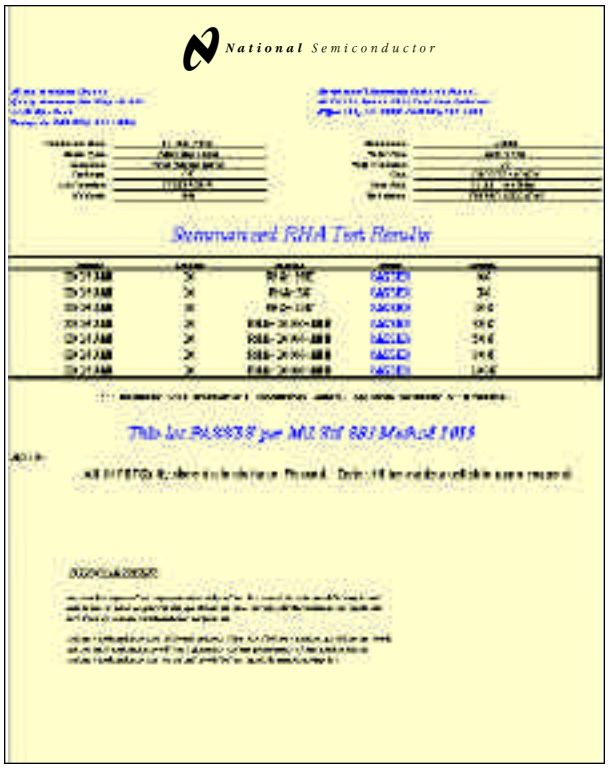
(Compliant to IEEE 1149.1)

Product	Parameter	3 krad(Si)	10 krad(Si)	30 krad(Si)	50 krad(Si)	+25°C Anneal
SCAN18Y541	I_{CCLQM}	1.0mA	1.5mA	3.5mA	5.5mA	5.5mA
	I_{CCHQM}	1.0mA	1.5mA	3.5mA	5.5mA	5.5mA
	I_{CCZQM}	1.0mA	1.5mA	3.5mA	5.5mA	5.5mA
	I_{CCT}	1.6mA	1.6mA	3.5mA	5.5mA	5.5mA
	I_{CCTRMX}	1.6mA	1.6mA	3.5mA	5.5mA	5.5mA
	I_{CCTRQ}	1.0mA	1.6mA	3.5mA	5.5mA	5.5mA
	I_{OZH}	25µA	25µA	25µA	25µA	25µA
	I_{OZL}	-25µA	-25µA	-25µA	-25µA	-25µA

Logic Final Reports

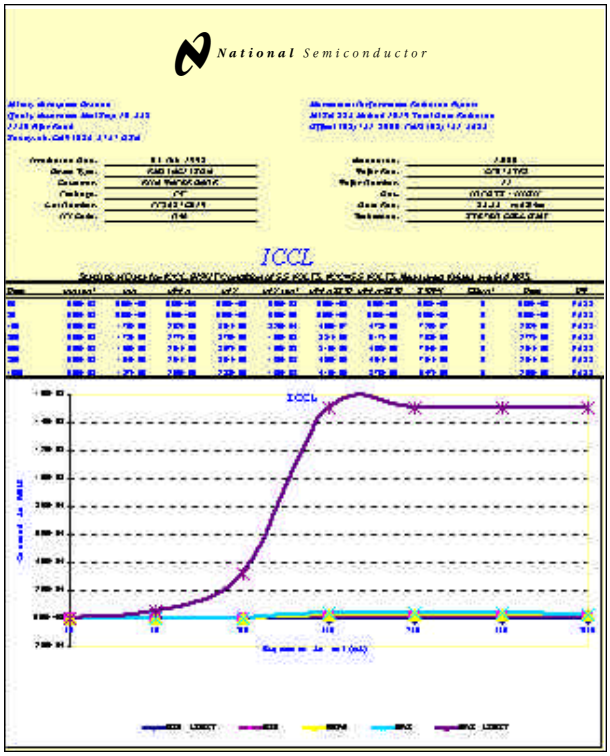
Cover Page Example

Includes:
- Product information
- Traceability
- Comprehensive test results
- Lot pass/fail status



Test Report Example

Includes:
- Test names from National Semiconductor datasheet or Customer Drawing
- Product information
- Statistical summary
- Test pass/fail status
- Graphic summary



Report Header Example

Includes:
- Corporate header and contact information
- Comprehensive product information
- Traceability

Logic test reports are available on National Semiconductor's web site at www.national.com/mil.

Report Statistics Example

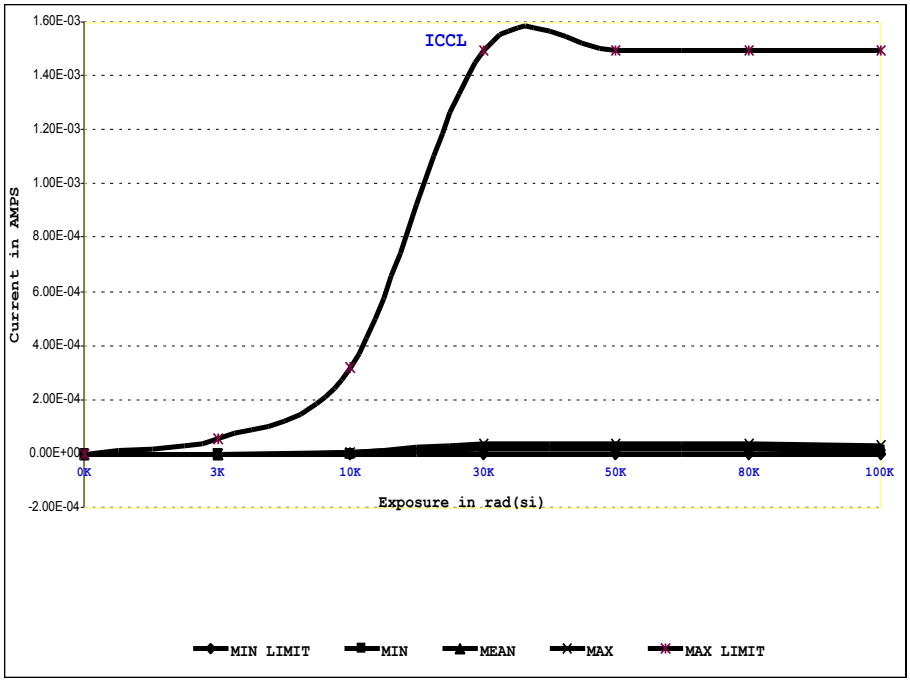
Includes:

- Test names from National Semiconductor's datasheet or Customer Drawing
- Summarized test results by exposure level
- Test limits from test program
- Statistical values

ICCL

Statistical Data for ICCL, INPUT Condition of 5.5 VOLTS, VCC=5.5 VOLTS. Measured Values are in AMPS.

Dose	MIN LIMIT	MIN	MEAN	MAX	MAX LIMIT	MEAN-3STD	MEAN+3STD	STDEV	COUNT	Delta	P/F
0K	-5.00E-08	0.00E+00	0.00E+00	0.00E+00	9.00E-08	0.00E+00	0.00E+00	0.00E+00	6	0.00E+00	PASS
3K	-5.00E-08	0.00E+00	0.00E+00	0.00E+00	6.00E-05	0.00E+00	0.00E+00	0.00E+00	6	0.00E+00	PASS
10K	-5.00E-08	1.75E-06	2.62E-06	3.51E-06	3.20E-04	4.60E-07	4.78E-06	7.20E-07	6	-2.62E-06	PASS
30K	-5.00E-08	1.78E-05	2.77E-05	3.76E-05	1.50E-03	3.81E-06	5.17E-05	7.98E-06	6	-2.77E-05	PASS
50K	-5.00E-08	1.66E-05	2.61E-05	3.67E-05	1.50E-03	3.16E-06	4.90E-05	7.64E-06	6	-2.61E-05	PASS
80K	-5.00E-08	1.64E-05	2.51E-05	3.51E-05	1.50E-03	4.06E-06	4.61E-05	7.01E-06	6	-2.51E-05	PASS
100K	-5.00E-08	1.37E-05	2.06E-05	2.83E-05	1.50E-03	4.19E-06	3.70E-05	5.47E-06	6	-2.06E-05	PASS



Report Graph Example

Includes:

- Graphic rendition of information