Table of Contents – Interface

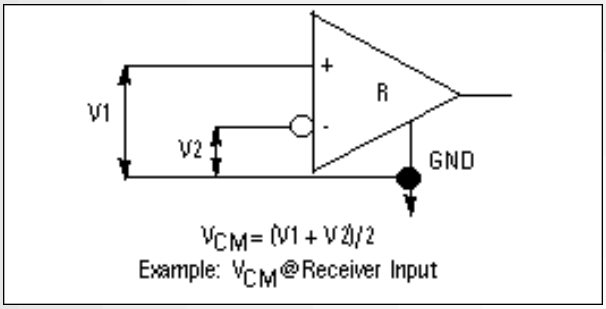
National Semiconductor will not guarantee the RHA performance of any product unless National Semiconductor has tested and certified the specific manufacturing lot.

Interface test reports are available on National Semiconductor's web site at www.national.com/mil.

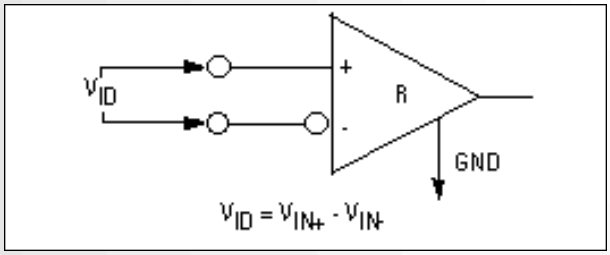
Glossary of Interface-Specific Terms

ANSI/TIA/EIA-644 (LVDS): Approved in 1995, this standard specifies a maximum data rate of 655Mpbs and a theoretical maximum of 1.923Gbps based on a lossless medium.

Common Mode Voltage (V_{CM}): The common mode voltage is defined as the algebraic mean of the two voltages. Measured with respect to circuit ground.



Differential Input Voltage (V_{ID}): The potential difference between two input voltages, usually with respect to the non-inverting input. Commonly used to define the maximum differential input voltage on Differential Receivers.



Differential Data Transmission: Uses two signal lines for data transmission between components. Supported by EIA/TIA-422-A (RS-422) and EIA/TIA-485 (RS-485).

EIA/TIA-232-E (RS-232): Introduced in 1962 for single-ended data transmission at relatively slow data rates (20 kbps) over short distances (typically up to ~50 feet).

EIA/TIA-422-A (RS-422): Standard which allows data rates up to 10 Mbps (up to 40 feet) and lengths up to 4,000 feet (up to 100 kbps).

EIA/TIA-423-A (RS-423): Standard for single-ended applications with a maximum data rate of 100 kbps (up to 30 feet) and a maximum distance of 4,000 feet (up to 1 kbps). EIA-TIA-423-A also requires high impedance driver outputs with power off to not load the transmission line.

EIA/TIA-485 (RS-485): Established in 1983 to meet the need for truly multipoint communications. Meets all of the requirements of EIA/TIA-422-A; but in addition, this standard allows up to 32 drivers and 32 receivers to be connected to a single bus thus allowing a truly multipoint bus to be constructed.

High-Level Input Current (I_{IH}): The current into* an input when a high-level voltage is applied to that input.

High-Level Input Voltage (V_{IH}): An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. *Note: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.*

High-Level Output Current (I_{OH}): The current into* an output with input conditions applied that, according to the product specification, will establish a logic high level at the output.

High-Level Output Voltage (V_{OH}): The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a logic high level at the output.

Hysteresis (V_{HYS}): The absolute difference in voltage value between the positive-going threshold and the negative-going threshold.

Input Clamp Voltage (V_{IK}): An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Input Current at Maximum Input Voltage (I_I): The current into* an input when maximum specified input voltage is applied.

Low-Level Input Current (I_{IL}): The current into* an input when a low-level voltage is applied to that input.

Low-Level Input Voltage (V_{IL}): An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. *(Note: A maximum is specified that is the most positive value of the low-level input voltage for which operation of the logic element within specification limits is guaranteed.)*

* Current out of a terminal is given as a negative value.

Low-Level Output Current (I_{OL}): The current into* an output with input conditions applied that, according to the product specification, will establish a logic low level at the output.

Low-Level Output Voltage (V_{OL}): The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a logic high level at the output.

Negative-Going Threshold Voltage (V_{TL}): The voltage level at a transition-operated input that causes operation of the logic element according to specification, as the input voltage falls from a level above the positive-going threshold voltage, V_{TH}.

Off-State Output Current (I_O, I_{CEX}): The current flowing into* an output with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state. *Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits at a specified voltage usually greater than the V_{CC} supply.*

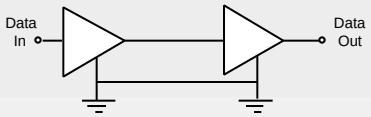
Output Current of a TRI-STATE Device (I_{OZ}): The current into* a TRI-STATE output having input conditions applied that, according to the product specification, will establish the high-impedance state at the output.

Positive-Going Threshold Voltage (V_{TH}): The voltage level at a transition-operated input that causes operation of the logic element according to specification, as the input voltage rises from a level below the negative-going threshold voltage, V_{TL}.

Single-Ended Data Transmission: Uses one signal line for data transmission between components. Supported by EIA/TIA-232-E (RS-232) and EIA/TIA-423-A (RS-423).

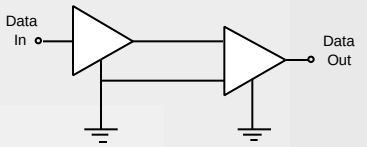
TIA/EIA Specifications

TIA/EIA-232-E Application



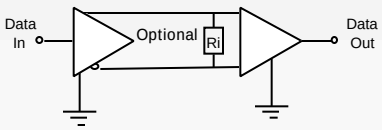
TIA-EIA-232-E was developed for single-ended transmission at relatively slow data rates (20kb/s) over short distances (typically up to 50ft).

TIA/EIA-423-A Application



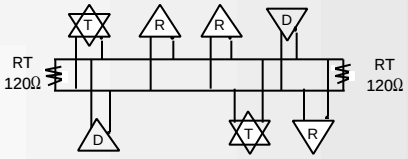
TIA/EIA-423-A extends the data rate of TIA/EIA-232 to 100kb/s (up to 30ft) and the maximum distance to 4000ft (up to 1kb/s). TIA/EIA also requires high impedance driver outputs with power off to not load the transmission line.

TIA/EIA-422-A Application

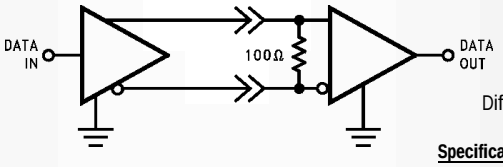


TIA/EIA-422-A is a differential data transmission standard that allows data rates up to 10Mbps (up to 40ft) and line lengths up to 4000ft (up to 100Kbps).

TIA/EIA-485 Application



TIA/EIA-485-A meets all the requirements of TIA/EIA-422 and allows up to 32 drivers and 32 receivers to be connected to a single bus to form a true multipoint bus. TIA/EIA-485 also features an extended common-mode range (-7v to +12v) for both drivers and receivers in TRI-STATE and with power off, and drivers can withstand contention and bus faults.



To meet the need for a very high speed interface, the TIA/EIA committee TR30.2 established TIA/EIA-644 in 1995. This electrical standard generically known as LVDS (Low Voltage Differential Signaling) provides all of the benefits of differential data transmission and is capable of operating at data rates up to 655Mb/s.

Differential Data Transmission Standards

Specification	TIA/EIA-644
Number of Drivers & Receivers Allowed on One Line	1 Driver, 1 Receiver
Maximum Data Rate	655Mb/s
Driver Output Maximum Voltage	±450mV
Driver Output Signal Level	
Loaded	±250mV
Unloaded	±450mV
Driver Load Impedance	100Ω
Receiver Input Voltage Range	GND to +2.4V
Receiver Input Sensitivity	±100mV
Receiver Input Resistance	High Z

Short-Circuit Output Current (I_{OS}): The current into* an output when that output is short-circuited to ground or any other specified potential, with input conditions applied to establish the output logic level farthest from ground potential or any other specified potential.

Supply Current (I_{CC}): The current into* the V_{CC} supply terminal of an integrated circuit.

* Current out of a terminal is given as a negative value.

Radiation Results – Interface Summary

National Semiconductor has performed total dose testing on several of the technologies used to manufacture its Interface products. National's new LVDS-based (ANSI/TIA/EIA-644) DS90C031 and DS90C032 exhibit total dose radiation tolerance up to 50 krad(Si) to an assigned PIPL. The LS technology used to manufacture the DS26LS31 and DS26LS32 has a total dose range of 100 - 350 krad(Si) level. The neutron radiation level is 10^{12} n/cm^2. No single event effect or dose rate testing has been performed on these products.

Total Dose Radiation Test Results: LVDS-Based Products

Today's leading-edge Mil/Aero systems [where data transmission rates exceed 155Mbits/s (77.5MHz)] demand higher reliability, faster speeds, reduced power consumption, and lower costs. Beyond these criteria, transmission systems used in space or for military systems must meet certain radiation resistance levels, based upon their application. While the progress of processing power and memory/storage have kept pace, data transmission has not. Traditional signaling technologies like TTL/CMOS, RS-422/423, RS-485, and PECL cannot move the data fast enough while maintaining low power, low noise, and low cost.

National is addressing these requirements with an industry-leading data transmission family based on the Low-Voltage Differential Signaling (LVDS) standard (ANSI/TIA/EIA-644). This technology uses National's advanced CMOS process, CS-80 (feature size of 0.8µm). LVDS-based devices are targeted at applications where data needs to move short distances between systems or subsystems at rates as high as 655Mbps, such as telecommunication/data communication routers; add/drop multiplexers and switches for box-to-box and rack-to-rack data transmission; and peripherals that need to transmit data between PC boards and/or system components, such as video, 3D graphics, interactive applications.

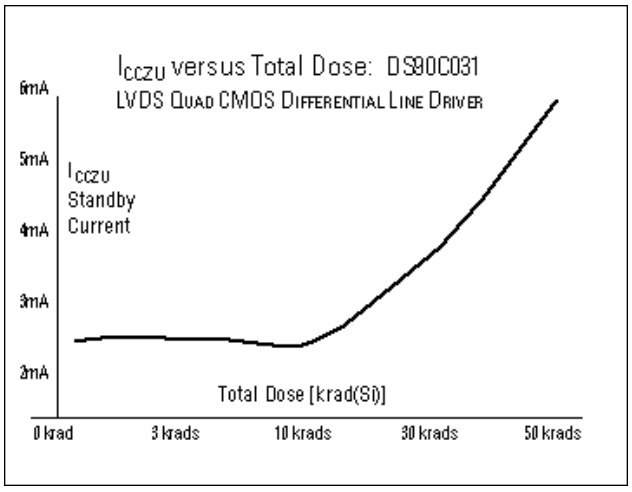
The emphasis with LVDS is to maximize data rates over short distances via printed circuit board traces or cables. With proper termination, an LVDS driver can drive a common twisted pair wire over 5 meters at speeds exceeding of 455Mbps. Because LVDS drivers and receivers do not depend on a specific power supply (such as 5V), the interface offers an easy migration path to lower supply voltages such as 3.3V or even 2.5V, while still maintaining the same signaling levels and performance. LVDS also supports low-power operation. The power dissipated by the load (the termination resistor on the LVDS line) is a mere 1.2mW. In comparison, an RS-422 load typically consumes 90mW – 75 times more than LVDS. The LVDS standard serves applications that require much higher data throughput than the other EIA/TIA interfaces.

DS90C031

The DS90C031 LVDS Quad CMOS Differential Line Driver features low power dissipation and high data rates that can operate in excess of 77MHz. It accepts TTL/CMOS input signals and translates these signals into 350mV differential output signals. The TRI-STATE® function allows the disabling of the output signal stage and placing the unit into a low power idle state.

The total dose testing plan required the devices to be biased under these conditions:

- Two static input biases were used with V_{CC} = 5.5Vdc; inputs were biased all HIGH and all LOW. The outputs were open-circuited and in the TRI-STATE mode for both input bias conditions.
- The high dose rate of the Cobalt-60 irradiator was 69.5 rad(Si)/s.
- All parts had burn-in screen performed.



- After the last final dose level, all irradiated parts were placed on 168-hour, +25˚C post-irradiation anneal. This anneal simulates the low dose rate of the space environment.

Preliminary total dose results indicate that three electrical parameters would require post-irradiation limits (PIPL) at a total dose level of 50 krad(Si). The following electrical parameters were assigned PIPL limits at 50 krad(Si):

- I_{CCZ} = 13mA (10mA at pre-radiation)
- I_{OZ} = +25µA (+10µA at pre-radiation)
- V_{OD} = ±45mV (±35mV at pre-radiation)

All other electrical parameters (DC and AC) remained within their pre-radiation limits. All DS90C031 devices passed their pre-rad or PIPL limits after the one-week, +25˚C, biased anneal. No functional failures occurred from the pre-radiation level to the 50 krad(Si) total dose level.

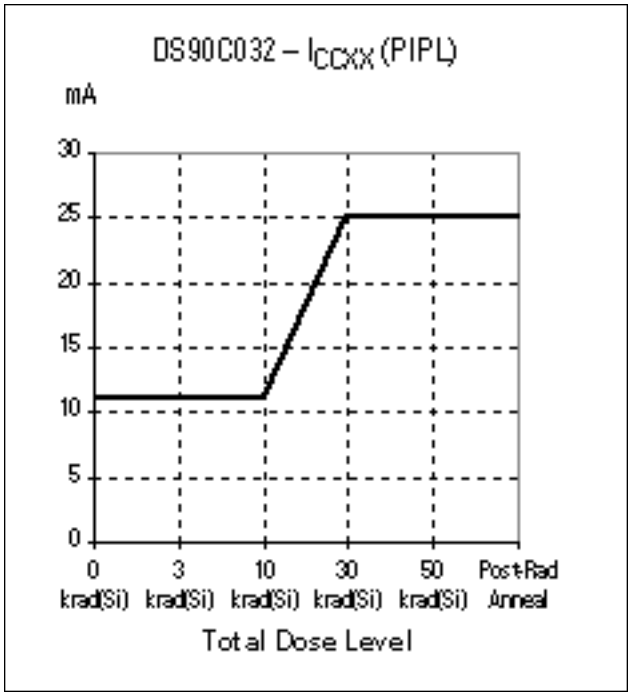
Before these parts can be RHA qualified, rebound and other additional testing must be performed. Plans are in place to test other LVDS-based products

DS90C032

For high speed, point-to-point interface applications, National's DS90C032 LVDS Quad CMOS Differential Line Receiver reduces board space consumption while providing an alternative to high power, pseudo-ECL devices. Small swing differential signal levels (350mV) support data rates in excess of 155Mbps (77.7MHz). The small differential input signals are translated to CMOS/TTL output levels. A TRI-STATE function allows output signals to be multiplexed.

In Total Ionizing Dose testing (MIL-STD-883E, Method 1019.5 plus +25˚C, 168-hour post-radiation anneal step), results indicate the only radiation-sensitive parameter is I_{CCXX} (Standby Leakage Current). All other DC and AC parameters remain within their pre-radiation limits.

National's DS90C032 LVDS Differential Line Receiver and its companion DS90C031 Differential Line Driver are RHA evaluated to 50 krad(Si) (RHA L level) using Post-Irradiation Parametric Limit (PIPL) and no functional failures.



Interface Products Proposed for RHA Qualifications

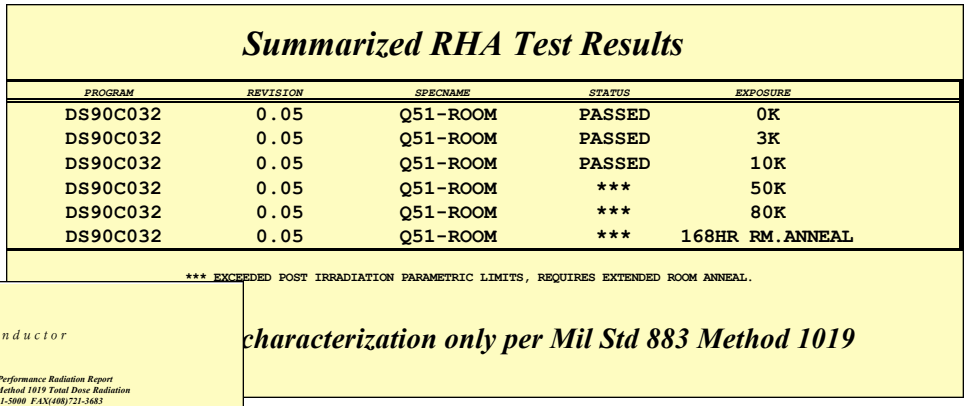
LVDS (Low Voltage Differential Signaling) Products

Product	Parameter	3 krad(Si)	10 krad(Si)	30 krad(Si)	50 krad(Si)	100 krad(Si)	300 krad(Si)	+25°C Anneal	Single Event Effects Heavy Ion Test Results Latchup (SEL [MeV/(mg/cm^2)])
DS16F95	All Parameters	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Not available	>120
DS26C31	All Parameters	Meets Pre-Rad	Meets Pre-Rad	–	–	–	–	Not available	>38 (Californium 252)
DS26C32	All Parameters	Meets Pre-Rad	Meets Pre-Rad	–	–	–	–	Not available	>38 (Californium 252)
DS26F31	All Parameters	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	–	Not available	Not available
DS26F32	All Parameters	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Not available	Not available
DS26LS31	All Parameters	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Not available	Not available
DS26LS32	All Parameters	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Meets Pre-Rad	Not available	Not available
DS90C031	I_{CCZ}	10mA	10mA	13mA	13mA		Not available	Not available	
	D_{V0S}	± 25mV	± 25mV	± 35mV	± 35mV		Not available	Not available	
	D_{V0D}	± 35mV	± 35mV	± 45mV	± 45mV		Not available	Not available	
	I_{OZL}	10µA	10µA	25µA	25µA		Not available	Not available	
	I_{OZH}	10µA	10µA	25µA	25µA		Not available	Not available	
DS90C032	I_{CCHQ1}	11mA	11mA	25mA	25mA			25mA	
	I_{CCHQ2}	11mA	11mA	25mA	25mA			25mA	
	I_{CCHQ3}	11mA	11mA	25mA	25mA			25mA	
	I_{CCLQ2}	11mA	11mA	25mA	25mA			25mA	
	I_{CCLQ3}	11mA	11mA	25mA	25mA			25mA	
	I_{CCZQ1}	11mA	11mA	25mA	25mA			25mA	
	I_{CCZQ2}	11mA	11mA	25mA	25mA			25mA	
	I_{CCZQ3}	11mA	11mA	25mA	25mA			25mA	
	I_{CCZQ4}	11mA	11mA	25mA	25mA			25mA	
	I_{CCZQ5}	11mA	11mA	25mA	25mA			25mA	

Interface Final Reports

Cover Page Example

Includes:
- Product information
- Traceability
- Comprehensive test results
- Lot pass/fail status

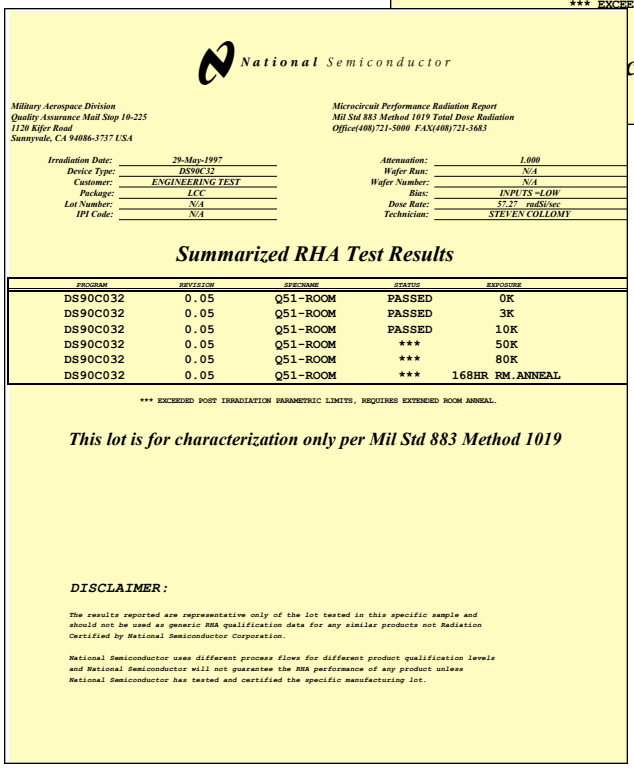


Summarized RHA Test Results

PROGRAM	REVISION	SPECNAME	STATUS	EXPOSURE
DS90C032	0.05	Q51-ROOM	PASSED	0K
DS90C032	0.05	Q51-ROOM	PASSED	3K
DS90C032	0.05	Q51-ROOM	PASSED	10K
DS90C032	0.05	Q51-ROOM	***	50K
DS90C032	0.05	Q51-ROOM	***	80K
DS90C032	0.05	Q51-ROOM	***	168HR RM.ANNEAL

*** EXCEEDED POST IRRADIATION PARAMETRIC LIMITS, REQUIRES EXTENDED ROOM ANNEAL.

characterization only per Mil Std 883 Method 1019



National Semiconductor

Military Aerospace Division
Quality Assurance Mail Stop 10-225
1120 Kifer Road
Sunnyvale, CA 94086-3737 USA

Microcircuit Performance Radiation Report
Mil Std 883 Method 1019 Total Dose Radiation
Office(408)721-5000 FAX(408)721-3683

Irradiation Date:	29-May-1997	Attenuation:	1.000
Device Type:	DS90C32	Wafer Run:	N/A
Customer:	ENGINEERING TEST	Wafer Number:	N/A
Package:	LCC	Bias:	INPUTS =LOW
Lot Number:	N/A	Dose Rate:	57.27 radSi/sec
IPI Code:	N/A	Technician:	STEVEN COLLOMY

Summarized RHA Test Results

PROGRAM	REVISION	SPECNAME	STATUS	EXPOSURE
DS90C032	0.05	Q51-ROOM	PASSED	0K
DS90C032	0.05	Q51-ROOM	PASSED	3K
DS90C032	0.05	Q51-ROOM	PASSED	10K
DS90C032	0.05	Q51-ROOM	***	50K
DS90C032	0.05	Q51-ROOM	***	80K
DS90C032	0.05	Q51-ROOM	***	168HR RM.ANNEAL

*** EXCEEDED POST IRRADIATION PARAMETRIC LIMITS, REQUIRES EXTENDED ROOM ANNEAL.

This lot is for characterization only per Mil Std 883 Method 1019

DISCLAIMER:

The results reported are representative only of the lot tested in this specific sample and should not be used as generic RHA qualification data for any similar products not Radiation Certified by National Semiconductor Corporation.

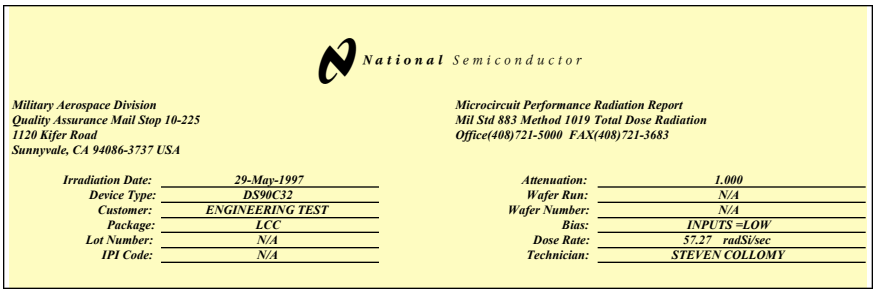
National Semiconductor uses different process flows for different product qualification levels and National Semiconductor will not guarantee the RHA performance of any product unless National Semiconductor has tested and certified the specific manufacturing lot.

Test Report Example

Includes:
- Test names from National Semiconductor datasheet or Customer Drawing
- Product information
- Statistical summary
- Test pass/fail status
- Graphic summary

Report Header Example

Includes:
- Corporate header and contact information
- Comprehensive product information
- Traceability



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Customer:	ENGINEERING TEST	Wafer Number:	N/A
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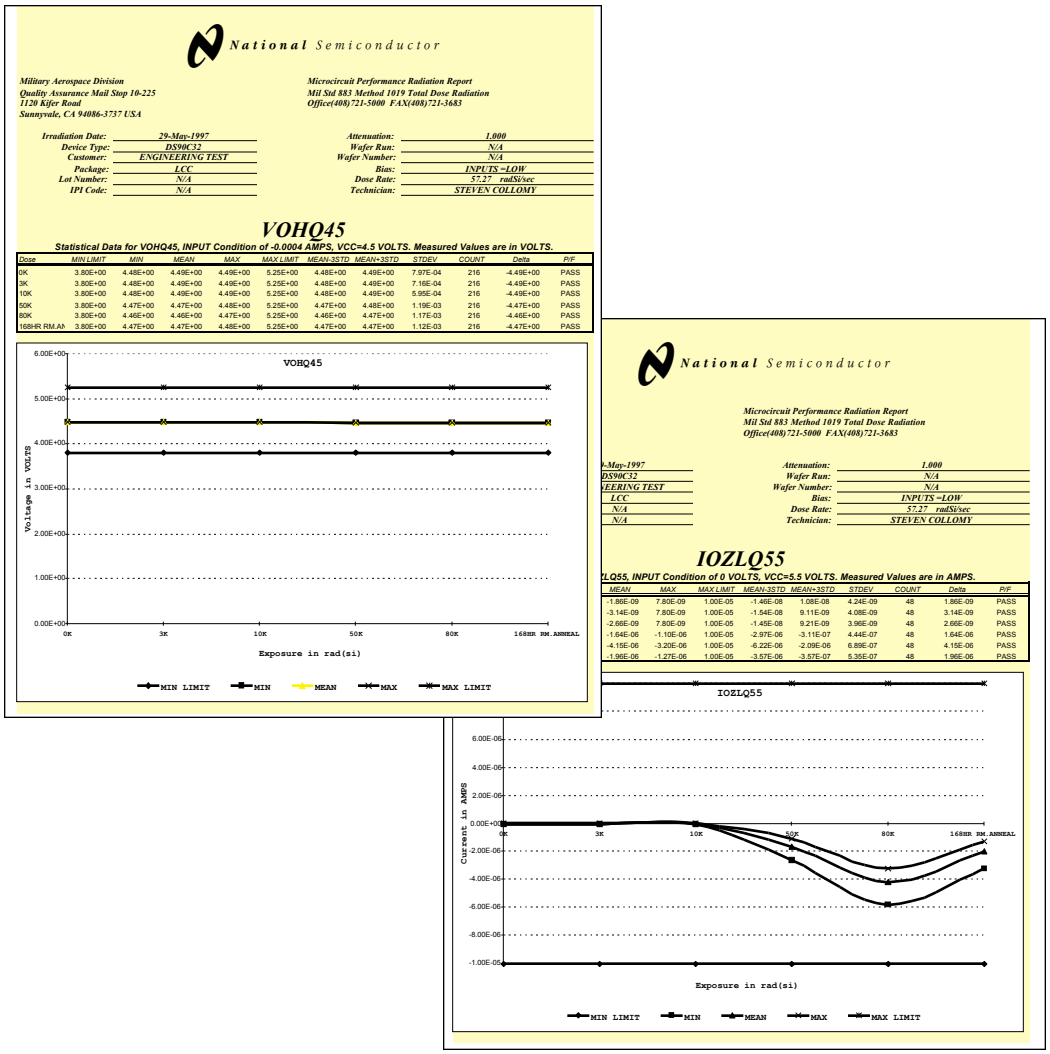
Lot Number:	N/A	Dose Rate:	57.27 radSi/sec
IPI Code:	N/A	Technician:	STEVEN COLLOMY

Interface test reports are available on National Semiconductor's web site at www.national.com/mil.

Report Graph & Statistics Examples

Includes:

- Test names from National Semiconductor's datasheet or Customer Drawing
- Summarized test results by exposure level
- Test limits from test program
- Statistical values



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Irradiation Date:	29-May-1997	Attenuation:	1.000
Device Type:	DS90C32	Wafer Run:	N/A
Customer:	ENGINEERING TEST	Wafer Number:	N/A
Package:	LCC	Bias:	INPUTS =LOW
Lot Number:	N/A	Dose Rate:	57.27 rad(Si)/sec
IPI Code:	N/A	Technician:	STEVEN COLLOMY

VOHQ45

Statistical Data for VOHQ45, INPUT Condition of -0.0004 AMPS, VCC=4.5 VOLTS. Measured Values are in VOLTS.

Dose	MIN LIMIT	MIN	MEAN	MAX	MAX LIMIT	MEAN-3STD	MEAN+3STD	STDEV	COUNT	Delta	P/F
0K	3.80E+00	4.48E+00	4.49E+00	4.49E+00	5.25E+00	4.48E+00	4.49E+00	7.97E-04	216	-4.49E+00	PASS
3K	3.80E+00	4.48E+00	4.49E+00	4.49E+00	5.25E+00	4.48E+00	4.49E+00	7.16E-04	216	-4.49E+00	PASS
10K	3.80E+00	4.48E+00	4.49E+00	4.49E+00	5.25E+00	4.48E+00	4.49E+00	5.95E-04	216	-4.49E+00	PASS
50K	3.80E+00	4.47E+00	4.47E+00	4.48E+00	5.25E+00	4.47E+00	4.48E+00	1.19E-03	216	-4.47E+00	PASS
80K	3.80E+00	4.46E+00	4.46E+00	4.47E+00	5.25E+00	4.46E+00	4.47E+00	1.17E-03	216	-4.46E+00	PASS
168HR RM.An	3.80E+00	4.47E+00	4.47E+00	4.48E+00	5.25E+00	4.47E+00	4.47E+00	1.12E-03	216	-4.47E+00	PASS

National Semiconductor

Microcircuit Performance Radiation Report
Mil Std 883 Method 1019 Total Dose Radiation
Office(408)721-5000 FAX(408)721-3683

-May-1997		Attenuation:	1.000
DS90C32		Wafer Run:	N/A
EERING TEST		Wafer Number:	N/A
LCC		Bias:	INPUTS =LOW
N/A		Dose Rate:	57.27 rad(Si)/sec
N/A		Technician:	STEVEN COLLOMY

IOZLQ55

LQ55, INPUT Condition of 0 VOLTS, VCC=5.5 VOLTS. Measured Values are in AMPS.

MEAN	MAX	MAX LIMIT	MEAN-3STD	MEAN+3STD	STDEV	COUNT	Delta	P/F
-1.86E-09	7.80E-09	1.00E-05	-1.46E-08	1.08E-08	4.24E-09	48	1.86E-09	PASS
-3.14E-09	7.80E-09	1.00E-05	-1.54E-08	9.11E-09	4.08E-09	48	3.14E-09	PASS
-2.66E-09	7.80E-09	1.00E-05	-1.45E-08	9.21E-09	3.96E-09	48	2.66E-09	PASS
-1.64E-06	-1.10E-06	1.00E-05	-2.97E-06	-3.11E-07	4.44E-07	48	1.64E-06	PASS
-4.15E-06	-3.20E-06	1.00E-05	-6.22E-06	-2.09E-06	6.89E-07	48	4.15E-06	PASS
-1.96E-06	-1.27E-06	1.00E-05	-3.57E-06	-3.57E-07	5.35E-07	48	1.96E-06	PASS

Example of Raw Data – Excel (.xls) File

DOSE	SN#	TEST#	NAME	IN	OUT	MIN LIMIT	MAX LIMIT	MEASURE
0K	1	1	ICCH	0	16	-5.00E-08	9.00E-08	0.00E+00
0K	2	1	ICCH	0	16	-5.00E-08	9.00E-08	-1.59E-08
0K	3	1	ICCH	0	16	-5.00E-08	9.00E-08	-1.59E-08
0K	4	1	ICCH	0	16	-5.00E-08	9.00E-08	-1.59E-08
0K	5	1	ICCH	0	16	-5.00E-08	9.00E-08	-1.59E-08
0K	6	1	ICCH	0	16	-5.00E-08	9.00E-08	-1.59E-08
3K	1	1	ICCH	0	16	-1.00E-06	1.50E-05	-1.59E-08
3K	2	1	ICCH	0	16	-1.00E-06	1.50E-05	-1.59E-08
3K	3	1	ICCH	0	16	-1.00E-06	1.50E-05	0.00E+00
3K	4	1	ICCH	0	16	-1.00E-06	1.50E-05	0.00E+00
3K	5	1	ICCH	0	16	-1.00E-06	1.50E-05	0.00E+00
10K	1	1	ICCH	0	16	-1.00E-06	7.50E-05	-1.59E-08
10K	2	1	ICCH	0	16	-1.00E-06	7.50E-05	5.40E-07
10K	3	1	ICCH	0	16	-1.00E-06	7.50E-05	2.31E-06
10K	4	1	ICCH	0	16	-1.00E-06	7.50E-05	1.84E-05
10K	5	1	ICCH	0	16	-1.00E-06	7.50E-05	6.95E-06
30K	1	1	ICCH	0	16	-2.00E-05	7.00E-04	-1.59E-08
30K	2	1	ICCH	0	16	-2.00E-05	7.00E-04	2.60E-04
30K	3	1	ICCH	0	16	-2.00E-05	7.00E-04	2.44E-04
30K	4	1	ICCH	0	16	-2.00E-05	7.00E-04	2.87E-03
30K	5	1	ICCH	0	16	-2.00E-05	7.00E-04	8.93E-04
50K	1	1	ICCH	0	16	-2.00E-05	7.00E-04	-1.59E-08
50K	2	1	ICCH	0	16	-2.00E-05	7.00E-04	4.19E-04
50K	3	1	ICCH	0	16	-2.00E-05	7.00E-04	3.36E-04
50K	4	1	ICCH	0	16	-2.00E-05	7.00E-04	6.77E-03

Interface test reports are available on National Semiconductor's web site at www.national.com/mil.

Notes