IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 42 NO. 6, DECEMBER 1995 1823

Ion Induced Charge Collection and SEU Sensitivity of Emitter Coupled Logic (ECL) Devices

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Abstract

This paper presents single event upset (SEU) and latchup test results for selected Emitter Coupled Logic (ECL) microcircuits, including several types of low capacity SRAMs and other memory devices. The high speed of ECL memory devices makes them attractive for use in space applications. However, the emitter coupled transistor design increases susceptibility to radiation induced functional errors, especially SEU, because the transistors are not saturated, unlike the transistors in a CMOS device. Charge collection at the sensitive nodes in ECL memory elements differs accordingly. These differences are responsible, in part, for the heightened SEU vulnerability of ECL memory devices relative to their CMOS counterparts.

Introduction

Emitter Coupled Logic (ECL) devices have been used in numerous electronic systems in the past twenty or more years [1-3]. Because the gate delay (on the order of 1 ns) is significantly shorter for ECL devices than for devices from the CMOS or TTL logic families, ECL microcircuits are often utilized in the so-called "front end" of electronic systems, where input signals need to be processed rapidly. ECL memory devices are also used in computer cache memory systems, again because of their high speed.

The high speed of ECL microcircuits makes them attractive to space system engineers. However, before their continued use in critical space applications can be fully endorsed, a more thorough characterization is needed of the susceptibility of these devices to single event effects, such as single event upset (SEU) and single event latchup (SEL).

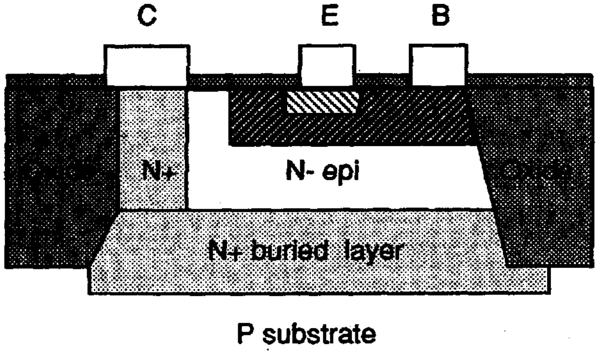

Fig. 1. Schematic of ECL Transistor Structure

Because the coupled transistors in an ECL memory cell remain in a non-saturated state continuously, the charge collection characteristics and SEU susceptibility of these devices differs from those fabricated in CMOS or TTL technology. For example, in ECL devices prompt charge collection at the sensitive nodes appears to be more important than drift charge collection in causing upset.

In the following, we present SEU and latchup results relevant to the use of ECL devices in space, and discuss the implications of these findings for our current understanding of upset mechanisms in this family of devices.

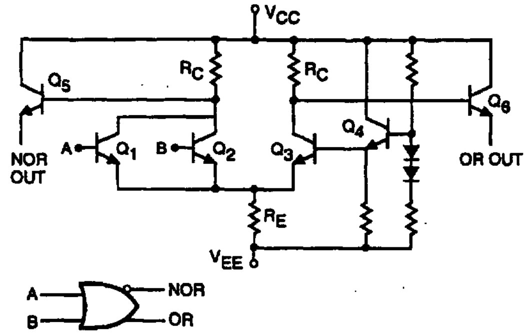

Fig. 2. ECL OR/NOR Gate

ECL Devices

The transistors (see Fig. 1) in an ECL gate are not fully saturated, unlike the transistors in devices from other logic families, such as TTL and CMOS. The output of an ECL gate (e.g., see Fig. 2) exhibits minimum high levels and maximum low levels of about -1V and -1.6V, respectively. The typical relationship between the input and output logic levels is shown in Fig. 3. About 1 ns (or less) is required for transition from one logical state to another. Thus, an overall operational speed of several gigahertz can be achieved by logic systems that utilize devices fabricated in mature ECL technology.

High speed memory elements can be developed using combinations of ECL "AND" and "OR" gates. For example, Fig. 4 shows a master-slave flip-flop constructed from six ECL gates. ECL technology has also been used to fabricate fast SRAMs. Each SRAM cell consists of two matching active transistors, as shown in Fig. 5. Unlike the collectors of the Q2 and Q3 transistors in the circuit for a logic gate (see Fig. 2), the collectors in ECL SRAM cells are tied to the bases of the opposite transistors (Fig. 5), forming bistable

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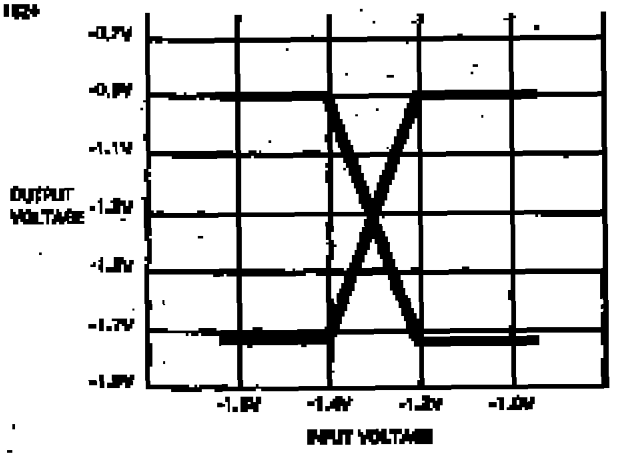

Fig. 3. Typical ECL Transfer Characteristics

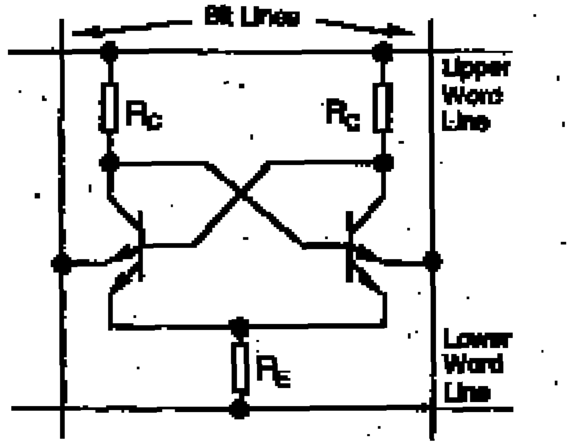

Fig. 5. Transistors in Memory Element of ECL SRAM

logic elements. Because neither transistor is saturated, a stable state consists of one transistor (the "on" transistor) carrying a much larger current than the other (although both are forward biased). The logic polarity is changed if the other transistor carries a higher current. The complementary processes of reading from and writing to the cell are both accomplished through the bit lines. Consequently, the bit lines are connected to the sense amplifier while the cell is being read, and to a set of drivers while the cells is being written.

The resistors in the memory cell are placed adjacent to the transistors in order to reduce the geometry and the capacitance between various layers, such as the boundary between the collector and the base [4]. In these so-called "isoplanar" devices, it is possible to achieve a subnanosecond transition of the memory state.

Because the majority of the transistors in ECL microcircuits are forward biased, and therefore transitions from logic "high" to "low" and vice versa take place very fast, power consumption (hence, heat generation) tends to be greater for ECL microcircuits than for those fabricated in other technologies, such as TTL or CMOS. The capacity of ECL SRAMs (up to tens of thousands of address locations) therefore tends to be smaller than that of SRAMs from other logic families.

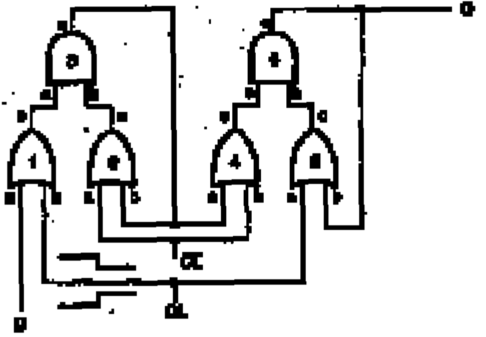

Fig. 4. Functional Logic of Master-Slave D Flip-Flop

Table 1 shows the ECL devices selected for irradiation with heavy ions and protons (as described in the following section). The 100331 flip-flops and the 100341 shift register belong to National Semiconductor's F100K300 technology family, and have a feature size of about 2.5 µm. The thickness of the epi layer is on the order of 1 micron (see Fig. 1). The Motorola line driver belongs to the ECL 10K technology family and has a somewhat larger feature size. Because this device type does not have memory elements, it was tested for latchup only. The Cypress Semiconductor, Fujitsu, and NEC SRAMs share the same 1K x 4 memory configuration, making comparisons of SEU susceptibility somewhat simpler.

Table 1. Selected ECL Test Devices

Device Type	Mfr.	Function	Date Code
100331	NSC	Master-Slave D FF	9220
100341	NSC	Shift Register	9220
MC10H115	MOT	Line Receiver	8930
CY100E474	CYP	SRAM (1K x 4)	9010
MBM10474A	FUJ	SRAM (1K x 4)	8802
µPB10474	NEC	SRAM (1K x 4)	8721

Single Event Effects Testing and Observations

The test techniques utilized in the present study of ECL devices are similar to those typically used to test microcircuits fabricated in other technologies, with two exceptions. First, because ECL devices consume a rather large current and therefore the device temperature rises sharply, especially in a vacuum environment, the temperature of the test devices needs to be controlled; both thermoelectric and water cooled apparatuses were used for this purpose. Second, ECL logic levels (-1.0 volts for "high" and -1.6 volts for "low") need to be translated to either CMOS or TTL levels in order to use

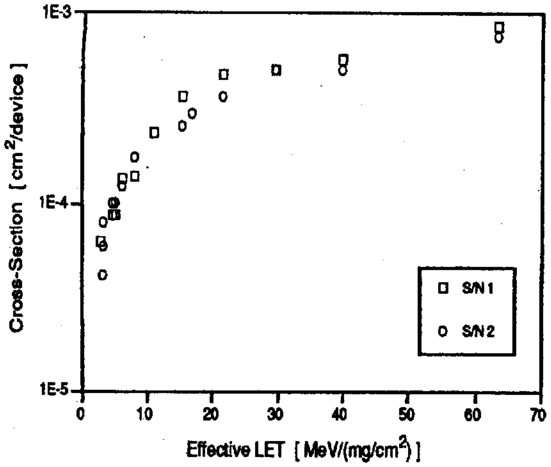

Fig. 6. SEU Test Results for NSC 100331 D Flip-Flop

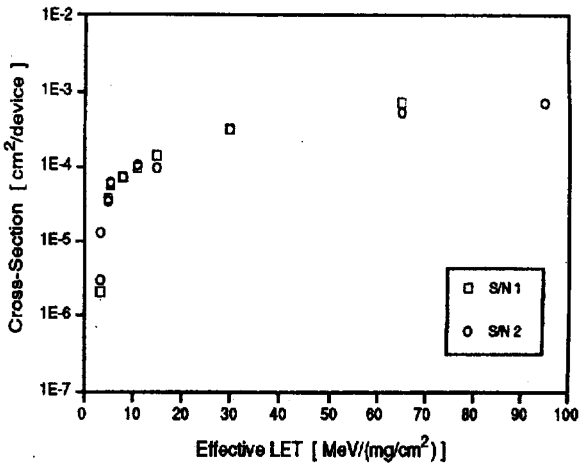

Fig. 7. SEU Test Results for NSC 100341 Shift Register

standard laboratory equipment. SEU testing of ECL devices has seldom been performed in the past, mainly because of these two difficulties [5].

The test devices for the present study (see Table 1) were irradiated at the Lawrence Berkeley Laboratory 88-inch cyclotron facility using the following ion beams: xenon (603 MeV), krypton (380 MeV), copper (290 MeV), argon (180 MeV), neon (90 MeV), nitrogen (67 MeV), and protons (35 and 55 MeV). The corresponding linear energy transfer (LET) values for the non-hydrogen beams were: 63, 41, 30, 15, 5.6, and 3 MeV/(mg/cm^2).

A brief description of the testing procedure follows (detailed information on beam delivery and data collection techniques can be found in [6,7]). While running the test, the single event upset rate was kept between 1 and 3 events per second. This made the dead time caused by resetting the device under test (DUT) negligible compared to the total test time. After a sufficient number of errors had been recorded, the test was stopped and the total fluence of particles and total number of errors were recorded. The device error probability or cross-section, σ, was then calculated from the expression:

$$\sigma = \frac{N \sec(\theta)}{F},$$

where N and F are the number of errors and beam fluence, respectively, and θ is the incident angle of the beam, measured with respect to the chip-surface normal. (The cross-section provides an index of gross susceptibility to SEU.) During the SEU tests, the DUT power supply current was closely monitored to detect any occurrence of latchup.

When the incident ion is very energetic and the sensitive region is a very thin, flat volume (resembling a pancake), the charge deposited varies with sec(θ) for a wide range of incident angles. In this case, the effective LET is [L sec(θ)], where L is the LET of the incident ion. However, for many microcircuits, and ECL devices in particular, the geometry of the sensitive region cannot be assumed to be flat. Therefore, only small incident angles were utilized in the present study.

SEU test results for the National Semiconductor 100331 and 100341 flip-flop devices are shown in Figs. 6 and 7, respectively. The 100331 contains three flip-flops in a single package, whereas the 100341 consists of eight flip-flops, organized as an 8-bit shift register. The SEU cross-sections shown in Figs. 6 and 7 are aggregate measures of the SEU susceptibility of all the flip-flops in a single package (either three or eight, respectively).

As illustrated in Figs. 6 and 7, the cross-section curves for 100331 and 100341 differ in overall shape, although the saturation values are similar (just under 10^{-3}). For 100331 the cross-section values increase gradually with LET, whereas for 100341 a sharp "knee" is observed at about 4 MeV/(mg/cm^2). The gradual slope of the curves for 100331 suggests that the memory elements in this device have different critical charges for SEU; in contrast, the charge thresholds for the memory elements in 100341 appear to be nearly uniform. This disparity may be due to the use of master-slave flip-flops in 100331 but not in 100341 (in a master-slave flip-flop, the master and slave can have different critical charges [8]).

Figures 8 through 10 show the heavy ion SEU test results for the NEC μPB10474, Fujitsu MBM10474A, and Cypress Semiconductor CY100E474 1K x 4 SRAMs, respectively. MBM10474A was also tested for proton induced SEU using 35 and 55 MeV protons, as shown in Fig. 11.

The cross-section curves for both μPB10474 (Fig. 8) and MBM10474A (Fig. 9) display a relatively sharp "knee" below an effective LET of about 3 MeV/(mg/cm^2), which suggests that the critical charge for SEU is similar for most memory elements in these devices. In contrast, for CY100E474 (Fig. 10) the cross-section gradually increases, suggesting non-uniformity in the charge thresholds of the memory elements. (This could be due to the memory elements having different sizes or geometries; however, this possibility was not investigated here.)

The LET thresholds of the μPB10474 and MBM10474A SRAMs, but not the CY100E474, are lower than those of typical commercial CMOS and NMOS RAMs (e.g., see [9,10]). Overall, the saturation cross-sections for ECL SRAMs appear to be comparable to those of many CMOS SRAMs, although σ_{sat} is highly variable in both technologies.

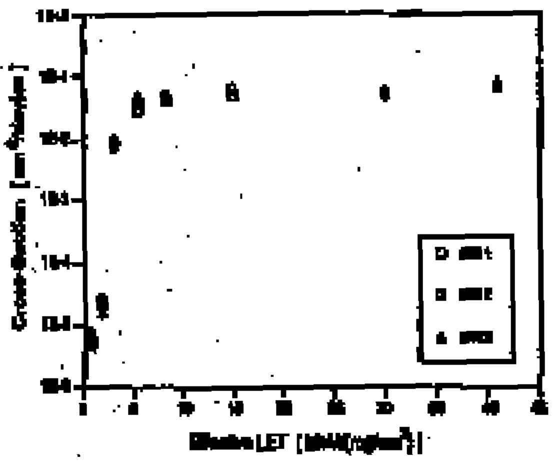

Fig. 8. SEU Test Results for NEC µPB10474 SRAM

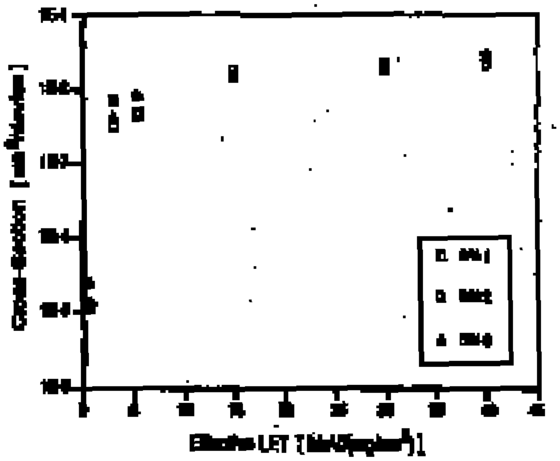

Fig. 9. SEU Test Results for Fujitsu MBM10474A SRAM

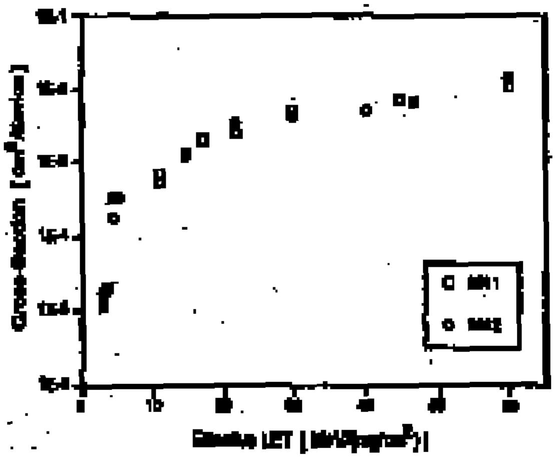

Fig. 10. SEU Test Results for Cypress CY100E474 SRAM

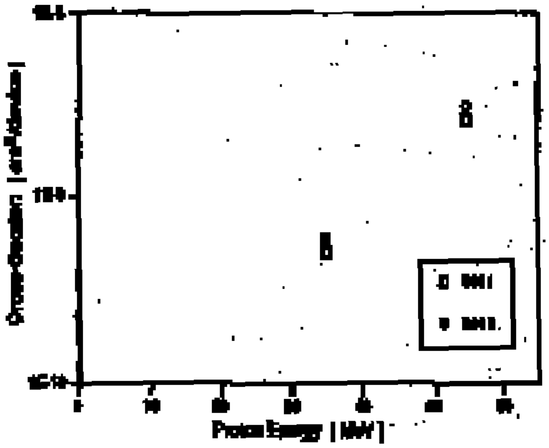

Fig. 11. Proton SEU Test Results for MBM10474A SRAM

The nature of the upsets was examined in detail, and is summarized here for MBM10474A. The polarity of the bit upsets appeared to be essentially unbiased: 47% 0 → 1 errors and 53% 1 → 0 errors, as shown in Table 2 (data obtained with Kr ions). The absence of a polarity effect indicates that the transistors in the memory elements (see Fig. 5) have very similar geometric sizes [11].

Single ion induced multiple-bit upsets have been reported for SRAMs fabricated in other technologies [9,12,13]. In the present investigation (again taking MBM10474A as an example), the frequency and distribution of multiple-bit upsets were analyzed by irradiating the test devices with Kr, Cu, Ar, Ne, and N ions normal to the chip surface, and recording the number of memory cells upset by each ion strike. The percentage of multiple versus single bit upsets is shown in Table 3. Notice that no more than two bits were upset by any

Table 2. Upset Bit Polarity for MBM10474A

		Upsets		
Run #	S/N	0 → 1	1 → 0	Total
1	1	55	45	100
2	1	45	55	100
3	2	56	44	100
4	2	40	61	101
5	3	50	51	101
6	3	42	60	102
		47%	53%	607

ion, and those upset bits appeared to be physically adjacent. Furthermore, for multiple-bit upsets, the two upset bits belonged to different logical words – that is, there were no single-word multiple-bit upsets [13]. No "stuck bits" were observed either (in some CMOS and NMOS SRAMs a sizable number of bits become stuck during ion irradiation in either logical "0" or logical "1" [14]).

Table 3. Multiple-Bit Upsets for MBM10474A

Ion	% of Upsets Caused by Single Ion Hit		
	1 bit	2 bits	> 2 bits
Kr	80	20	0
Cu	78	22	0
Ar	80	20	0
Ne	98	2	0
N	100	0	0

The Motorola MC10H115 line receiver was tested for latchup only. Neither this device nor any of the aforementioned devices latched-up during testing. The calculated upper limit of the latchup cross-section is thus about 1 x 10^{-7} cm^2.

Discussion: SEU Mechanisms

The mechanisms responsible for SEU in bistable ECL memory elements are described below. The high SEU susceptibility (i.e., low SEU thresholds) of ECL devices in comparison to CMOS and NMOS devices stems, in part, from the large base-to-collector current amplification factor (β) and low capacitance of the transistors; a small voltage swing can easily alter the bistable elements in these devices.

As shown in Fig. 5, each ECL cell is constructed from two similar transistors. The vulnerable nodes are located at the bases of the transistors, as well as at the collector of the "off" transistor. Because the transistors are not in the saturated state while biased at a low voltage (V_{CE} = ~1V), the depletion regions are thin. The large base-to-collector current amplification factor of the transistors (β = ~120) greatly magnifies relatively small charges (~9 fC in the thin sensitive regions) at the collector of the "off" transistor, causing an alteration of the logic state of the other (coupled) transistor. Because ECL circuits have a very small parasitic capacitance by design, there is no significant time delay. The combined change in the states of the transistors alters the logical state of the memory bit, resulting in SEU.

This model is supported by additional experiments in which an MBM10474A memory cell was exposed to a pulsed laser beam. (A description of the use of laser beams in SEU research can be found in [15].) Because the spot size of the laser beam is on the order of one micron, it was possible to expose one section of the cell at a time. Results indicate that the "off" transistor was 5 times more sensitive than its counterpart (sensitivity is measured by the laser power required to induce upset). That is, the memory cell could be upset by exposing the "on" transistor at 5 times the energy required to cause upset at the "off" transistor. This further supports the observation that charge collection at the base of the "on" transistor can lead to memory upset.

Thick SiO_2 surrounds the silicon island that makes up a transistor (see Fig. 1). Within a transistor, the collector occupies the entire lateral area and the base occupies about two-thirds of this area. The sensitive region is therefore a very large portion of the entire area. The large cross-section of ECL devices arises from the fact that the sensitive regions occupy a large fraction of the transistor.

For devices fabricated in CMOS and other technologies diffusion charge collection can affect sensitive regions at a distance from the ion impact site as the column of charge expands to a wider area, thereby resulting in multiple-bit upsets potentially involving several bits at a time. However, as shown in Table 3, only single and double bit errors were observed for the MBM10474A SRAM, which suggests that diffusion charge collection is relatively ineffective at producing SEU in this device type; instead, it appears that prompt charge collection is the primary cause of upset.

The sensitive regions of the 100331 and 100341 flip-flop devices are located at various transistors within the gates (see Fig. 4). Some transistors, such as Q4 in Fig. 2, are more sensitive than others due to their relationships with other transistors in the microcircuit.

Table 4 shows the cross-section per bit for the test devices, obtained by dividing the saturation cross-section by the total number of bits. The geometrical area of a transistor base for the 100341 shift register is approximately 140μ^2. Therefore, the cross-section for a single memory element is about 7 times as large as the sensitive area of a single transistor.

Table 4. Sensitivity of ECL Memory Elements

Device Type	Cross-Section per Bit (μ^2)
CY100E474 SRAM	370
MBM10474 SRAM	730
µPB10474 SRAM	2100
100341 Shift Reg.	1000
100331 D Flip-Flop	2670

The high resistivity p-substrate is located below the buried layer. Regardless of the resistivity, no p-n-p-n parasitic SCR circuits are activated because the p-substrate is tied to the negative supply voltage; this, possibly, is also the reason that all the test devices were immune to latchup.

Conclusion

The present study has demonstrated that ECL devices are very vulnerable to SEU. ECL SRAMs display a lower LET threshold (~3 MeV/(mg/cm^2)) than most comparable CMOS devices. The ECL devices appear to be sensitive to prompt charge collection only, which limits effective charge collection to a small region near the ion impact site; they are therefore less susceptible to multiple-bit upsets than many commercial CMOS RAMs. None of the test devices latched-up.

The above results represent only a preliminary study of ECL devices; additional research is required to more thoroughly characterize the radiation vulnerability of this family of devices. Because these devices have been (and will continue to be) used in space electronics systems, it is essential to determine the probable upset rate of each device, to understand the mechanisms of SEU, and to create effective SEU mitigation strategies (such as redundant logic systems).

Acknowledgments

We would like to thank our Aerospace colleagues V.T. Hunt, B.M. Johnson, M. Lalic, and R.L. Walter for providing technical assistance, and the staff of the LBL 88-inch cyclotron facility for beam delivery.

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