NAVIGATOR
TECHNOLOGY DIRECTION FOR THE MIL/AERO COMMUNITY

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1999

1999 WILL HAVE MANY CHALLENGES

As we enter 1999, the many changes that started in the Military/Aerospace market over the past few years continue unabated. Driven by the need to use the latest technology and the government's initiative to reduce the acquisition cost of equipment, we have seen:

- Increased procurement of commercial-grade components for use in harsh environments
- Re-testing or upscreening of components for applications outside the range for which they were designed and tested by semiconductor manufacturers
- The use of higher integration or system-on-a-chip to boost functionality, increase performance, and reduce cost

National is committed to the military and aerospace market, supplying products that meet customers' needs. We will continue to adapt to customers' changing needs and proactively work with them to meet their objectives. This includes reducing the time to bring new products to market, ensuring that designers have access to the latest technologies. Our goal is to simultaneously introduce new hi-rel products with their commercial-grade counterparts.

National does not recommend that customers upscreen components for use in applications which are outside their intended use *(see editor's note, page 7)*; however, we are happy to work with customers to provide components that are designed and tested by National to meet a specific application and/or environment. The manufacturing costs and selling prices of many of our standard military-grade components have been reduced such that customers can more affordably use the correct component, especially when the additional cost of upscreening is considered.

Supporting the move to higher integration is our Custom Business Unit (CBU). Formed three years ago, it provides an impressive offering of custom designs. From foundry services to full turnkey designs, from prototypes to high volume production, the CBU has full systems-on-a-chip capability.

Add to this that the Mil/Aero Division is also responsible for many of our hermetic commercial-grade products as well as National's die and wafer products and you can see that we provide nearly all of your product needs.

On a personal note, this past year has been one of many changes for me. In May, I rejoined National after having left 16 years ago. I am impressed by the many positive changes which have taken place, and am optimistic about our strategy and future. I also made my own contribution to new products when in November my wife gave birth to twins.

Yes, 1999 will have many challenges!

Tom Freeze
Vice President
Military/Aerospace Division

CONTENTS

Boundary Scan Benefits Realized with Demo

Boundary scan is a tremendous time saver for prototyping boards and systems. It eliminates structural faults which are often difficult and time consuming to debug using functional techniques. It also provides a means to test interconnects for the entire system by enabling efficient failure detection, diagnosis to the pin/net level, and PCB repair.

Now available to help designers implement embedded system-level boundary scan test is National Semiconductor's boundary scan demonstration system and acompanying SCAN EASE software. This demo consists of a multidrop backplane that interconnects a processor card to several system I/O cards. The backplane contains a 16-bit data bus, 16-bit address bus, and several control signals routed to 6 connectors. The processor card consists of a processor core and includes a Motorola 68302 microprocessor, boot EPROM, working SRAM, RS232 port for remote communication, parallel backplane interface, and auxiliary parallel port. The I/O cards have identical architectures and include a 16-bit LCD display, on-board EPROM to store LCD messages, and a backplane interface. I/O cards also contain logic which multiplexes data from either the backplane or EPROM to the display.

A multidrop (i.e., parallel) backplane architecture enables cards to populate the system's backplane I/O card connectors. Board addressing is used to select cards for functional operation. Messages and system status information can be displayed using the LCD display located on each I/O card. All test vectors were generated using third-party software tools.

Test Objectives

Techniques used with National's demo can be applied from system development to in-field operation. Boundary scan can detect and diagnose printed circuit board (PCB) and interconnect failures at all stages of the system's life cycle.

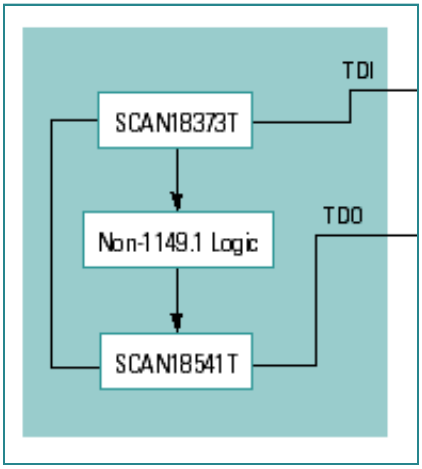
System-level test is a concern during development. Limited tester access typically forces system test to rely on functional patterns. This may lead to complex test patterns, poor fault coverage, and difficult failure diagnostics. Embedded, system-level boundary scan can replace many functional tests with simple and easily diagnosable tests.

Used in concert, boundary scan and functional test routines can maximize test effectiveness while reducing test development efforts.

Board & Backplane Test Points

The first step in implementing boundary scan is to integrate 1149.1 compliant components into the functional design. Maximizing the percentage of nets covered by boundary scan reduces the cost of other techniques and equipment *(such as in-circuit testers)* while increasing the ability to apply the benefits of boundary scan at later phases of the product's life cycle.

As the number and complexity of components increases, the development of test vectors becomes more difficult and diagnostic resolution increases. To increase the structural fault coverage on nets connected to devices which are not available with boundary scan, National's demo implements a "cluster test". *(see figure below)* A cluster test relies on at least two boundary scan components and a functional knowledge of the cluster (i.e., cluster of devices) connected between them. Using one 1149.1 compliant component to drive test vectors to the cluster and the other to receive expected data from the cluster, the structural integrity of the cluster can be evaluated.



System-Level Boundary Scan Access & Partitioning

National's demo interconnects the 1149.1 component TAP signals – TMS, TCK, TDI, TDO and TRST – at both board and system levels by adding a 5-bit bus to the backplane design and placing its Hierarchical and Multidrop Addressable JTAG Port (SCANPSC110F) component at the backplane interface of the processor card and each I/O card. The SCANPSC110F can efficiently interconnect and partition a 1149.1 compliant system at the board and system levels.

The ability to partition a board and system using the SCANPSC110F sim-

continued on page 4

Die Products Go Tape on Reel

Continued growth of the bare die and bumped die (flip-chip) market has included an increasing segment of high volume applications (e.g. automotive, computers, telecommunications). Because of tape on reel's proven characteristics of low cost and high-speed manufacturing, National Semiconductor's customers are increasingly requesting that die be delivered on tape on reel.

The speed and efficiency that tape on reel provides gives customers a competitive advantage. Carrier tape offers the high electrical and mechanical protection of National's other shipping media while additionally providing large die quantities on a single reel for greater efficiency. In fact, a single 13-inch reel may hold as many as 24,000 die. Tape on reel also offers the advantage of consistently providing die in one orientation and position for quick processing on an assembly machine. There is no need for the machine to waste time searching for the part or determining proper orientation. Reels, when used in a cassette format, may be plugged into or removed from an assembly machine in banks, allowing quick reconfigurations.

All of National's Known Good Die (KGD) products are available on tape on reel and have the option of 7-inch or 13-inch diameter reels. Two types of carrier tapes are available – embossed tape *(see figure 1)*, and adhesive-assisted tape *(see figure 2)*. Both carrier tapes are available in 8mm, 12mm, 16mm, and 32mm widths (tape width used is determined by die size). Embossed tape

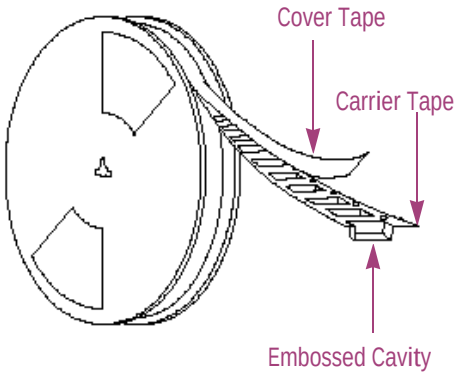


Figure 1

uses a close tolerance pocket to protect the die and maintain position. To keep the die in the pocket, a continuous strip of clear cover tape is applied to the top of the carrier tape as the die is placed. The cover tape is held in position by a pressure-sensitive adhesive along the edges.

The adhesive assisted carrier tape uses a punched cavity opening with pressure-sensitive adhesive at the bottom to hold the die in place. The pressure-sensitive adhesive is actually a strip on each side of the cavity bottom, which provides a gap for push pin removal of the die.

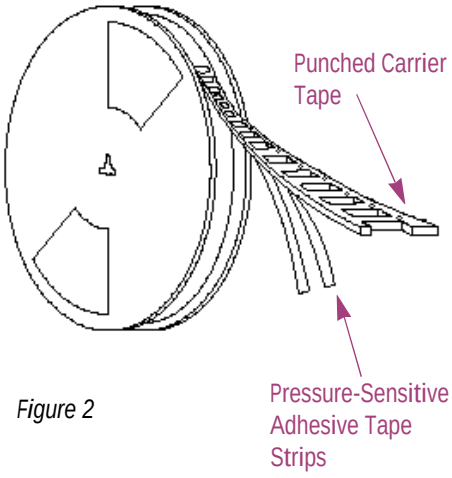


Figure 2

Purchasing die products from National Semiconductor is as easy as purchasing the more traditionally packaged ICs.

- National Semiconductor is a recognized industry leader in the development of die products, serving on numerous industry consortia and trade organizations, including SEMATECH, MCC's Die Products Consortium, IMAPS, and the Good Die Consortium in Europe.
- Products are available as either bare die (DC tested at +25˚C) or fully warranted Known Good Die.
- Full technical, QA, warehousing, customer service, marketing, and program management services are also available for customers that are interested in using die products in their applications.

For more information, please email us at milmktg@nsc.com.

Coming soon – KGD in flip-chip. Look for additional information in an upcoming edition of *Navigator*.

DS16F95 SMD Updates

Updates have been completed on the DS16F95 SMD to add new QML V and Q level products.

Device	SMD Designation
DS16F95J-QMLV	5962-8961501VPA
DS16F95WG/883	5962-8961501QXA

Updates have also been made to the DS16F95 to add RHA availability:

Device	SMD Designation
DS16F95JFQML	5962F8961501QPA
DS16F95WFQML	5962F8961501QHA
DS16F95WGFQML	5962F8961501QXA
DS16F95JFQMLV	5962F8961501VPA
DS16F95WFQMLV	5962F8961501VHA
DS16F95WGFQMLV	5962F8961501VXA

54AC299 RHA Approval

The FACT 54AC299 is now available with RHA guarantees to the R level [100 krad(Si)]. Packaging is CDIP, flatpak, and LCC.

Device	JM38510 SMD Part Number
54AC299	JM38510R76506SRA
	JM38510R76506SSA
	JM38510R76506S2A
	JM38510R76506BRA
	JM38510R76506BSA
	JM38510R76506B2A

Harris Is Out of the Logic Business

TI recently announced its intent to purchase Harris Semiconductor's commercial and military logic business, including the CD4K, HC/HCT, AC/ACT, and FCT product lines.

Unforeseen issues can arise when consolidating complimentary product lines, such as unexpected manufacturing problems and poor yields. Process transfers on mature products frequently cause parametric shifts and inability to meet published specifications. There is also risk of product obsolescence. The cost to transfer many of these functions can often exceed the revenue generated by the device, especially when some Harris products are duplicated by the TI portfolio.

National is here to support Harris' customers with availability of complimentary products as shown on page 7. This cross-reference guide is also available in pdf form on our web site at www.national.com/mil.

Coming soon in *Navigator* –

Low-Voltage Analog, Digital, and Interface Solutions

Scan Demo – continued from page 2

plifies test development, improves test efficiency, and allows failures to be diagnosed to the partition level without use of an off-line diagnostics tool. The demo system tests each board as a separate entity and tests the interconnects between the boards (i.e., the backplane), enabling each board to be tested separately and easily.

Embedded Boundary Scan Test Control

This boundary scan demo also provides the means to apply and evaluate boundary scan test vectors. For boards and systems which are tested using an external tester, the hardware implementation involves adding an applicable tester interface, e.g., additional pins on the edge connector, amd a special purpose connector/header or vias for ICT probes. For boards and systems which do not permit physical access and/or require self-test or remote test capability, the test control must be embedded within the system.

For designs which require embedded test control, the optimal hardware

continued on page 6

Harris Part #	Direct Replacement National Part #	Similar National Part #
CD54AC00F3A	54AC00DMQB	
CD54AC02F3A	54AC02DMQB	
CD54AC04F3A	54AC04DMQB	
CD54AC05F3A	54AC05DMQB	
CD54AC08F3A	54AC08DMQB	
CD54AC109F3A	54AC109DMQB	
CD54AC138F3A	54AC138DMQB	
CD54AC139F3A	54AC139DMQB	
CD54AC153F3A	54AC153DMQB	
CD54AC157F3A	54AC157DMQB	
CD54AC161F3A	54AC161DMQB	
CD54AC163F3A	54AC163DMQB	
CD54AC191F3A	54AC191DMQB	
CD54AC240F3A	54AC240DMQB	
CD54AC244F3A	54AC244DMQB	
CD54AC245F3A	54AC245DMQB	
CD54AC257F3A	54AC257DMQB	
CD54AC273F3A	54AC273DMQB	
CD54AC280F3A	54AC280DMQB	
CD54AC283F3A	54ACTQ283DMQB	
CD54AC299F3A	54AC299DMQB	
CD54AC32F3A	54AC32DMQB	
CD54AC373F3A	54AC373DMQB	
CD54AC374F3A	54AC374DMQB	
CD54AC534F3A	54ACT534DMQB	
CD54AC541F3A	54AC541DMQB	
CD54AC573F3A	54ACQ573DMQB	
CD54AC574F3A	54AC574DMQB	
CD54AC74F3A	54AC74DMQB	
CD54ACT00F3A	54ACT00DMQB	
CD54ACT02F3A	54ACTQ02DMQB	
CD54ACT04F3A	54ACTQ04DMQB	
CD54ACT05F3A		54AC05DMQB
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CD54ACT32F3A	54ACTQ32DMQB	
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CD54ACT374F3A	54ACT374DMQB	
CD54ACT533F3A		54ACQ533DMQB
CD54ACT534F3A	54ACT534DMQB	
CD54ACT540F3A		54FCT540DMQB
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CD54ACT573F3A	54ACT573DMQB	
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CD54ACT86F3A		54AC86DMQB
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JM38510/05003BCA	JM38510/05003BCA	
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7901502EA		7901501EA
8101602EA		8101601EA
8101801EA		8101803EA
8102001CA		8102002CA

Scan Demo – continued from page 4

implementation must enable both embedded and external tester access. This allows the design to benefit from the strengths of each method. The external tester offers the best means to develop tests for hardware debug and manufacturing.

National's demo system hardware supports both embedded and external test application. With the ability to address each card separately, embedded and external access is only required on the processor card. The processor card then acts as the master to test each card and the backplane. Re-use of test vectors at higher levels of integration minimizes the cost.

Test Application and Failure Diagnosis

A combination of external and internal tests are performed at all stages of a system's life cycle. For PCB prototyping and board/system manufacturing test, an external test is applied, followed by an embedded test. For field-level test, the opposite order is followed. The system is tested using the embedded tester and then, if necessary, tested using the external tester. The order of testing is dependent on the number of failures expected and the ability to diagnose failures with the embedded versus external test methods.

When using the field-level test aspect of the demo system, the objective is to quickly confirm that interconnects are sound and the system is functioning. Since the system was thoroughly tested in manufacturing, the likelihood of failure is low. For this reason, the embedded self-test is an ideal method of testing the system.

Tests are done at the board or subsystem level for most field applications. The goal in the field is to minimize system down time. If a failure is found, the board or subsystem is removed, replaced, and retested. Depending on cost, the board or subsystem is discarded or sent for repair. The demo system follows a similar routine. National's SCAN EASE software applies a separate test for each card and the backplane, then provides pass/fail diagnostics to the card/backplane level.

A System-Level Test Strategy and Technology Reusability Lower Total System Costs

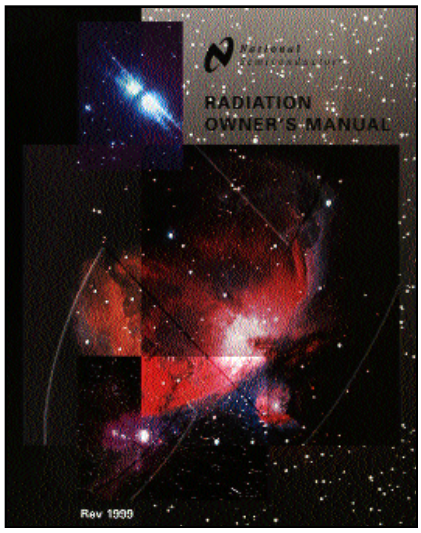
- The time and cost to develop the hardware and software for testing can be significant. Frequently much of this investment is used during the design debug and board manufacturing stage, and then dismissed for subsystem integration and system-level test. By reusing this technology throughout all stages of the product manufacturing phases, significant savings in development and manufacturing costs can be achieved and fault coverage can be extended.
- Once subsystem modules are integrated into the final complete system, the assembly is verified for the correct hardware and structural and interconnect integrity between subsystems is verified. Complete system test capability results from integrating the test patterns for the subsystems with test patterns for evaluating interconnects between subsystems. After the final system equipment is installed in the field, the ability to quickly identify and repair faults can also impact the total system cost by lowering the cost of maintenance contracts for post-sale support. Spare parts' inventory can be minimized by providing fault isolation to individual field replaceable units (FRU). Maintenance labor can be minimized through swift debug and replacement.
- Expand the use of the DfT strategy and boundary scan to the system level. Methods for partitioning and hierarchical access can enhance fault isolation by organizing the test access so subsystems can be tested independently. A single test bus and test master can control access in a multidrop environment for partitioning and hierarchy among subsystems, shortening scan chains to manageable lengths and optimizing test time versus fault isolation. Partitioning simplifies the management of in-system-configuration via scan ports (such as FPGA programming) and allows a test master to evaluate one part of the system while other subsystems fulfill their missions on-line.
- Adoption of a system-level test strategy offers life cycle benefits through design, manufacturing, and field-level maintenance and repair.

Field-Level System Test & Diagnostics

National's demonstration system is transported and presented around the world. To borrow the SCAN demo, please email National's Mil/Aero Marketing Group at milmktg@nsc.com. For additional information, vist the web site at www.national.com/scan and download Applications Note AN-1022, *Boundary Scan Silicon and Software Enable System-Level Embedded Test.*

Now Available! *Radiation Owner's Manual*

Working in the radiation environment requires much more insight than is available with the product specifications contained in a databook. It requires knowledge of the types of radiations to which a system may be subjected, the environments where each can be found, the severity of the adverse affects that can happen on a particular type of semiconductor technology, and the means to overcome these issues. We've included discussions on all of these topics – plus, of course, radiation test results on National's products – in the now-published *Radiation Owner's Manual*. Order your copy today by emailing us at milmktg@nsc.com.



"Ask Jackie..."

To "Ask Jackie", send your email to milmktg@nsc.com. In your subject line, please reference "Ask Jackie". Because of space, all comments may not be addressed in the column; but we will provide you with an answer.

Q. Why doesn't National publish skew specifications for products like ECL and FACT™?

anonymous

A. FACT and F100K 300 Series ECL families have been around for 10 to 12 years and are considered mature technologies. When these families were first designed and specified, logic clock frequencies were not pushing the limits in military systems like they are today. So, skew was not much of an issue and was not generally characterized or specified. That is, ***unless*** a clock driver device was designed specifically for mimimum skew such as the 100315 or the 54AC2525.

Q. Why are National's databooks so hard to get?

anonymous

A. National's databooks can be ordered from our web site at www.national.com/order/databooks.html. However, the number of new databooks being printed has dropped dramatically since all of this data is available on the World Wide Web and/or on CD-ROM. A special Mil/Aero CD-ROM is planned for later this year. You'll hear about it first in *Navigator*.

Note from the Editor

National Semiconductor is aware that some customers may be "upscreening" or "retesting" semiconductor components. Using components in applications or environments for which they were not intended can lead to component or system failure.

National offers a wide variety of COTS (Commercial Off the Shelf) component solutions to meet numerous application and environmental conditions. These COTS products are designed and manufactured to perform reliably in applications ranging from office desktop PCs to radiation-sensitive satellites.

We strongly recommend that National Semiconductor's products be used only within the electrical and environmental limits published in their respective datasheets. National does not authorize the use of any of its products beyond these published datasheet limits. Electrical and/or environmental testing or use of National products outside of the published datasheet limits voids all National warranties. National will not be responsible for any component or system failure due to inappropriate use of its products.

Should you have questions or comments, please contact your National Semiconductor representative.

Brochures/Design Information

For more information on National's Mil/Aero solutions:

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	Description	Lit. #
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	DS96F172,3,4,5 RS-485	550049-001
	LM6172	650274-001
	54ABT244J-QML	650280-001
	LVDS Quads Pitch-Pack	650288-001
	LP2956	650290-001
	LM7171	650295-001
	CLC452	660450-001
	CLC449	663049-001
	Available Brochures, Databooks	
	LVDS Owners' Manual	550062-002
	Known Good Die Line Card	650215-004
	Mil/Aero Products & Services Line Card	650217-001
	Mil/Aero 1998 Product Line Card	650214-001
*	Radiation Owner's Manual	650221-001
	Technologies for Space 1996	650271-002

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