NAVIGATOR
TECHNOLOGY DIRECTION FOR THE MIL/AERO COMMUNITY

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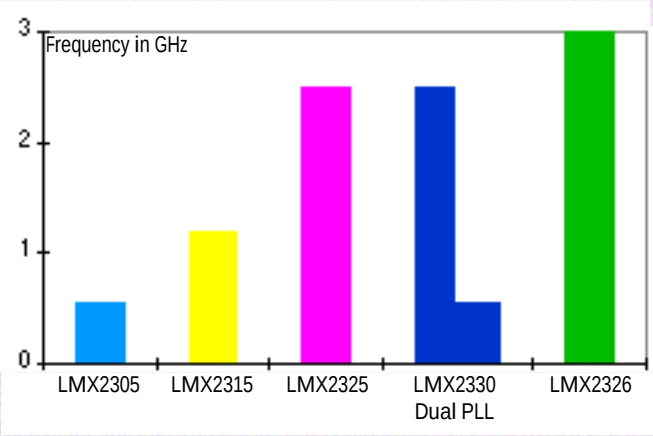
Phase Lock Loops Qualified for Military and Space Applications

Today's communications and signal processing design requirements dictate more processing capacity in smaller volumes, operation for longer periods of time, and lower power consumption. Meeting these demands in aerospace systems requires new technologies. Now available from National Semiconductor – radiation tolerant, high reliability, low power, high frequency phase lock loop (PLL) frequency synthesizers for use in space and military systems. This family features:

- ❏ Industry-leading monolithic PLL products
- ❏ Frequencies ranging from 550MHz to 3GHz
- ❏ Extensive characterization

Since any one device can mean the difference between a project's economic success or demise, the performance and reliability of a critical new technology is crucial. These military/aerospace PLLs will be produced to an SMD. Fabrication, assembly, and test will occur in National's QML- and QML V-certified facilities for maximum quality assurance. National's PLLs are built on a high volume, advanced BiCMOS process – not in a low volume, special process fab with non-DSSC-certified quality controls as

Planned Mil/Space LMX Series PLL Frequency Envelope



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Expand Board Test Strategies to the System Level for Life-Cycle Advantages

With Boundary Scan to test components and interconnects on printed circuit boards (PCBs) becoming mainstream, the next step is re-use of these test features in embedded system-level test to:

- ❏ Lower total system costs, i.e., technology reusability
- ❏ Yield significant improvements in fault detection and isolation at the system level

System developers and manufacturers that use boundary scan in their design for test (DfT) strategy have investments in software tools [for scan insertion and automatic test pattern generation (ATPG)] and in the training of their use. This development effort includes the generation of test vectors for testing individual PCBs — typically fault graded to a known level of fault coverage. These automated software tools provide complete coverage of the fault spectrum and reduce the time to develop a test solution.

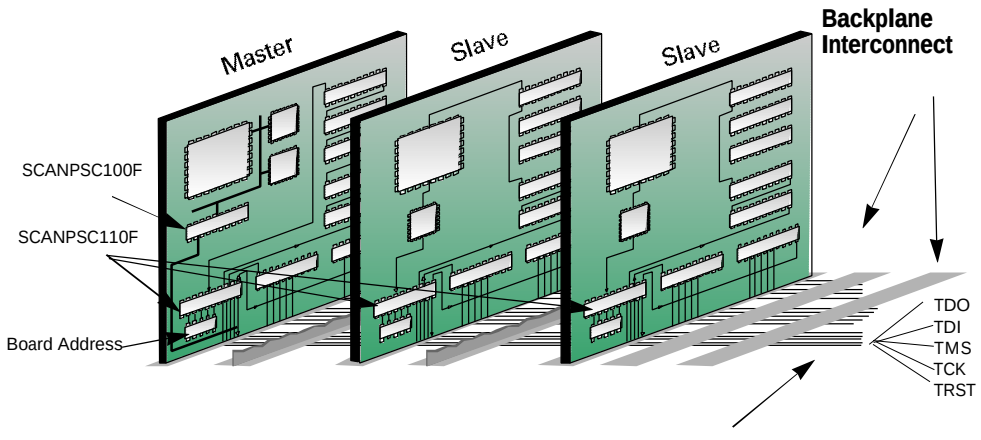
Unfortunately, much of the hardware and software investment is used during the design debug and board manufacturing stage, and then often dismissed during subsystem integration and system-level testing. National has the system test access SCAN solution that makes it possible to re-use this test technology throughout all stages of the product life cycle, achieve significant savings in development and manufacturing costs, and provide field test capabilities for superior value to the end user.

Re-using Test Vectors to Test a Complete System

Once testing is complete at the PCB level, boards are typically integrated into subsystems. Another set of tests verify that the assembly was done properly with the correct hardware, and detect structural and interconnect faults between boards. By integrating previously developed board-level test vectors with the subsystem-level interconnect test patterns, rapid verification of the subsystem's integrity can be achieved.

The next step integrates the subsystem modules to complete the system. Here the assembly is verified for correct hardware as well as the structural and interconnect integrity between subsystems. By once again integrating the test patterns for the subsystems with test patterns for evaluating interconnects between subsystems, there now exists the capability to test a complete system. A built-in capability for fast isolation of any faults would be verified to a specific PCB or interconnect between boards.

Once the final system equipment is installed in the field, continued re-use of test vectors provides the ability to quickly identify and repair faults. This reduces the system's overall operating cost by lowering the expense of post-sale support. The field service spare parts inventory is minimized as fault isolation to individual field replaceable units (FRU) is provided. Maintenance labor is also minimized through swift debug and replacement. Back in the maintenance depot, the test features are still in use to quickly repair the FRU.



IEEE STD. 1149.1 Multi-Drop System Test Bus

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National's New Family of QML and QML V PLLs

National Part #	SMD#
LMX2315WG-QML	5962-985001QXA
LMX2315WG -QML V	5962-985001VXA
LMX2325WG-QML	5962-985002QXA
LMX2325WG-QML V	5962-985002VXA
LMX2326WG-QML	5962-9861001QXA
LMX2326WG-QML V	TBD
LMX2305WG-QML	5962-9860901QXA
LMX2305WG-MLS	TBD
LMX2330AWG-QML	TBD
LMX2330AWG-QML V	TBD

often occurs with competitive devices.

PLL Characterization Testing

National's PLLs are qualified in its hermetic ceramic Small Outline IC (SOIC) surface-mount package. *(See SOIC article on page 5.)* In comparison with the plastic package, PLL evaluations in the ceramic SOIC indicate a higher lead inductance with resulting differences in RF performance. For example, phase noise at room temperature shows a 2dB - 8dB degradation (versus plastic package performance at 890MHz). Phase noise at 915MHz is nearly identical between the two package types (≤ 0.5dB difference). Spur data shows improved performance for the ceramic package. Extensive RF sensitivity test data is also available. As National's PLLs operate at supply voltages from 2.7V to 5V and have low current consumption (<8.5mA). They are ideal for low voltage designs.

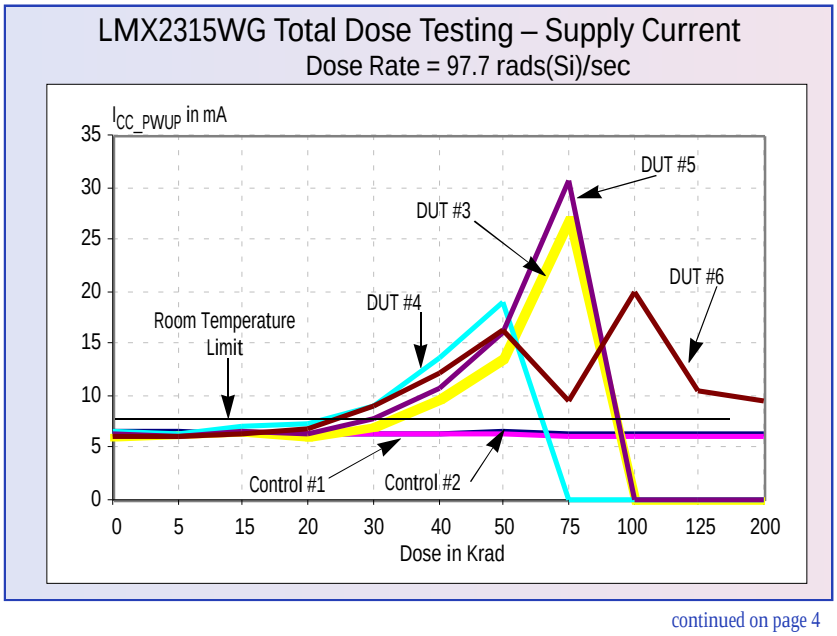
Other characterization data is being collected and will be made available upon demand.

National anticipates its PLLs will be characterized over the full military temperature range. At present the upper operating temperature is +105˚C. Cold testing is in process, and preliminary results are positive. The SMD will contain the final recommended operating temperature ranges.

PLL Radiation Testing

High dose rate (total dose) testing on the LMX2315's supply current is shown below *(tested in National Semiconductor's Santa Clara, California, Gammacell 220)*. This plot is typical of how the device has performed under total dose conditions. The LMX2315 generally remains within specification limits up to 25 krads(Si). From 25 krads to 50 krads, the device is fully functional with some parameters exceeding their pre-radiation specification limits. After 50 krads, device performance varies. As shown in the figure below, DUT #4 failed after 50 krads. While DUTs #3 and #5 are operable at 75 krads, they draw a larger supply current and eventually fail at 125 krads. DUT #6's supply current measurement fluctuated between 75 krads and 200 krads. DUT #6 remained operational after a dose of 200 krads. All post-irradiation exposure testing was done at room temperature per MIL-STD-883, Method 1019.4. The complete LMX2315 report will be available in July on National's web site at www.national.com/mil; then select the radiation home page link.

National has worked with NASA's Jet Propulsion Laboratory (JPL) to characterize how National's PLLs perform in a radiation environment. JPL's total dose testing included both high and low dose rate tests of the LMX2305 and LMX2325 devices.



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PLLs – continued from page 3

The high dose rate results generally agreed with National's total dose tests on the LMX2315. The low dose rate results showed less degradation for the same dose level, compared with high rate testing.

JPL's PLL testing with protons and heavy ions of the LMX2305 and LMX2332 devices encountered no single event latchup. SEU anomalies were quantified and deemed acceptable for its planned application.

Heavy ion testing has been performed both at Brookhaven National Labs and JPL. Proton testing was conducted at Texas A&M University Cyclotron. Brookhaven testing included use of gold, bromine, and lithium ions. The LMX2325WG exhibited no latchup to an LET of 84.1 MeV/mg/cm^2. Similarly, no latchup was observed during JPL testing in Pasadena with Californium fission fragments. The epi substrate of the ABiC IV process is credited for providing much of the PLL's single event latchup suppression.

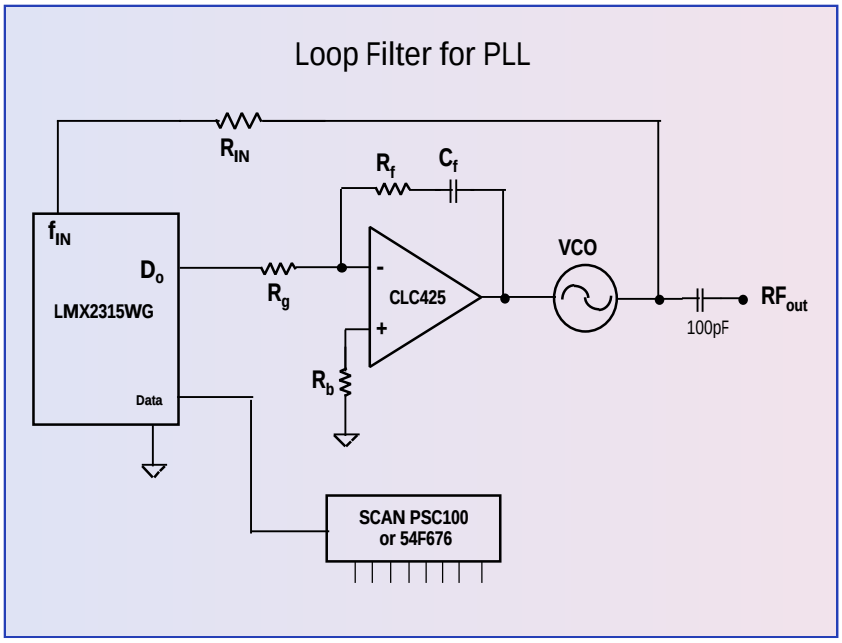
Independent Device Evaluations

JPL has performed extensive analysis of parts built on National's Advanced BiCMOS IV process (.8µ feature size). JPL in its construction analysis report (dated 4/30/97) stated *"… results of the construction analysis … on the LMX2315 confirms that National Semiconductor maintains an excellent process fabrication and quality control for this product. This is evident in the quality of the wire bonds, and especially in the quality of the chip's two-level layered metal interconnections, which exhibit excellent step coverage, metal line width pattern, and very good alignment at the contacts."*

Additional evaluation has been done by a major commercial satellite manufacturer, which has selected National's LMX2315WG for its communications satellite. These satellites rely on National's PLLs in its critical communications payload. Similarly, the LMX2305 and LMX2325 have been designed into JPL's EOS-MLS satellite.

Supporting Silicon

In many broadband tuning applications, it is necessary to supply a higher tuning voltage than the PLL can create, or to isolate the D_O output voltage from successive stages. This necessitates the need for active devices in the loop filter. As these active devices introduce noise, it is important to minimize these adverse effects. The circuit implementation *(see figure below)* works toward centering the D_O output voltage. National's CLC425AJ-QML (Very Low Noise Op Amp) with its ultra low input noise voltage level specification of 1.05nV/√Hz and low current noise of 1.6pA/√Hz makes it ideal for isolating the D_O output from successive stages.



If amplification of D_O from a 0V - 5V range to a 0V - 15V range is required, then current noise becomes a critical factor. National has three op amp options for this task – the LM6142, LM6172, and LM7171. Each may be used in the inverting configuration as shown in the figure above. The LM6142AMJ-QML has an ultra low current noise of 0.22pA/√Hz that helps to minimize noise effects when boosting the D_O voltage.

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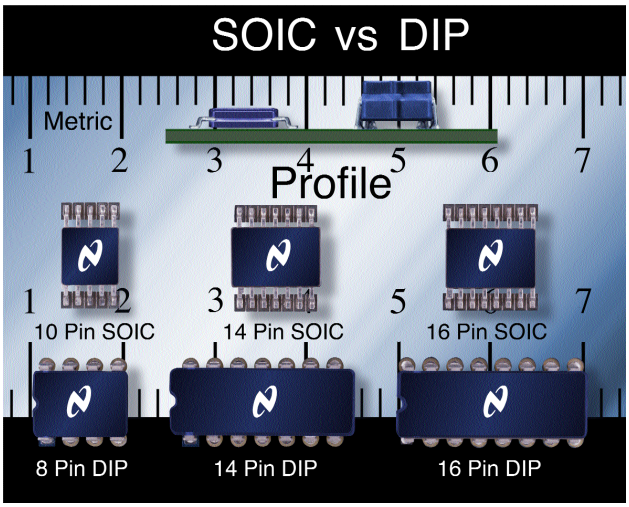
The World's First QML ICs in Ceramic SOIC

Meeting the demand for smaller footprint, lighter, hermetic, surface-mount ICs for portable, avionics, and satellite applications are National's QML-certified devices in the new ceramic SOIC (Small Outline Integrated Circuit) package.



This new package emulates the JEDEC standard for plastic wide-body (300 mil) SOICs while providing the reliability and heat dissipation characteristics the military market demands. Since the outline is similar to that of a standard plastic wide-body SOIC, it can be easily integrated into a surface-mount production line with little or no retooling. Products come from National fully tested and guaranteed.

National's ceramic SOIC package has a typical footprint reduction of 37%, typical profile reduction of 61%, and typical weight savings of 80% as compared with ceramic DIPs. High power devices and devices targeted at high heat applications are offered in packages constructed of aluminum nitride rather than standard alumina. Aluminum nitride packages have nearly nine times the thermal conductivity of a standard alumina package: 150W/m˚K versus 18W/m˚K (typ).

For additional ceramic SOIC information including package drawings and datasheets, please visit our web site at www.national.com/mil or send an email to milmktg@nsc.com.

These devices available in National's ceramic SOIC package. They are manufactured in accordance with MIL-PRF-38535 in National's QML facilities and are guaranteed over the full military temperature range.

Part Number	Part Number	Part Number
DS26C31MWG/883	LM139AWG-QMLV	LM6165WG/883
DS26C32AMWG/883	LM139AWG/883	LMC6464AMWG-QML
LM108AWG/883	LM139WG/883	LMX2315WG-MCP*
LM111WG/883	LM6161WG/883	LP2951WG/883
LM119WG/883	LM6162WG/883	LP2953AMWG-QMLV
LM124AWG/883	LM6164WG/883	LP2953AMWG/883
LM124WG/883		** Guaranteed from -40˚C to +125˚C*

These devices are undergoing qualification.

Part Number	Part Number	Part Number
CLC414AWG-QML	LM2990WG5.0-QML	LM6165WG-QMLV
CLC420AWG-QML	LM2990WG-12-QML	LM7171AMWG-QML
DS16F95WG/883	LM2990WG-15-QML	LMC6442AMWG-QML
LM12H458MWG/883	LM2991WG-QML	LMC6484AMWG/883
LM2940WG5.0/883	LM3940WG3.3-QML	LMX2315WG-QML
LM2940WG8.0/883	LM6172AMWG-QML	LMX2315WG-QMLV
LM2940WG-12/883	LM6161WG-QMLV	LMX2325WG-QML
LM2940WG-15/883	LM6162WG-QMLV	LMX2325WG-QMLV
LM2941WG/883	LM6164WG-QMLV	

These devices are being considered for qualification.

Part Number	Part Number	Part Number
JL108ABZA	JL124ASZA	JL139BZA
JL108ASZA	JL124BZA	JL139SZA
JL117-.5BZA	JL124SZA	JL148BZA
JL117-.5SZA	JL137-.5BZA	JL148SZA
JL117-1.5BZA	JL137-.5SZA	LM6172AMWG-QMLV
JL117-1.5SZA	JL137-1.5BZA	LM7171AMWG-QMLV
JL124ABZA	JL137-1.5SZA	

National is pursuing suggestions and feedback regarding future devices in the ceramic SOIC package. If you have questions or need more information regarding this package, please send a note to milmktg@nsc.com.

Board Test – continued from page 2

SCAN Provides the Solution

Expanding your DfT strategy and boundary scan to the system level requires a few special considerations. Methods for partitioning and hierarchical access are needed to enhance the fault isolation by organizing the test access such that subsystems have independent access. A single test bus and test master can control access in a multidrop environment. This

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Reserve a SCAN Demo

Use National Semiconductor's SCAN Demo Board to help you perform boundary scan tests.

The Demo

The SCAN Demo contains a hardware tool kit and a software package. Use it to individually scan any board ... or to execute interconnect tests between boards on the backplane. The tool set is engineered to make it easy to include and use boundary scan. The hardware kit includes a multidrop backplane board connected to a processor card (i.e., the SCAN Master Board). The backplane is populated with two slaves, plus three empty slots.

The SCAN Master Board is comprised of a microcomputer interfacing with the system test access (STA) bus, an address data bus, a communication port (RS232), and National's SCANPSC100F Embedded Boundary Scan Controller. The communication port is used to upload test results and download test vectors.

The SCANPSC100F serializes out-going parallel data from the microprocessor and controls the test clock (TCK). It then inputs them to the backplane test bus downstream to the SCAN Bridges that connect with the system test access (STA) bus.

Each slave contains an LCD to display messages on the card, an EPROM to store messages, and an address/data bus interface.

Both the master and slave cards have a SCANPSC110F Bridge. The Bridge is connected to the STA bus and can perform hierarchical and multidrop addressable testing. This enables the user to address a particular card to participate in boundary scan testing, or to partition a board or a system into more manageable sub-systems for scan test operations.

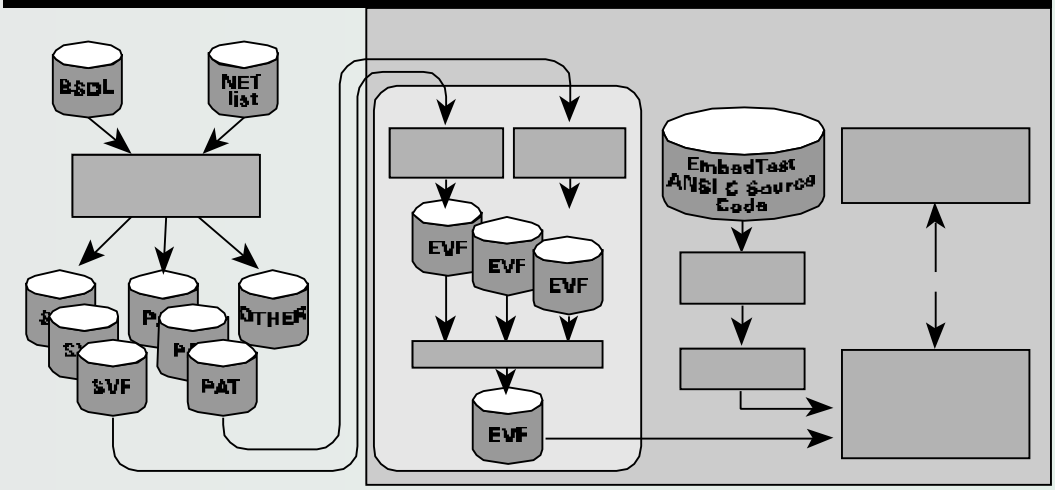
SCANEASE Software

SCANEASE test management software accompanies the hardware. Its algorithms provide a platform for remote access and to administer boundary scan tests over an IEEE 1149.1-compliant bus. SCANEASE tools also enable customers to convert test vectors generated by Automatic Test Pattern Generation (ATPG) [tools like Teradyne's VICTORY and JTAG Technologies' Vector Interface Package (VIP)] to be embedded within the IEEE 1149.1-compliant system.

National's SCAN Demo is a comprehensive and practical aid in implementing boundary scan technology. It vividly demonstrates how complex systems can be controlled and evaluated for optimal test results.

To schedule use of the SCAN Demo, contact Carrel D'Haiti (207-541-6471, carrel.d'haiti@nsc.com).

SCANEASE Embedded Application Software Enabler



PLLs – continued from page 4

The LM6172AMxx-QML and LM7171AMxx-QML are available in the hermetic SOIC package for surface-mount applications or CERDIP for through hole applications. The CLC430AJ-QML may also be used if a non-inverting amplifier configuration is desired. Should the host device controlling the PLL's input data have parallel outputs, National's SCANPSC100F (Embedded Boundary Scan Controller) or 54F676 (16-Bit Serial-Parallel-In/Serial-Out Shift Register) can convert parallel data to serial data for input into the PLL's serial data line. Each of these devices is available in flat-pak or CDIP; the SCANPSC100F is also available in an LCC package.

Further Information

A variety of PLL application notes and datasheets are available. Application Notes AN-885, AN-1000, and AN1001 reference PLL design and usage. Application notes regarding high-performance filters constructed with National's Comlinear op amps are included in OA-26, OA-27, OA-28, OA-29. Copies may be obtained by downloading the .pdf file from the National Semiconductor web site (www.national.com) Or contact Larry Dano at 408-721-2582 (larry.dano@nsc.com). In Europe, contact Petra Pavel at 49-8141-351495.

The author thanks Shri Agarwal and Gary Swift of JPL for assistance in reviewing this article.

Featured in the next edition of *Navigator* –

Fast CMOS translation –

The solution for mixed-supply systems

Board Test – continued from page 6

allows partitioning, creates a hierarchy among subsystems, and shortens scan chains to a manageable length to optimize test time versus fault isolation. Partitioning also simplifies the management of in-system-configuration via scan ports (such as FPGA programming) and allows a test master to evaluate one part of the system while other subsystems fulfill their mission in on-line mode.

National Semiconductor's SCAN products support DfT at the system level with the hierarchical, multidrop addressable JTAG port (SCANPSC110F) and the Embedded Boundary Scan Controller (SCANPSC100F).

Also available is SCANEASE shareware for embedded application of boundary scan. If system-level test is in your test development roadmap, our System Test Demo kit (available on a limited basis) demonstrates how a system-level test architecture can be implemented.

Adoption of a system-level test strategy has many life cycle benefits through design, manufacturing, and field-level maintenance and repair. By coupling technology re-use with the application of board-level test development efforts, your test approach can expand to cover all stages of the product life cycle. Reduced costs and shortened development and debug time can enhance the value of your products for faster time to market.

For more information about National's SCAN products, shareware, or to inquire about availability of our SCAN demo kit, check our web page at www.national.com/mil/SCAN/scanpage.html, or contact Carrel D'Haiti (207-541-6471, carrel.d'haiti@nsc.com), Brian Stearns (207-541-8671, brian.stearns@nsc.com), or Bill Aronson at (207-541-8223, bill.aronson@nsc.com). In Europe, contact Petra Pavel at 49-8141-351495.

Neutron Testing

Neutron radiation causes lattice structure damage in bipolar devices, thereby affecting a device's minority carrier life time and transistor gains.

National Semiconductor recently conducted neutron irradiation on three logic technologies – TTL (FAST™ logic), BiCMOS (ABT logic), and ECL bipolar (F100K 300 Series ECL). Tests were coordinated by National's Radiation Effects Lab (REL) in South Portland, Maine. Neutron irradiation of National's 54ABT244, 54F373, and 100331 product types were conducted by White Sands Missile Range using a Fast-Burst Reactor with a background total dose level of less than 1300 rads(Si) at 5E12n/cm^2.

The 54F373 Octal Transparent Latch with TRI-STATE outputs is manufactured on the FAST-M process. This process is an isoplanar, recessed oxide isolation technology. The 100331, low power ECL Triple D Flip-Flop product is produced on the FAST-LSI process using advanced isoplanar techniques, doped-field oxide, and improved metalization techniques. The 54ABT244 Octal Buffer/Line Driver with TRI-STATE Outputs device is built with high speed Advanced BiCMOS technology (1.0µm feature size) using a P-substrate and P-Epi wafer. This process combines bipolar and CMOS transistors in a single process.

The results of the neutron testing for these three technologies indicated there was no neutron radiation sensitivity up to 5E12 n/cm^2. All parametric limits for each function were well within the pre-radiation values as noted in the table below.

Neutron Sources

- ❏ Nuclear explosion
- ❏ Nuclear reactors
- ❏ Radioactive contaminants
- ❏ Integrated circuit manufacturing equipment (ion implanters, plasma etchers, etc.)

Total ionizing dose irradiation testing is also being performed on these products. Results will be published in an upcoming edition of *Navigator*.

For additional information, contact Mike Maher (207-541-8391, mike.maher@nsc.com). In Europe, contact Petra Pavel at 49-8141-351495.

Test Results – Neutron Irradiation

Part Type	Parameter	Pre-Radiation	Post-Radiation	Pre-Radiation Limit
FAST TTL Logic				
54F373	I_{CCZ}	34.5mA	35.0mA	55mA (max.)
	I_{IL}	-443.0µA	-379.0µA	-600µA (min.) -250µA (max.)
	I_{IH}	24.0nA	119.0nA	20µA (max.)
	V_{OH}	2.92V	2.94V	2.5V (min.) 5.0V (max.)
	V_{OL}	387.0mV	383.0mV	500mV (min.)
F100K 300 Series ECL Logic				
100331	I_{EE}	-84.6mA	-84.6mA	-122mA (min.) -65mA (max.)
	I_{IL}	78.0µA	77.0µA	0.5µA (min.)
	I_{IH}	135.0µA	131.0µA	240µA (max.)
	V_{OH}	-933.0mV	-931.0mV	-1025mV (min.) -870mV (max.)
	V_{OL}	-1699.0mV	-1696.0mV	-1830mV (min.) -1620mV (max.)
ABT Logic				
54ABT244	I_{CC}	119.0nA	244.0nA	
	I_{IL}	-5.0nA	4.0nA	-5µA (min.)
	I_{IH}	-8.0nA	16.0nA	5µA (max.)
	V_{OH}	2.94V	2.95V	2.0V (min.)
	V_{OL}	353.0mV	347.0mV	0.55V (max.)

PURCHASING CORNER

Looking for SRAM Known Good Die?

National Semiconductor can help. In spite of our exit from the packaged goods business, National remains actively engaged in testing and selling military-grade SRAM die in Known Good Die form. Through an agreement with Galvantech, National is obtaining 128K x 8 asynchronous SRAM die which National is testing to military temperature specifications and offering as standard and low power product with 15ns access times. Full KGD datasheets are available with X,Y coordinates, die layout, and electrical performance tables.

Pricing is substantially below the packaged pricing for 1 Meg SRAMs to full Mil specifications.

Watch *Navigator* for announcements about a 4 Meg SRAM Known Good Die which is currently in qualification to the full military flow.

For more information contact National Semiconductor's authorized die processors – Chip Supply and Minco in the United States; and Die Technology, Ltd., and Mintech, Ltd., in the U.K. Or contact Bruce Blaisdell (207-541-8896) in the U. S. and Petra Pavel (49) 8141- 351495 in Europe.

SRAM Known Good Die – Available from Stock

For low-power applications
NS41024L15MDA

For standard-power applications
NS41024S15MDA

Note: Packaged products not available

NEW RELEASE

CLC452 Drives Low-Impedance, Highly Capacitive Loads

- ❏ Sources up to 100mA
- ❏ Drives a 100Ω load within 1.0V of either supply rail
- ❏ Consumes minimal quiescent supply current (3.0mA) from a single 5V supply
- ❏ Maintains consistent performance over a wide range of gains and signal levels
- ❏ Linear-phase response up to one half of the -3dB frequency
- ❏ 400V/µs slew rate
- ❏ 4.5ns rise/fall times (2V step)
- ❏ 130MHz small-signal bandwidth
- ❏ Qualified over the military temperature range

For more information on the CLC452 single supply, low power, high output, current feedback amplifier, visit National at www.national.com. To reserve a copy of the upcoming CLC452 pitch-pack or for answers to other questions, email shawn.turschak@nsc.com. In Europe, contact Petra Pavel at 49-8141-351495.

Applications for National's CLC452

System	Application	Key Features
Data transmission	Point to point through Twisted Shielded Pairs (TSP)	Low harmonics, high output current
Coax cable drivers	Video line driver for moving map, displays, weapon video	Wide bandwidth, low DG/DP, low power
Digital video	8 to 10-bit video ADC driver 8 to 10-bit video DAC buffer	Low harmonics, low DG/DP Low harmonics, high speed
Instrumentation	Portable test/measurement	Low power, high speed, low distortion
Communications	High speed modems	Low power, high output current

WEB CORNER

Boundary SCAN on the Internet

New to National's Military/ Aerospace web page (www.national.com/mil) is a link to information on our Test products: *Boundary Scan (IEEE1149.1) and System Test Support Products.* Accessing this link brings the user to another web page which contains:

- **Literature: White Papers & Application Notes**
  - Non-Contact Test Access for Surface-Mount Technology
  - Design of a Parallel Bus-to-Scan Test Port Converter
  - Structural System Test via IEEE Std 1149.1 with PSC110F Hierarchical & Multidrop Addressable JTAG Port
  - Embedded IEEE 1149.1 Test Application Example
  - Boundary Scan Silicon & Software Enable System Level Embedded Test
- **Hardware: Silicon Product Datasheet Information**
  - SCAN18245T Non-inverting 18-bit Transceiver w/TRI-STATE Outputs
  - SCAN18373T Transparent Latch w/TRI-STATE Outputs
  - SCAN18374T D Flip-Flop w/TRI-STATE Outputs
  - SCAN18540T Inverting Line Driver w/TRI-STATE Outputs
  - SCAN18541T Non-Inverting Line Driver w/TRI-STATE Outputs
  - SCANPSC100F Embedded Boundary Scan Controller
  - SCANPSC110F Heirarchical & Multidrop Addressable JTAG Port
- **Software: Support Tools**
  - SCANEASE (Embedded Application Software Enabler) Datasheet and Shareware download
  - BSDL – Boundary Scan Description Language models

Links are also provided to other sites. Updates to this site will be made as more information becomes available.

For more information, contact Bill Aronson, applications (207-541-8223, bill.aronson@nsc.com) or Brian Stearns, marketing (207-541-8671, brian.stearns@nsc.com).

New Certificate of Conformance System Includes Attribute Data

Effective June 1, 1998, there is a new, value added, automated Certificate of Conformance for all compliant Military/Aerospace products that National Semiconductor ships. This is the final step in the automated Quality Conformance Inspection (QCI) system that National has been developing.

In addition to the data that National has historically included, this revised Certificate of Conformance now includes complete Groups A, B, C, and D data attributes for every lot shipped. This new fully automated system links directly into National's QCI database.

As this is an enhancement to National's existing system and not a baseline change, a Product Change Notice (PCN) will not be issued. This system is not retroactive to lots previously shipped.

For additional information, contact Tom Stortini at 408-721-4993 or tom.stortini@nsc.com.

- ❏ No-cost Certificate of Conformance
- ❏ Now includes Groups A, B, C, and D data attributes
- ❏ Unique serial number provides lot traceability
- ❏ Reference the serial number when inquiring about a shipment or a return without sending a copy of the Certificate of Conformance.

To "Ask Jackie" use the attached reply card, fax "Ask Jackie" at 207-541-6140, or EMAIL jacqueline.l.collard @nsc.com. Because of space, all comments may not be addressed in the column; but we will provide you with an answer.

Q. When available, I would like the *Owner's Manual for Radiation Products & Services*.

William Morgan, Tracor Aerospace Electronic Systems

A. You have been added to our distribution list! At this point, we are finalizing the contents of this publication and expect it to become available in mid-summer. Watch for an announcement in our next edition of *Navigator*.

Q. Now that National has acquired Cyrix, are there any plans to offer microprocessors as Known Good Die?

anonymous

A. National is in the preliminary stage of developing a strategy to offer Cyrix processors as KGD. Look for announcements in *Navigator* later this year. If you would like to comment on this future offering, please contact Bruce Blaisdell in the U. S. at bruce.g.blaisdell@nsc.com, 207-541-8896; or Petra Pavel in Europe at petra.pavel@nsc.com, (49) 8141-351495.

Q. Why are the new products on the Mil/Aero www site about one-year old?

anonymous

A. While National was developing a revised Mil/Aero web site, it was decided to keep all new items (i.e., introduced within the last twelve months) listed under the "new products" section. The revised web page is now available. Please stop buy and visit at:

www.national.com/mil

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