National Semiconductor®

NAVIGATOR

TECHNOLOGY DIRECTION FOR THE MIL/AERO COMMUNITY

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Industry Migrates to Bare Die and Known Good Die – Virtual Packaging

It was just a few years ago that electronics designers who wanted the smallest form factor for system upgrades were limited to assorted surface-mount packages. More recently, this has included BGA and CSP packaging. While some larger semiconductor producers, such as Motorola and IBM, long ago developed bare die and known good die for in-house flipchip and chip-on-board technologies, they remained proprietary, and were not offered to the general market.

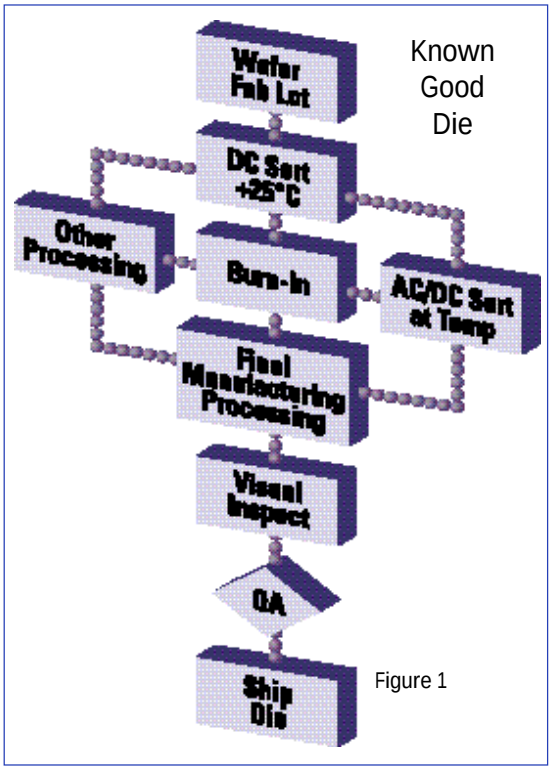

Figure 1

Today this is changing. Bare die and known good die are available from multiple sources. Die offerings span most technologies.

To reduce weight, manufacturers are coming to prefer bare die in applications such as chip-on-board (COB), flip-chip, wire bond, and chip-on-flex. As a bonus, using die versus packaged parts can also result in lower costs for both components and substrates.

According to a recent market analysis commissioned by SEMATECH, bare die usage comprised only 7% of the 53 billion integrated circuits manufactured in 1996. By the year 2001, this is expected to grow to 11% of the 85 billion integrated circuits forecast to be manufactured. That's over 9 billion bare die and known good die! The trend is clear. If you haven't yet designed with bare die, you will soon.

National Offers Alternatives

There are no universal definitions of bare die and known good die. At National Semiconductor our customers may select from two basic categories of die products. The

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INDUSTRY ISSUE

Radiation Design Considerations

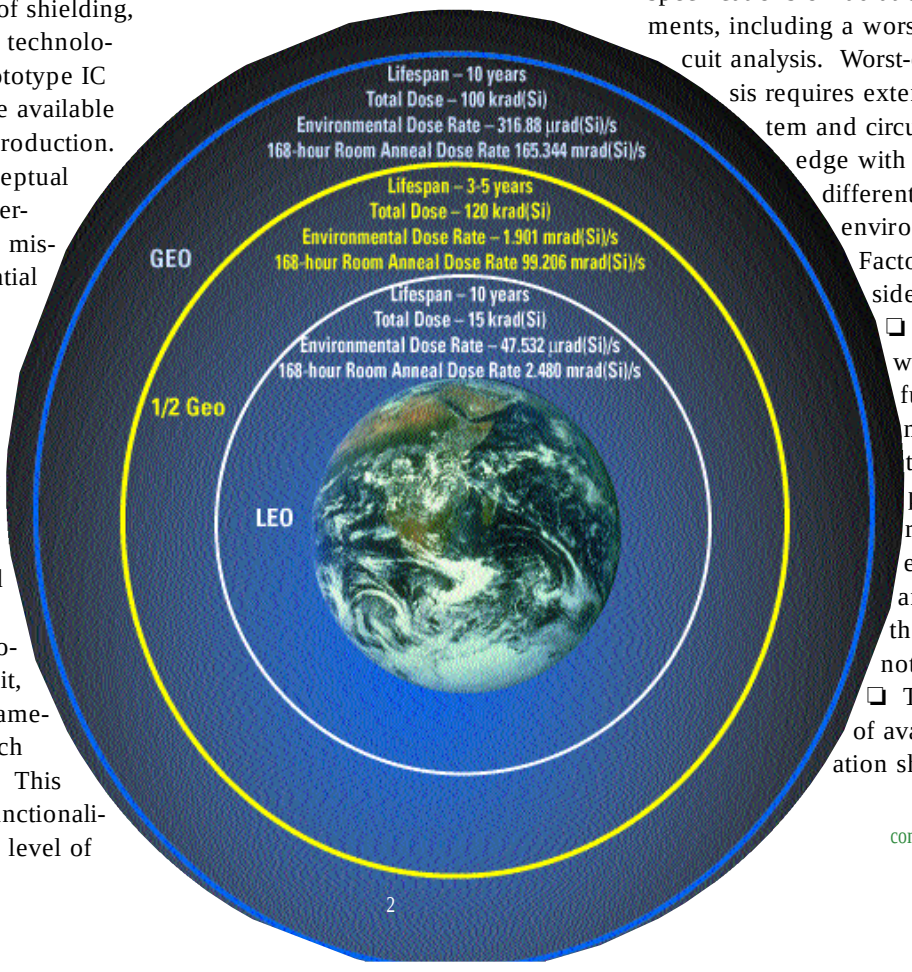
Designing and producing a radiation-hardened system is time extensive and financially expensive. Rather than meet premature demise due to inadequate radiation design, precautions can enable systems to survive their full life expectancies.

The most efficient and cost-effective approach to designing a radiation-hardened system is to start at the conceptual stage. This is where proper evaluation and selection of semiconductor technology and other factors occur, i.e., determining the extent of shielding, selecting viable existing technologies, and evaluating prototype IC technologies that will be available when the system is in production. Most critical at the conceptual stage is a thorough understanding of the system's mission relative to its potential radiation environments.

Incorporating Radiation Design

To ensure the best RHA (Radiation Hardness Assurance) design, it is necessary to understand the complete radiation response of each component in the system circuit, e.g., what electrical parameters are affected by which radiation environments. This includes variable and functionality (attribute) data to the level of radiation failure. Variable data as performed in a step-stress radiation approach permits observance of non-monotonic behavior for each electrical parameter's radiation response. For example, standby current of a non-hardened field oxide is non-linear and exhibits significant increases in value above its pre-radiation value.

When designing a radiation-hardened system, guidelines must be based on the system's mission and required survivability. After the conceptual phase comes selection of the proper components for the investigative Engineering Development Phase. This is often the most costly phase as testing procedures include components, circuit board, systems assembly, and software documentation.



Once the radiation environment is identified, radiation test procedures must be set and a Hardness Assurance Plan & Program instituted. Establishing a Change Control Board ensures that circuit design modifications do not impact the system's hardness assurance.

When a system design is approved to radiation-hardness criteria, other documentation must be initiated to prevent compromise to the established radiation hardness level. Written specifications include radiation test conditions. Acceptance test procedures ensure that components identified to HCI (Hardness Critical Items) specifications are properly tested.

Part procurement drawings, assembly drawing schematics, and purchase orders require complete specifications of radiation requirements, including a worst-case circuit analysis. Worst-case analysis requires extensive system and circuit knowledge with respect to different radiation environments. Factors to consider include:

- ❑ Analysis of which circuit functions must operate through a particular radiation environment and those that would not
- ❑ The amount of available radiation shielding

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Bare Die & Known Good Die, cont. from page 1

distinction between them comes in the level of assurance that accompanies each category.

National's Known Good Die (KGD) is sold fully warranted to perform to datasheet electrical specifications – the same way our packaged products are sold. The process used to achieve this level of assurance may vary from product to product, depending on the technology, maturity of the product, and temperature range over which it is specified. In this respect, National's KGD testing is the same as testing packaged products. A typical KGD process flow is shown in Figure 1 *(see page 1)*. KGD pricing varies from 70% to 150% of the pricing for comparable packaged parts, due to the variability of the testing flows. NRE (non-recurring engineering) charges may be assessed to develop KGD testing for non-standard products. KGD datasheets include electrical tables, X, Y coordinates, bonding diagrams and physical information such as bond pad size and composition, backside potential, passivation, etc.

The alternative to KGD is bare die. National Semiconductor bare die are subjected to DC test at +25˚C, then visually inspected. Although bare die is not warranted to yield over temperature to a particular specification, products sold as bare die are usually those with well established, stable manufacturing processes. This is a high yield, low cost choice for many applications. A typical bare die process flow is shown in Figure 2. Prices for volume purchases are typically well below packaged good prices. Bare die data-sheets also include

Figure 2

X,Y coordinates, bonding diagrams and physical information. They do not include electrical specifications.

Both bare die and KGD can be ordered in commercial, military, and S level grades for many products. Optional testing, such as Total Dose RHA testing and Lot Acceptance Testing, are available on select products.

Choosing the Right Die Process for Your Application

The next step is to choose the process that is right for your particular program. Unless you are manufacturing for an extremely weight- or space-sensitive application, your choice may depend on simple economics – the bare die will cost less to purchase than the KGD. Depending on your design, this cost differential may be offset by the difference in yield between the bare die and KGD. This, in turn, will be depend on the ability of your manufacturing process to tolerate rework or to accept scrap.

Figure 3 below illustrates this relationship. The X axis represents the number of die in your module or chip-on-board application. The Y axis is the first-pass yield of your product, and the curved lines are the average yield of the die you have chosen. For example, in a hybrid with only five die, you might elect to use bare die, each of which averages 97% yield for your application. This will result in a first-pass yield for your hybrid of 86%. Now you need to decide whether your business model can accept this yield and remain competitive. If not, you may choose to rework the hybrid by identifying and replacing the defective die, or use KGD, at a higher initial price, but with a 99.99% yield. The

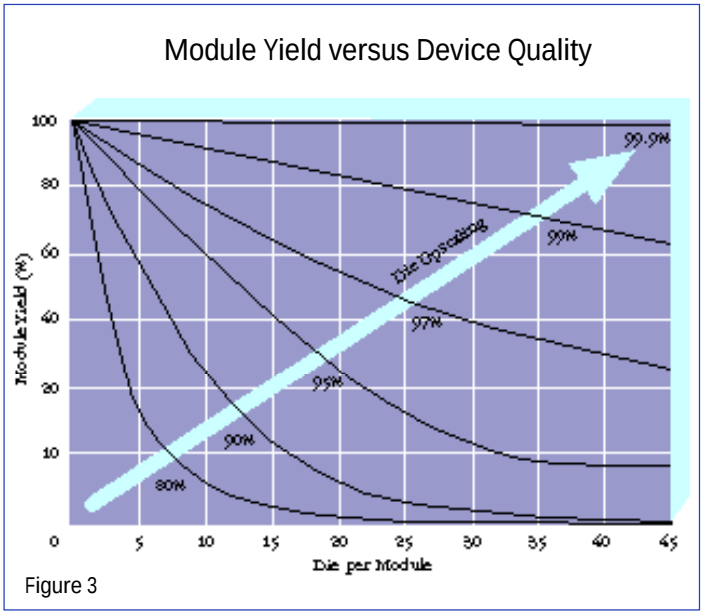


Figure 3

continued on page 4

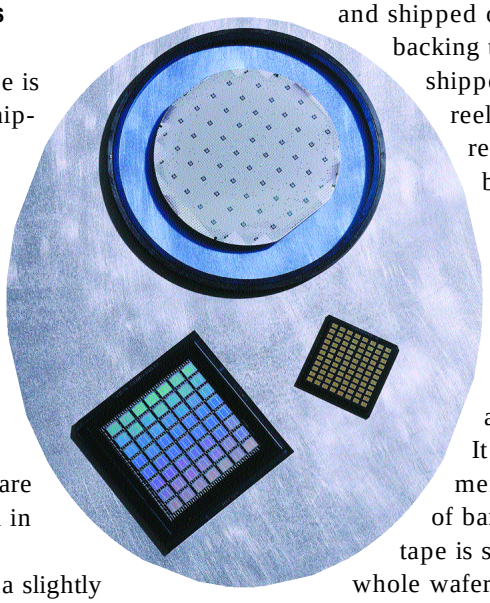
Bare Die & Known Good Die, cont. from page 3

answer depends on which result is the less expensive option. As the product you are manufacturing becomes more complex, the case for KGD grows stronger. A module with 25 devices – each one averaging 97% yield – results in a first-pass module yield of only 45%. In this scenario it is likely that either rework or the use of KGD is mandatory. The decision tree in Figure 4 depicts these tradeoffs.

If your process cannot tolerate rework or if the cost of rework is too high, your choice is KGD. If rework is easily accomplished, you may elect bare die in either commercial, military, or S level grades.

National can help you to assess these choices. Under a Non-Disclosure Agreement (NDA), we will share with qualified customers yield data based on our packaged goods experience in order to evaluate the tradeoff between bare die and KGD. We want you to reach a solution that fits your economic model.

Shipping Options



Your final choice is in selecting a shipping method. For orders where no customer preference is stated, die is shipped at National's discretion in either waffle packs or GelPaks. Both are well established in the industry.

GelPak uses a slightly tacky membrane to hold die in place. It is flexible in the range of die sizes that it will accept. In very sensitive applications, the issue of membrane residue may need to be evaluated.

Waffle Pack depends on cavities in a plastic grid to hold die in place. In order to be effective, the cavities must closely match the die dimensions to prevent die rotation or excessive movement in shipping which can cause chipping.

For large orders, National offers the additional choices of die diced and shipped on adhesive backing tape or die shipped as tape and reel. The issue of residue must also be considered for die shipped on tape. This method is recommend only where die will be used immediately on arrival. It is not recommended for storage of bare die. Die on tape is sold only in whole wafer multiples. National is preparing to offer tape and reel, using a tape developed by 3M that employs embossed cavities to hold the individual die in place. Orders for tape and reel must be in multiples of a whole reel quantity.

For additional information on National Semiconductor's Die Processing Program, please use the attached card to request our *Known Good Die/Die Processing Line Card*. Or contact Bruce Blaisdell at 207-541-8896 (bruce.g.blaisdell@nsc.com).

In Europe, contact Petra Pavel at +49-8141-351495.

Die Product Decision Tree

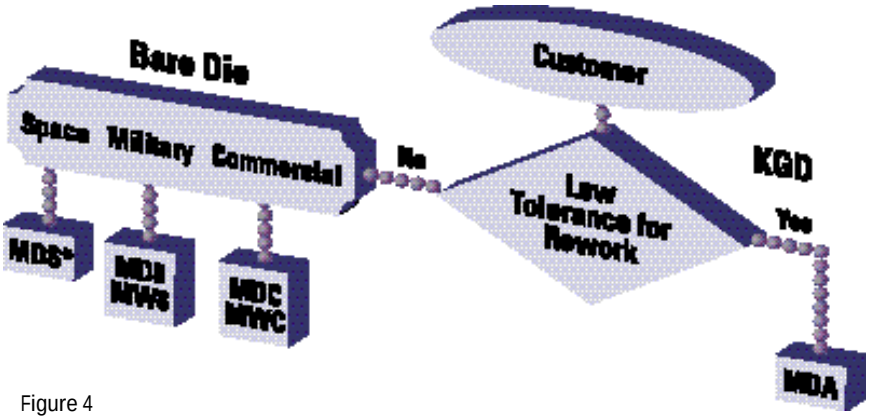


Figure 4

Featured in the next edition of Navigator

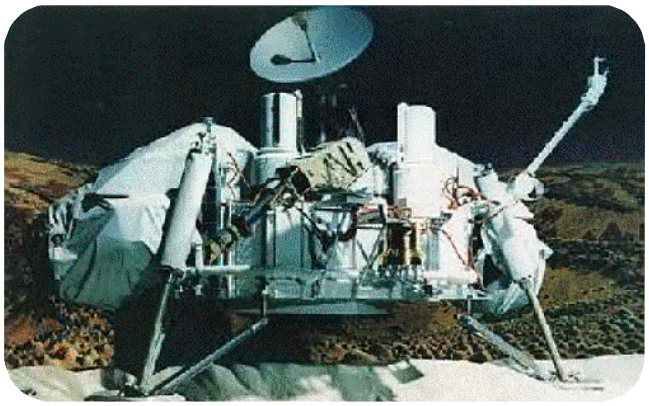
PLLs (Phase Lock Loop)

National Complementary Gallium Arsenide Configurable Logic Array

National Semiconductor is partnering with Systems & Processes Engineering Corp. (SPEC) of Austin, Texas, to jointly develop a Complementary Gallium Arsenide (CGaAs) Configurable Logic Array (CLAy) based on National's patented CLAY10 architecture. This joint development venture couples the design expertise of SPEC with National Semiconductor's leadership role in the Military and Aerospace market. This part is targeted for space applications that require high speed, low power, and good immunity to radiation.

The CLAY10 will be a 32 x 32 fine-grained SRAM-based cell array. This 1024 Cell FPGA will feature 96 configurable user I/O, a maximum of 1024 registers, and an equivalent gate count of 2,000 based on 70% sequential and 30% combinational.

SPEC, a respected research and development corporation, has a multi-technology ASIC design center and Gallium Arsenide library. Using National's existing CLAY10 CMOS architecture, SPEC has designed a CGaAs gate array. The CGaAs process offers very high speed devices with excellent radiation tolerance and low power consumption.



Viking Lander, 1/28/98 image, courtesy NASA

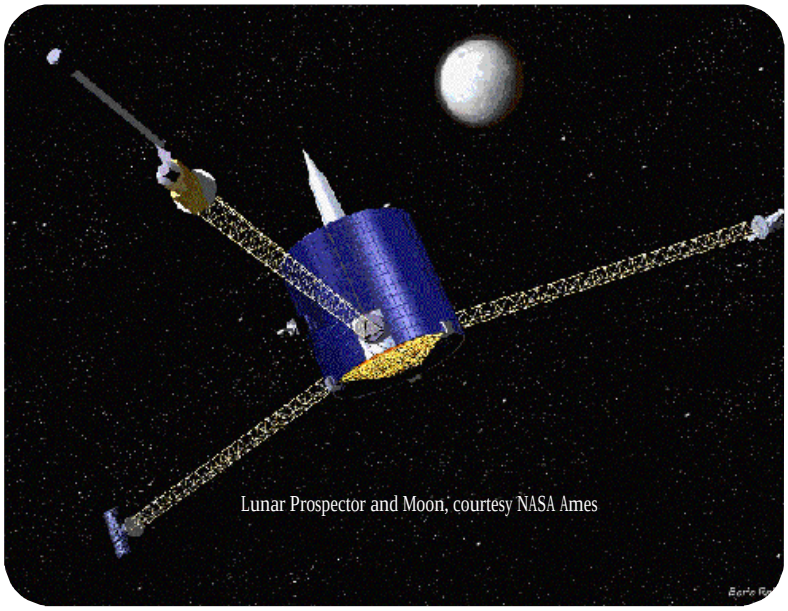
The CLAY10 has been modeled to show system speed of greater than 300MHz with power consumption a fraction of that of low voltage CMOS logic. Power dissipation will be less than 1W. The CLAY10 will be latchup immune, have total dose greater than 1Mrad, and SEU of 30 - 40 LET. The I/O can be configured to support 3.3V TTL and CMOS levels. Packaging will be an industry-standard 132-lead CQFP that is qualified for space applications.

National is targeting this CGaAs Configurable Logic Array toward applications in communication and remote sensing satellites that need the high speed on the front end, with the flexibility of an FPGA. Its high level of radiation tolerance will make this part suitable for the most demanding orbit. Its low power consumption will save on power supplies.

National's software tools are PC compatible and work with industry-standard front-end design software. The development roadmap has first samples available in the third quarter of 1998, and full production in the first quarter of 1999. Following this design will be the CLAY31, a 56 x 56 cell array FPGA; and a 50k gate FPGA based on architecture currently in development by National.

For additional information on National Semiconductor's CGaAs CLAY products, contact Jon Ewald at 207-541-8750 (jon.ewald@nsc.com).

In Europe, contact Paul Wakefield at +49-8141-351492.



Lunar Prospector and Moon, courtesy NASA Ames

AT A GLANCE

New National Literature Includes All Military and Aerospace Products

National's new *Mil/Aero Product Line Card* includes all available Analog, ASIC, Interface, Logic, Memory, and other products. Included are process flow, qualifications, package options, and more.

Also included is information on product/family migration paths. It's a handy tool if your system is in need of upgrades, or should a product obsolescence be pending.

For your copy, please use the attached reply card. Or contact your National sales representative.

Radiation Design Considerations, cont. from page 2

- ❑ Selecting manufacturers with radiation-resistant components

Piece-part testing is one of the more costly efforts when radiation hardening a system. Here each component's radiation response is determined by different radiation environment simulators.

Selecting RHA Components

Once a technology is selected, the next step is to choose RHA components. Use of RHA devices reduces cost, improves reliability, and ensures the system's radiation hardware requirements. RHA component qualification does not guarantee the devices are impervious to adverse radiation effects, but that they have end-point electrical values which account for radiation-effects-generated responses.

If the system's manufacturer determines RHA acceptability via its own radiation testing program, the system's cost will significantly increase. In addition to the system manufacturer's involvement in comprehensive radiation testing, the OEM bears the burden of scheduling and purchasing costly radiation time at test facilities.

A better, less costly method is for OEMs to work with RHA-qualified IC manufacturers. In general, RHA devices are qualified for neutron environment and total dose irradiation, but are not specified for transient (dose rate) environment or single event phenomena.

Concerns associated with RHA components include examining vendor's data for outstanding issues, annealing, lot-to-lot variation, wafer-to-wafer variation, and radiation test conditions. It is important to select a semiconductor manufacturer that provides either the specified data or eliminates a particular concern. By choosing the correct technology and component manufacturer, a radiation-hardened systems can be produced with minimal cost, fewer components, and maximum survivability. The technology of choice to meet these radiation requirements is a CMOS with a thin epitaxial (Epi) layer or silicon-on-

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When Designing with CMOS . . .

- ❑ Do not use NMOS technology, if possible.
- ❑ Use enhanced mode MOSFET design.
- ❑ Use CMOS product with thin gate oxide less than 300Å thick.
- ❑ Use low voltage (power supply) product.
- ❑ Use design margin of 2 or greater.
- ❑ Use CMOS product that does not have the Rebound Effect with the total ionizing dose level to be used.
- ❑ Use circumvention schemes for dose rate and Single Event environments.
- ❑ Use current-limiting resistors when necessary to prevent latchup. This increases power consumption as well as increases propagation time.
- ❑ Use sequential logic that uses circuitry or resistive elements. This increases RC times to prevent upset.
- ❑ Employ CMOS product that uses a low resistivity substrate as well as a very thin, low resistive epi layer.
- ❑ To minimize leakage current of the n-channel and threshold voltage of the p-channel do not use NOR gates. Do use NAND gates.
- ❑ CMOS devices are immune to neutron radiation and offer excellent total dose, transient (dose rate), and single event effects characteristics.

Radiation Design Considerations, cont. from page 6

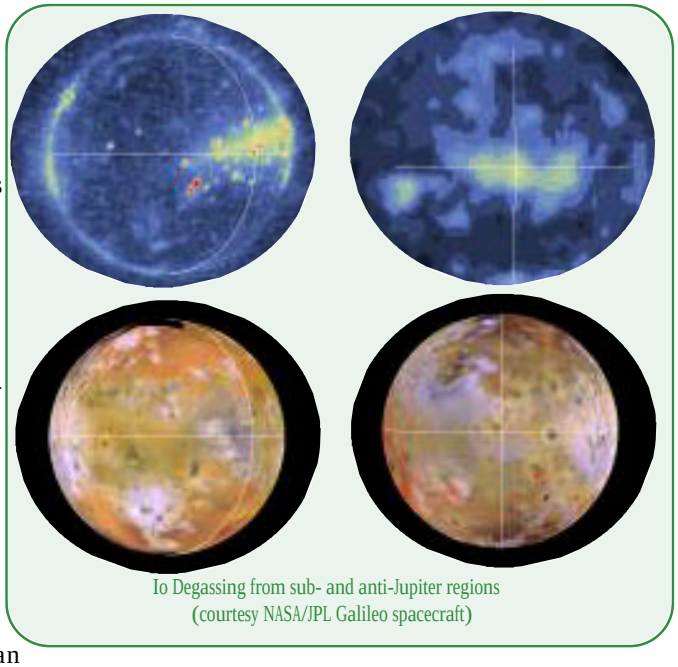
insulator (SOS or SiO_2 process). National's FACT™ logic has been built on thin Epi since 1987.

Ionizing (Total Dose Rate) Radiation & CMOS Devices

Total ionizing dose radiation affects CMOS products in two areas – threshold voltage shifts and radiation-induced leakage current. Damages involve trapping positive charge in the gate and field oxides. A positive trapped charge in the gate oxide causes enhancement mode n-channel MOSFETs to approach depletion while enhancement mode p-channel MOSFETs are driven further into enhancement. Other generated trapped charges (a.k.a., interface states) cause the n-channel MOSFET to increase after having decreased toward depletion operation. This Rebound Effect is a reliability concern for long-term space flight. P-channel MOSFETs are slightly affected by interface states. Trapped-positive charge and interface-state charge generation combine with subsequent annealing effects to constitute Time Dependent Effects (TDE) of total dose ionization.

The two major parametric concerns are leakage currents and propagation times. Depending on a vendor's CMOS processing, other parametrics (such as V_{IL}, V_{IH}, V_{OL}, V_{OH}) may also change.

Design margin is also important in CMOS logic design. It is used if a device function fails to meet or if it exceeds the radiation requirements of a specific application. Design margin is essentially a ratio of total dose radiation failure level of the design versus specified total dose radiation failure level. Design margins are determined by statistical analysis methods and can be applied as device, circuit, or system criteria. For CMOS devices, possessing a design margin greater than 100 requires minimal radiation testing. If the CMOS device's design margin is less than 10, it must have lot acceptance testing and specified controls.



Io Degassing from sub- and anti-Jupiter regions
(courtesy NASA/JPL Galileo spacecraft)

Transient (Dose Rate) Radiation & CMOS Logic Design

Transient irradiation is primarily associated with a nuclear explosion and is a major concern for circuit and system designers of tactical equipment. Dose rate radiation is the amount of total dose irradiation given in specified time intervals.

The affect of the dose rate pulse is generation of excess charge in a short period of time. The quantity of excess charge is dependent on the total ionizing dose used. The concentration of these excess carriers is determined by the dose rate and carrier lifetime. Excess charge results when the ionizing pulse occurs at a faster rate than can be recombined. When a threshold level of excess charge is attained in a CMOS device, these radiation-induced effects can cause temporary effects or catastrophic failures:

- ❏ Upset (soft error)
- ❏ Latchup
- ❏ Junction burn-out

Other effects are short transient pulse on the output and saturated outputs. These depend on the amount of generated photocurrent (excess charge) and output loading.

Since there is no permanent damage, upset of output data is a soft error. Combinatorial circuits will upset, then return to their original state. This type of upset generates a transient voltage at the output pin which might or might not affect the next IC. Sequential logic circuits are the devices which upset and remain in this condition until the affected device is reset.

While logic upset is acceptable for some projects, the dose rate threshold level is important to designers who must work around the upset condition. Latchup occurs when a sufficiently large quantity of radiation-induced photocurrent initiates a parasitic Silicon-Controlled Rectifier (SCR).

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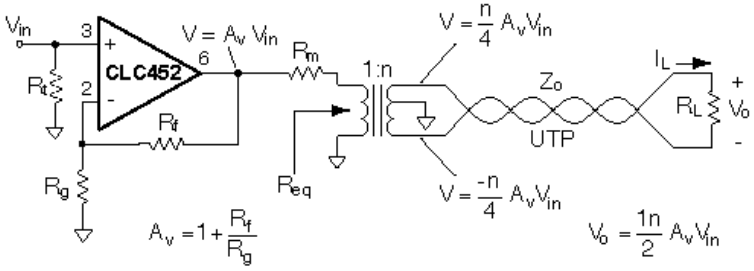
CLC452 for Low-Impedance Loads & Low Power Needs

Now released for military and aerospace applications is National's CLC452, single supply, low power, high output, current feedback amplifier.

The Comlinear CLC452 has a patented output stage that allows it to source up to 100mA and drive a 100Ω load within 1.0V of either supply rail, but consumes minimal quiescent supply current (3.0mA) from a single 5V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels; and has a linear-phase response up to one half of the -3dB frequency.

The superior dynamic performance of the CLC452 features a 130MHz small-signal bandwidth, 400V/µs slew rate, and 4.5ns rise/fall times (2V step). Its combination of low quiescent power, high output current drive, and high-speed performance make the CLC452 ideal for battery-powered personal communication and computing systems.

The ability to drive low-impedance, highly capacitive loads also makes the CLC452 ideal for single-ended cable applications. Low impedance loads can be driven with minimum distortion. A 100W load produces only -75/-74dBc second/third harmonic distortion (Av = +2, V_{out} = 2V pp, f = 1MHz); with a 25W load and the same conditions, only -65/-77dBc second/third harmonic distortion. It is also optimized for driving high currents into single-ended transformers and coils.



The CLC452 as a Twisted Pair Driver

When driving the input of high-resolution A/D converters, the CLC452 provides -78/-85dBc second/third harmonic distortion (Av = +2, V_{out} = 2V pp, f = 1MHz, R_L = 1kW), and fast settling time.

The high output current and low distortion features of the CLC452 also enable it to effectively drive transformers. The figure above illustrates a typical twisted pair driver that uses the CLC452 and a transformer. The transformer provides the signal and its inversion for the twisted pair.

To match the line's characteristic impedance (Z_o) set:

$$R_L = Z_o$$
$$R_m = R_{eq}$$

Where R_{eq} is the transformed value of the load impedance (R_L) and is approximated by:

$$R_{eq} = \frac{R_L}{n^2}$$

Select the transformer so that it loads the line with a value close to Z_o over the desired frequency range. The output impedance (R_o) of the CLC452 varies with frequency and can affect the return loss. The return loss (below) takes into account an ideal transformer and the value of R_o.

$$\text{Return Loss (dB)} \approx -20\log_{10}\left| n^2 \cdot \frac{R_o}{Z_o} \right|$$

The load current (I_L) and voltage (V_o) are related to the maximum output voltage and current of the CLC452 by:

$$|V_o| \le n \cdot V_{max}$$
$$|I_L| \le \frac{V_{max}}{n}$$

The above current relationship concludes that an amplifier with high output drive capability is required.

For more information, visit National at www.national.com. To reserve a copy of the upcoming CLC452 pitch-pack or for answers to other questions, email at shawn.turschak@nsc.com. Or in Europe, contact Paul Wakefield at +49-8141-351492.

Applications for National's CLC452

System	Application	Key Features
Data transmission	Point to point through Twisted Shielded Pairs (TSP)	Low harmonics, high output current
Coax cable drivers	Video line driver for moving map, displays, weapon video	Wide bandwidth, low DG/DP, low power
Digital video	8-10 bit video ADC driver	Low harmonics, low DG/DP
	8-10 bit video DAC buffer	Low harmonics, high speed
Instrumentation	Portable test/measurement	Low power, high speed, low distortion
Communications	High speed modems	Low power; high output current

Radiation Design Considerations, cont. from page 7

Once activated, this SCR acts as a low resistance path between ground and power supply. This usually leads to catastrophic failure, such as blown bond wires or die metalization.

Junction burnout is another catastrophic failure in the dose rate environment. It occurs when sufficiently large photocurrent accumulates in the sensitive junction and cannot be distributed quickly. As a result, thermal energy increases to a level which causes junction burnout. For most technologies, the junction area is fairly large and heat can be dissipated. At very high dose rate levels, junction burnout is a major concern.

Single Event Effects & CMOS Logic Design

Single Event Effects (SEE) are predominantly associated with trapped radiation in space. As technology has evolved to decreased geometries, feature sizes, and gate oxide volume coupled with increased device speed, the energy required for gate switching has also reduced. The result – low energies (less than 0.5 pico joules) can now switch device gates, making SEE-charged particles an important radiation environment.

SEE hardness design is dependent on mission requirements and circuit application of the device. It is affected by orbit placement, time duration in space, and orbit inclination. Single Event Phenomena (SEP) is generated by three charged particles: alpha, protons, and heavy ions.

- ❏ The alpha particle – the weakest of the particles in causing SEE – causes upset in sequential logic or memory devices. Thorium, a radioactive material used in ceramic packages, is a source for alpha particles.
- ❏ High-energy protons originate in the Van Allen Belts or by solar flares. Protons having energy greater than 10MeV cause a single event problem.
- ❏ Heavy ions are caused by solar flares and galactic cosmic rays.

The detrimental results of SEE on electronic systems include transients, soft errors, and permanent damage. Single Event transient spikes are generally associated with combinatorial logic circuits. The transient spike resulting from a Single Event strike has a short time duration, but could contain sufficient energy to cause a subsequent sequential or combinatorial logic input to change. While combinatorial logic outputs have transient upset, the inputs will force the output to its original state. Soft errors are temporary Single Event upsets and are defined as bit flips.

Latchup is the major permanent damage caused by SEP. It and other effects, such as funnel effect, result when a high-energy charged particle passes through a sensitive area and deposits energy along its path. The rate of energy loss in the material is Linear Energy Transfer (LET). This energy loss generates a plasma of electron-hole pairs. If this plasma occurs in a depletion area of the sensitive region, the result is generation of induced current. This induced current is primarily collected from the depletion region and the funnel region.

Induced current is a function of the circuit's parameter, the voltage applied at the sensitive node, and node capacitance. The amount of charge required to generate a change of state in a memory cell or sequential logic device is defined as the critical charge. Associated with the critical charge are the sensitive nodes of an IC. Sensitive nodes are the reversed-biased nodes, e.g., the OFF drains of the p- and n-channels of a memory cell. The collected charge at these sensitive nodes causes a voltage transient to develop and be applied to other cross-coupled inverters of the memory cell or sequential logic device that generates the change of state at the output of the device.

Latchup in the Single Event Effects environment can affect devices manufactured on CMOS, bipolar, and ECL processes. Because of heavy ions, latchup in CMOS technologies is generally associated with a bulk technology or with devices fabricated on a thick Epi substrate. While similar to Transient (Dose Rate), SEE latchup is generated by heavy ions. Since SEE latchup usually has catastrophic results, designers must select components that will be impervious to a single particle strike, e.g., devices which are fabricated with guard rings, built on a very thin EPI, or that use dielectrically-isolated CMOS technologies (SOS, SOI). National's FACT product is manufactured on a very thin epitaxial layer. At extremely high LET levels, FACT remains immune to latchup from heavy ions.

Designing with Linear Bipolar Products

In the past, the major radiation concerns for linear bipolar product

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Radiation Design Considerations, cont. from page 9

came from environments where neutron and dose rate were issues. The effect of neutron irradiation on linear bipolar basically affects ß (DC gain), drive current (fan-out), and V_{CE} (sat). There was little concern with total dose and Single Event Effects (SEE).

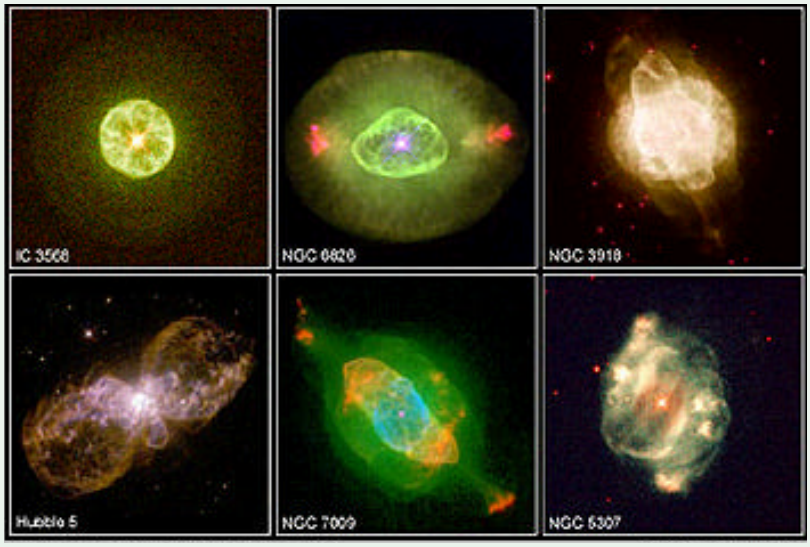
Recently, it has been noted that linear bipolar devices show total dose sensitivity to low dose rate. This is known as the Enhanced Low Dose Rate (ELDR) Effect.

In the Single Event Phenomena (SEP) environment, Single Event Transient (SET) and Single Event Burn-Out (SEB) are of greatest concern for linear bipolar devices.

The hardening of bipolar circuitry generally results by implementing geometrical considerations as well as adding current sources and resistors to accommodate different radiation environments. Some radiation hardening can be acquired through a set of radiation hardening design rules. Avoiding certain design techniques (i.e., serpentine resistors), minimizing the use of lateral and vertical PNP transistors in the device design, and avoiding Darlington circuit design. Additional parameters that affect bipolar performance and lead to radiation-induced failure are Early Voltage (VA) changes, input impedance, and output impedance. All result in a degraded device that has reduced output drive current and increased load sensitivity.

Low Dose Rate Sensitivity & Bipolar Linear Design

In the past, high dose rate irradiation was used on all bipolar product to simulate the total dose environment. As with CMOS technology, this was revered as the worst-case scenario. We now know it is low dose rate that is the worst-case condition, and can degrade a linear bipolar device by a factor of 2x to 10x for a particular parameter.



Hubble's Planetary Nebula Gallery (courtesy NASA)

This makes Enhanced Low Dose Rate Effect a major concern for space system designers who use linear bipolar product. To complicate the situation, the ELDR effect does not affect all linear bipolar products or fabrication processes – old or new. While op amps and comparators are apt to be most affected, all bipolar devices under consideration for use in space system design should be evaluated for low dose rate degradation.

Two failure mechanisms can occur simultaneously in the low dose rate environment of space [less than 1 rad(Si)/s]:

- ❏ Time-Dependent Effects (TDE)
- ❏ True Dose Rate Effect

TDE continues long after the linear part is removed from the environment. For example, a satellite that passes in and out of the Van Allen Belt is subject to TDE. However, the True Dose Rate Effect only exists while the device/system is within the low dose rate environment. Both failure mechanisms contribute to the degradation of linear bipolar parameters.

Because the ELDR effect is relatively new in the radiation environment, it is difficult to simulate these effects without fully understanding the mechanisms that cause them. New approaches to simulation are in various stages of development.

To observe the TDE mechanism, MIL-STD-883E Method 1019.5 can be applied using the +100˚C, 168-hour post-irradiation anneal section for bipolar parts. For the True Dose Rate effect, a proposed method is included in the new ASTM document, *Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices.* Total ionizing dose irradiation allows three options:

- ❏ Irradiate at the intended dose rate
- ❏ Perform the accelerated test method as described in the

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Radiation Design Considerations, cont. from page 10

document. This approach is used when it is impractical to irradiate and test within a reasonable time.

- ❑ Perform irradiation using one of two methods:
  1. Irradiate at room temperature low dose rate and apply a design margin factor of 2.
  2. Irradiate at +100˚C, employing a dose rate between 1 rad(Si)/s and 10 rad(Si)/s, then apply a design margin factor of 3.

National Semiconductor is investigating the use of Method 2 of the third option.

Shielding

Sometimes the product that you need just isn't available with inherent radiation resistance. This is where shielding is a consideration.

Shielding to protect integrated circuits from radiation environments has long been used in the military and aerospace industries. Over the years, shielding has developed into a science, replete with the latest simulation design tools and techniques. Beginning with a single layer material, shielding has evolved into multiple layers of high Z and low Z materials that are integrated into IC packages. Perhaps even more important than the type of material used is understanding the radiation environments to which the integrated circuits will be exposed. Today's radiation hardness design techniques enable system designers to use shielding as the last resort. It is only justified when circuit redesign is not possible, a radiation harder part is not available, or the radiation design margin is at its minimal limit.

Typical Shielding Evaluation Process

1. Evaluate the radiation environments
   - ❑ Electron
   - ❑ Proton
   - ❑ Neutron
   - ❑ Photon
   - ❑ Cosmic rays
2. Determine the radiation requirements
3. Identify the components, sub-assemblies or assemblies of each sub-system or system that does not meet the radiation design margin or acceptable radiation levels
4. Determine the radiation environment within the satellite or LRU (Line Replaceable Unit) through radiation analysis or modeling codes
5. Can inherent shielding within the satellite or LRU be used? Or is local shielding at the sensitive sub-assembly or part type needed?
6. If shielding is required, then determine the shield configuration and mass needed. Determination is based upon the remaining radiation environment.

Shielding is employed in military systems, space satellites, and the nuclear commercial business. Each application has unique shielding requirements and associated costs. The purpose of shielding is to reduce radiation degradation to an acceptable level based upon the application, safety issues, survivability needs, and radiation design margins. Shielding analysis begins by evaluating the need for shielding as based upon radiation environments, design margins, and restrictions. Once shielding needs are identified, the next step is to evaluate the available (inherent) shielding of the application's environment as well as additional local shielding, either on-board or at the part level.

Shielding is easiest with stationary ground facilities (i.e., nuclear power plants) where earth, cement, and lead can be used readily and the predominant limiting factor is cost. Mobile military systems are the next-to-the-hardest to design for shielding. This is where weight, size, and cost are restricting factors — particularly those systems that will be directly exposed to nuclear blast or must operate through the radiation environment. Space systems present the greatest obstacles for shielding. Here, weight is critical, service life is greater than 5 years, there is no available maintenance to replace failed systems, and size limitations are essential.

Since fixed military ground installations and commercial radiation sources can be shielded with readily available material, this discussion focuses on mobile military and space systems. Please note that at this time there is no practical method to shield systems from gamma rays or neutrons due to the mass of shielding material that would be required.

To provide insight to the design of the shield configuration, radiation analysis for shielding must include all transport codes for elec-

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Radiation Test Reports on the Web

Available on the Web are a number of National's radiation test reports for download in Portable Document Format (PDF). Point your browser to http://www.national.com/mil and click on the National Semiconductor's Radiation Home Page link to find total dose radiation test results. Included are Analog products such as the new high speed, high output current, LM7171 voltage feedback amplifier to the trusty LM117 3-terminal adjustable voltage regulator. Test information for National's Logic, Interface, and other products will be added at a later date.

The table (right) is an excerpt from the LM7171 radiation report and presents characteristics of twelve parameters for the LM7171J. It concentrates on the parameters that were tested with ±5V supply. All 15V supply parameters were tested, but only two (Input Offset voltage and current) are presented in this report. That data is available upon request. Since only DC parameters were tested, AC parameters (Slew Rate and Gain-Bandwidth) are not a part of this report. Data shows that all parameters remained inside the MDS sub group 1 limits throughout the test. Comparison of pre-rad and post 200krad data shows that overall changes in the parameter values were minimal, and all devices were functional after 200k rad exposure. The table shows a summary of average changes after 200krad exposure for each of the twelve parameters presented in this report.

Parameter	Avg Post 200k Change
Supply Current	-0.52mA
Input Offset Voltage	-0.111mV
Positive Input Bias Current	-0.146uA
Negative Input Bias Current	0.241uA
Input Offset Current	0.093uA
CMRR (V_{CM} = +/-2.5V)	-3.7dB
Positive Output Swing	-0.042V
Negative Output Swing	0.042V
PSRR (V_S = +/-15V to +/-5V)	0.485dB
Voltage Gain	-0.307 dB
Input Offset Voltage (V = +/-15V)	-2.975mV
Input Offset Current (V = +/-15V)	0.093uA

Also on this site is a radiation testing procedures document that describes how the tests were performed. Additional links on this site provide access to National's *Technologies for Space* brochure as well as links to Defense Supply Center Columbus (DSCC), Space News, *Aviation Week & Space Technology*, and ICS Radiation Technologies Inc.

Total dose radiation tests are designed to characterize changes in device performance due to total dose radiation. They are intended to give designers an idea as to how the devices will perform in a radiation environment – a starting point in the selection process. These tests are not intended to classify maximum radiation tolerance of any particular device; rather, to show trends in the critical parameters as a function of total dose. The reported results are representative of the lot tested in the specific sample and should not be used as generic RHA qualification data. National Semiconductor uses different process flows for different product qualification levels, and only guarantees RHA performance when National Semiconductor has tested and certified the specific manufacturing lot.

For additional information, please email to milmktg@nsc.com.

PURCHASING CORNER

National Can Provide Replacements for Monitored Line Products

The space IC-using community was recently surprised by the USAF announcement that the respected Monitored Line Program was terminated with only a one-day lifetime buy window.

But for those that still need the products previously offered by the Monitored Line at VLSI Packaging, there is good news. Because VLSI Packaging used National Semiconductor's die, these products are now available directly from National with the same footprint, electrical performance, and radiation resistance. This is the same die that National uses in its standard space-level flows: QMLV SMDs, JAN S Slash Sheets, and National's internal space flow "-MLS" (Microcircuit Line for Space).

Space-Level Process Flows

- ❑ JAN Class S
- ❑ JAN Class S "R"
- ❑ QMLV MIL-PRF-38535)
- ❑ MLS (Microcircuit Line for Space)
- ❑ JAN Class B "R"
- ❑ SMD (Standard Microcircuit Drawing)
- ❑ SCD (Source Controlled Drawing)

QML V and JAN S QPL Space-Level Data Package

National Semiconductor provides the following data for space-level orders.

At no charge

- ❑ Cover sheet (includes National Semiconductor ID, lot number, customer name, sales order number, purchase order number, wafer lot number, serial number range, part marking layout)
- ❑ Certificate of Conformance

At optional cost

- ❑ Full process attributes
- ❑ Wafer Lot Acceptance (WLA) report
- ❑ Scanning Electron Microscopy (SEM) report
- ❑ Groups A, B, and D attributes
- ❑ SEM photographs
- ❑ X-ray report
- ❑ X-ray films
- ❑ Read & Record data

National has been a Monitored Line supplier for over 20 years. The major differences between National's standard flows and the Monitored Line flow are:

1. National's QMLV-registered facility does not use the extensive third-party monitoring previously available from Lockheed.
2. Some Monitored Line drawings have unique electrical test or burn-in requirements which National no longer supports.

Product Families Available from National with Space-Level Flows

Logic Products

- ❑ CMOS Logic
  - FACT™ (AC/ACT)
  - FACT Quiet Series™ (ACQ/ACTQ)
  - FACT FCT (FCT)
- ❑ BiCMOS Logic
  - ABT
- ❑ Bipolar Logic
  - FAST™
  - Low Power Schottky
  - TTL
  - L (Low Power TTL)
- ❑ ECL Logic
  - F100K 300 Series ECL
- ❑ SCAN (Serial Controlled Access Network)

Advanced Systems & Interface Products

- ❑ Transmission Line Drivers/Receivers
- ❑ Bus Transceivers
- ❑ Memory Support

Analog Products

- ❑ Operational Amplifiers
  - VIP™ (Vertically Integrated PNP) Op Amps
  - Bipolar Op Amps
  - CMOS Op Amps
- ❑ Buffers
- ❑ Comparators
- ❑ Power Management
- ❑ Data Acquisition
- ❑ Comlinear Analog Products
  - Operational Amplifiers
  - Data Converters

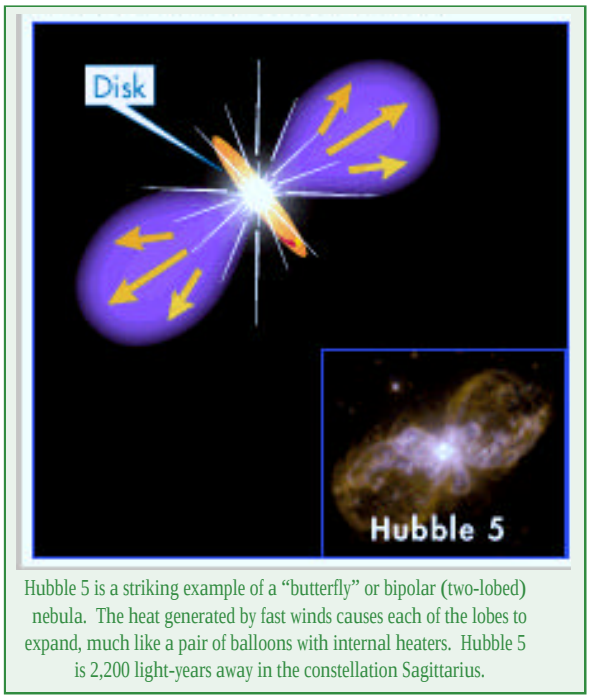
For more information, contact your National sales representative. Or contact Dave Allen at 408-721-4018 (david.allen@nsc.com).

In Europe, contact Paul Wakefield at +49-8141-351492.

Radiation Design Considerations, cont. from page 11

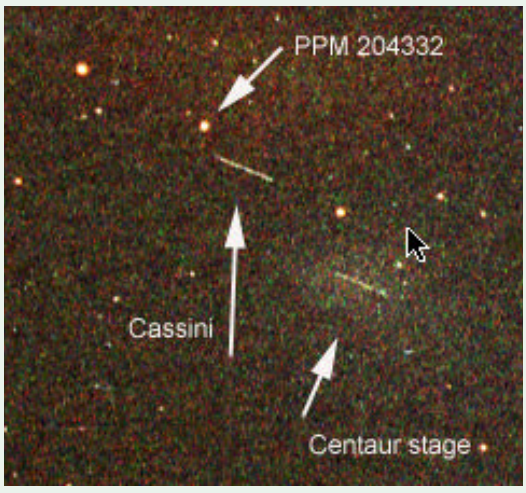
tron and proton environments. Another key consideration is knowing what materials are located between the radiation-sensitive IC and the radiation environment. It may be possible to use these materials as a part of the shielding. This approach can be combined with the possibility of relocating the part, board, or assembly to another position of the spacecraft or aircraft. If these evaluations fail to provide the required minimal radiation level, a determination may be made to use local shielding for a sensitive part and its configuration. Or the answer may be for a general mass shielding to be applied to the system or LRU.

Recent investigations show multi-layer shielding is very effective, particularly with the electron and proton environments of space. For example, a tri-layer shield configuration can significantly reduce radiation degradation. A shield configuration consisting of a high Z material sandwiched between two layers of low Z material will reduce the electron and proton radiation significantly. Thin layers of shielding will have a small effect of reducing cosmic ray low energy spectrum component. The high Z material shields against the penetrating electrons while the low Z material facing the part-type or system electronics shields against the proton environment. The first layer of low Z material could be part of the system's chassis cover or the surface of the spacecraft or aircraft.



Hubble 5 is a striking example of a "butterfly" or bipolar (two-lobed) nebula. The heat generated by fast winds causes each of the lobes to expand, much like a pair of balloons with internal heaters. Hubble 5 is 2,200 light-years away in the constellation Sagittarius.

Another option to shield radiation-sensitive part is to use a special package that employs the multi-layer shield concept. This shielded package is applicable for the electron and proton environments, but does not stop the effects of gamma or cosmic rays (heavy ions). These packages are costly and trade-offs are required.



Cassini and the Centaur booster stage at a range of approximately 39000km. Taken October 15, 1997, shortly after the end of the blowdown of unused fuel from the Centaur.

Questions?

While not all inclusive, this article provides a basic understanding. Most importantly, wherever possible, select vendors that have radiation-tolerant/radiation hard product and use the QML approach. This will provide a standardized product, a consistently reliable product base, cost-effectiveness, and diverse product selection.

Integrated circuit technology changes about every 1 1/2 to 2 years. With the decrease in feature sizes and the frequent changes in processing, it is necessary to stay in tune with the industry. Radiation damage is not going away with new technology advancements. In fact, in some aspects it may worsen. More testing needs to be done in the proton environment as well as the neutron upset arena.

For additional information, visit National's web site at www.national.com/mil.

Or contact Mike Maher at 207-541-8391 mike.maher@nsc.com).

In Europe, contact Paul Wakefield at +49-8141-351492.

To be available by mid-1998 – National's new *Owner's Manual for Radiation Products & Services.*

To "Ask Jackie" use the attached reply card, fax "Ask Jackie" at 207-541-6140, or EMAIL jacqueline.l.collard @nsc.com. Because of space, all comments may not be addressed in the column; but we will provide you with an answer.

Q. *I thought that Logic products were sold along with Fairchild. Yet National is still promoting Logic. Can you explain?*
anonymous

A. National Semiconductor sold its commercial commodity Logic, Discrete, and Memory products to Fairchild Semiconductor. This is enabling National to focus on its core product lines.

National retained its Mil/Aero products and the infrastructure to support these products, including the hermetic logic business. Servicing the Military and Aerospace market requires specialized skills and competencies which National's Military/Aerospace division proudly provides.

The die for National's Mil/Aero products are produced in Fairchild fabs – the same fabs that produced these die prior to divestiture. You could say that we have always been a customer of sorts, since we bought die from them for manufacturing in hermetic packages.

Today we continue this relationship with a long-term agreement for Fairchild to provide National with uncompromised die for our continue support of our Mil/Aero customers.

Q. *My company is contemplating taking 883 products and upscaling to a space-level flow. Would you comment on this upscreening practice?*
anonymous

A. National Semiconductor is aware that some customers may be "upscreening" or "retesting" semiconductor components. This upscreening can be potentially dangerous to the end user. Using components in applications or environments for which they were not intended can lead to component or system failure. For example, products specified to operate in office environments should not be expected to function properly or reliably in an application which is subjected to more extreme conditions.

National offers a wide variety of COTS (Commercial Off the Shelf) component solutions designed to meet today's numerous application and environmental conditions. These COTS products are designed and manufactured to perform reliably in applications ranging from office desktop PCs to radiation-sensitive satellites. We strongly encourage component users to work closely with their suppliers and demand devices that are specifically designed and tested for use in the intended application and environment.

Work closely with suppliers and demand devices that are specifically designed and tested for use in the intended application and environment.

In specific regard to National Semiconductor, our products are designed to be used only within the electrical and environmental limits published in their respective datasheets. National does not authorize the use of any of its products beyond these published datasheet limits. Electrical and/or environmental testing of parts after shipment from National may cause damage or result in latent reliability problems. Such electrical and/or environmental testing or use of National products outside of the published datasheet limits voids all National warranties. National will not be responsible for any component or system failure due to the inappropriate use of its products.

Should you have additional questions or comments, please contact with your National representative.

National Semiconductor®

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