National Semiconductor

Customizable Solutions – ASIC

Customizable Solutions – ASIC Table of Contents

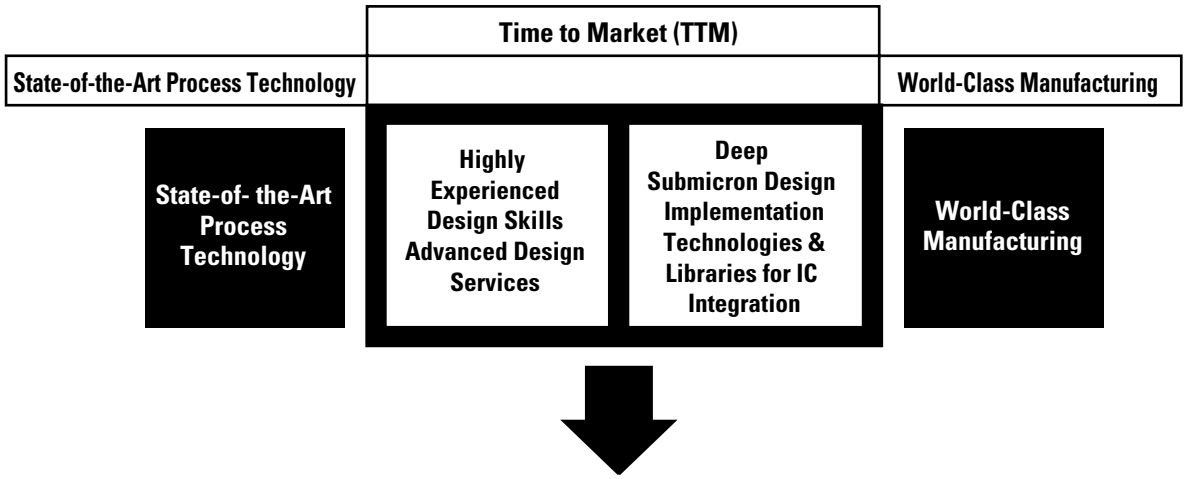
National Semiconductor offers customizable "systems-on-a-chip" solutions to all process flows and extensive packaging options. A unique competency-based alliance with Cadence Design Systems and Aspec Technology ensures complete design and manufacturing support.

Customizable Solutions – ASIC (cont.)

Customizable "Systems-on-a-Chip" Solutions

Today's world requires that data, voice, and video information be provided fast. Processing this multimedia information requires high throughput and high bandwidth in order to deliver global and affordable solutions to military, aerospace, consumer, telecommunications, Internet appliances, industrial control solutions, and client server markets.

National Semiconductor can help with customizable "systems-on-a-chip" design solutions that support your needs for short time to market, state-of-the-art process technology, and world-class manufacturing.

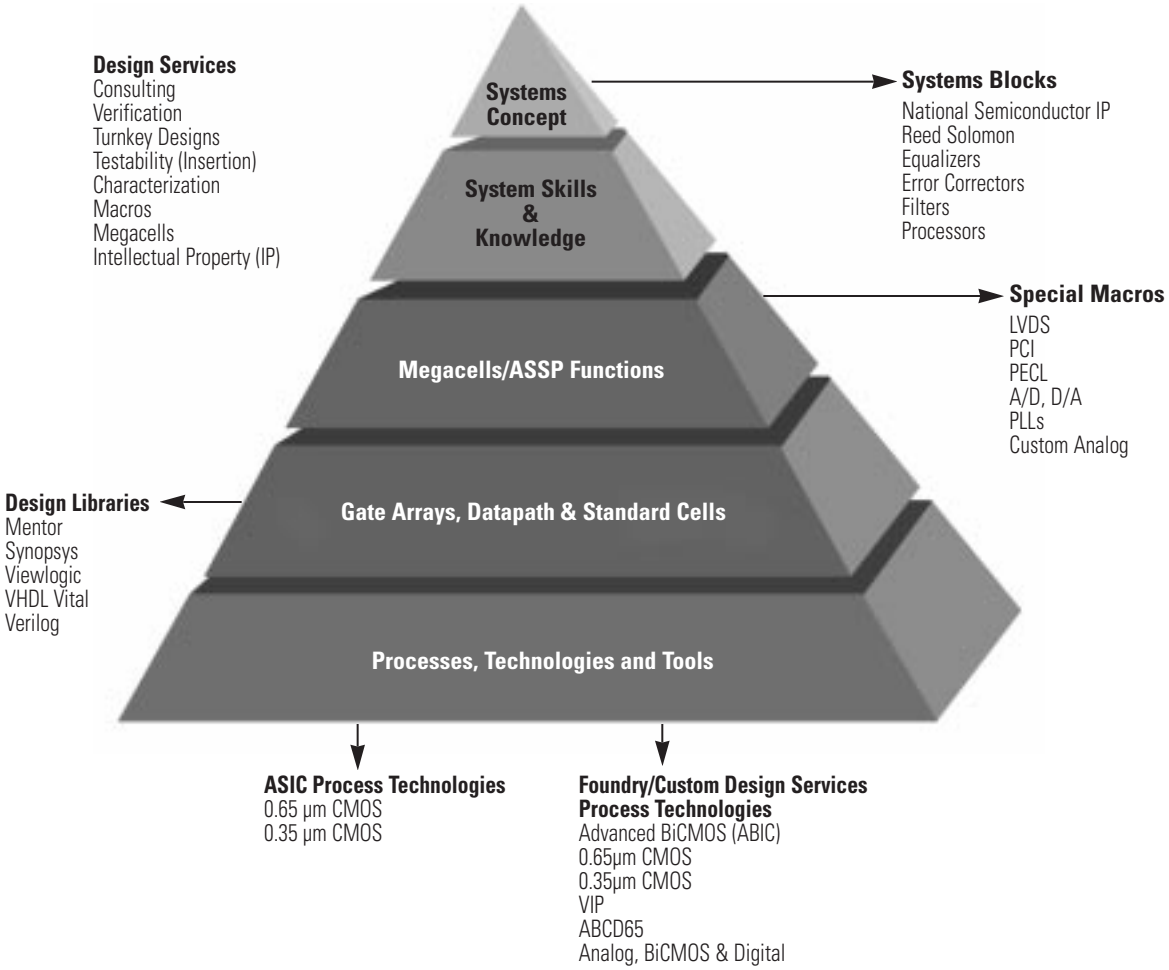


Supporting your diversity of needs, National has developed a unique competency-based alliance with Cadence Design Systems and Aspec Technology to afford you with the best resources for state-of-the-art advanced high-performance CMOS design and design services. At your discretion, functions can include anything from full custom design, to transistor-by-transistor, to complete ASIC design services. You take full control. Your GDS II database tape is backed by National's world-class manufacturing facilities.

If your deep sub-micron design requires intricate timing controls due to skews or simultaneous switching propagated across chip, engineering services are available to you. If clock tree insertion or testability is required and that's not your skill, let National help. We offer a wide range of design services to help you meet your design objectives. We can partner with you and provide services that fill the voids in your design skill portfolio.

Commercial, industrial, and military process flows are available to support your specific needs. Also available is one of the richest industry-standard packaging portfolios. This includes advanced packaging such as LTCC (Low Temperature Co-Fired Ceramic) for wireless systems design as well as high power, high pin count, ball grid array package technologies.

Top Down Design Methodology



Systems-on-a-chip requires a starting point for forward integration. At National, we are proud of our analog heritage and our leadership in mixed-signal design. The man/machine interface is real-world and that means an analog and mixed-signal capability.

Customized Support for Military/Aerospace Applications

Design Conversions for alternate sourcing (Form, Fit, Function)
Design Services
Analog/Mixed Signal and Custom Design
Design For Test (DFT)

- Scan Insertion
- JTAG IEEE 1149.1
  - ▲ TAP Controller
  - ▲ Input/Output Macros
- LSSD
- Parallel Access Testing Technique
- Compatible with National's SCAN products

Value-Added Foundry Services

- Major process technologies available
  - ▲ Advanced CMOS
  - ▲ Analog
  - ▲ Advanced BiCMOS (Ft>14GHz)
  - ▲ Bipolar

Industry-standard packaging – Where permitted meets the full MIL-PRF-38535 requirements for Qualified Manufacturing Lines (QML):

- Ceramic
- Ceramic Quad Flatpak
- Ceramic Pin Grid Arrays
- Ceramic Ball Grid Arrays
- Plastic (TQFP, PQFP, MQUAD, SBGA/BGA, PGA, MQFP)

Process flow options

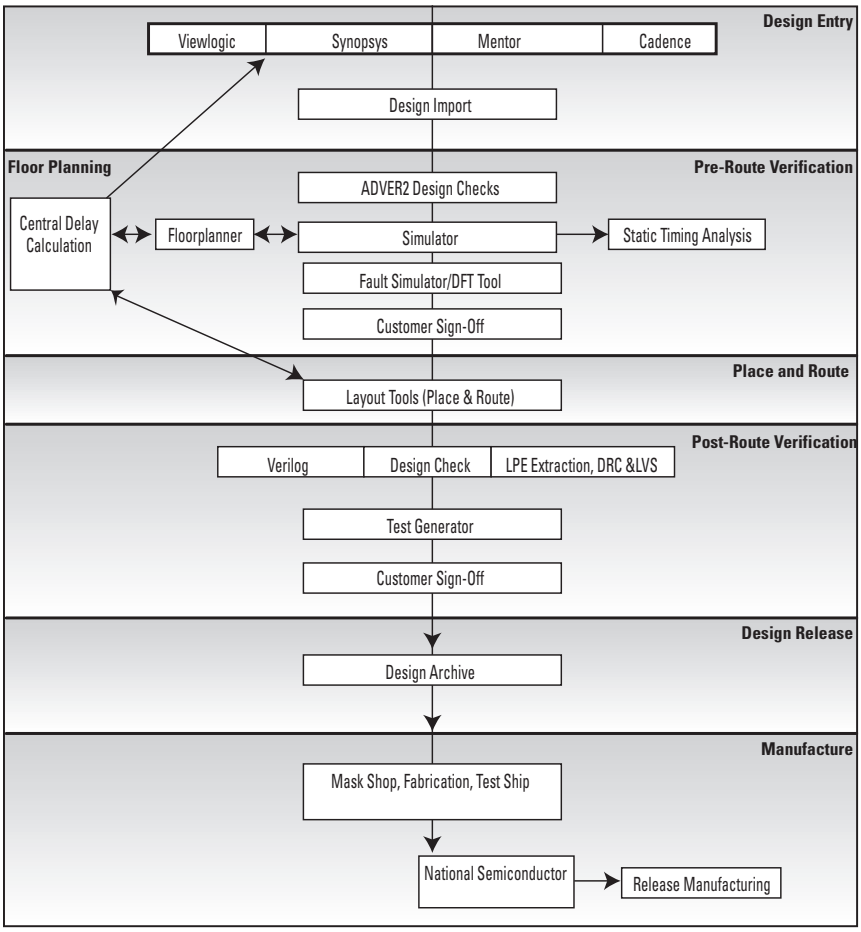
- Commercial
- Industrial
- Military

Additional manufacturing services

- Known Good Die (KGD)
- Special Testing
- Characterization

ASIC Design Methodology

- Right the first time
- Step-by-step procedure
- Retargetability



National Semiconductor's competency-based alliance with Aspec Technology provides Design Implementation Technology (DIT) that is tuned for the rigors of deep submicron design. Additionally there are the benefits of retargetability and portability which minimize the effects of process obsolescence.

National's Design Methodology supports the tools used by our customers. Not being bound by proprietary tools, we provide front-end design kits that support our customer's tool suite. This includes symbols and simulation models as well as synthesis and HDL Libraries that include Verilog and VHDL for both National's standard cell and gate array high density libraries. Additionally, National provides libraries for design-for-test tools as well as floorplanners – critical when high speed deep submicron designs require minimum timing skews.

ADVER™ (ASPEC Design Verifier) software is the primary communication link between the customer and National. Calculating the necessary pre- and post-layout delays from National's performance database, timing values are used for back annotation into design simulations. Simulations take into account interconnect, worst-case temperature, voltage, and process. This ensures first-time working silicon. This software's timing accuracy is portable across workstation platforms and simulators, making any simulator a "golden" simulator.

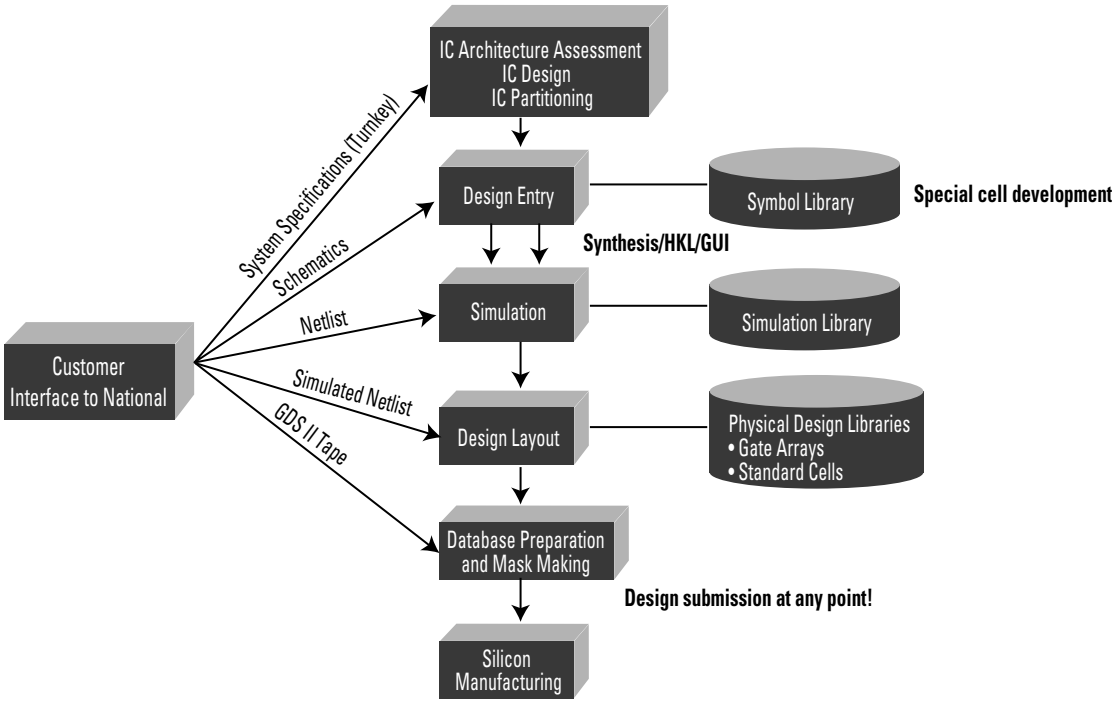
Design Kits

The table on the right is a sample of the design kits available from National Semiconductor for both our 0.65µm and 0.35µm CMOS Libraries. Contact our Sales Representative about your design flow, if your requirements are not listed.

Development Tool	Vendor Supported
Behavioral	VHDL Vital (Model Tech, Mentor, etc.)
	Synopsys Vss
	Verilog
Synthesis	Synopsys
Floor Planning	Cadence HLD
Symbol, Logic, Timing	Cadence
	Viewlogic
	Mentor
Delay Calculation	ADVER
Static Timing Analysis	Synopsys
	Motive
	Pearl
Place and Route	Cadence Cell3
	• Libraries developed by Aspec Technology

Design Services

National can accept your design anywhere in the design flow.



National Semiconductor

- Leader in Military and Aerospace semiconductors
- State-of-the-art process technology provider
- World-class manufacturer
- Fully compliant Quality and Reliability Programs

Cadence Design Systems

- EDA leader
- Full suite of design services
- Multiple design centers

Aspec Technology

- Leader in Design Implementation Technology (DIT)
- Technology library leader
- High density ASIC architecture for Gate Array standard cells

National Semiconductor's alliance with Cadence Design Systems provides the ultimate in design resources. Cadence supports the design aspect from its design factory headquartered in San Diego, California.

National has a long history of providing military customers with state-of-the-art technology and manufacturing. This is now coupled with Cadence's vast knowledge and skills in EDA and world-wide network for design services. These capabilities further combine with National's Intellectual Property (IP) to provide our customers with the broadest, most advanced design capability dedicated to the military and aerospace communities.

Services include:

- Turnkey designs
- Characterization
- Design for Test (DFT)
- Custom design (Analog & Mixed Signal)
- Macro/Megacell development
- Reliability analysis
- Debug and Failure Analysis

ASIC Product Families

SCX065 Gate Array Family Features

- Compatible libraries
- Over 700,000 raw gates
- Over 2,400 I/O buffer combinations
- Special I/O available: GTL, PECL, SCSI, PCI
- 5.0V, 3.3V, and mixed 5V/3.3V or lower voltages
- Supports the major third party tools and vendors
- ADVER™ Central Delay Calculator/Design Verifier
- Design for Testability (DFT)
  - JTAG Boundary Scan (IEEE1149.1)
- Megacell functions
  - TMS320C50,80C51, Analog, etc.

Preliminary SCL035 Standard Cell Family Features

- Compatible libraries
- Over 1.5 million gates
- Over 2,400 I/O buffer combinations
- Special I/O available: GTL, PECL, SCSI, PCI
- 5.0V, 3.3V, and mixed 5V/3.3V or lower voltages
- Supports the major third party tools and vendors
- ADVER Central Delay Calculator/Design Verifier
- Design for Testability (DFT)
  - JTAG Boundary Scan (IEEE1149.1)
- Megacell functions
  - TMS320C50,80C51, Analog, etc.

Gate Array Masterslice Listing

Device	Array Name	Total Gates DLM	Useable Gates TLM	Useable Gates	Max I/O Pads
1	MG6B	6,439	2,898	4,636	48
2	MG6C	11,781	5,301	8,482	64
3	MG6E	18,960	8,532	13,651	80
4	MG6F	25,482	11,212	17,939	92
5	MG6G	30,098	13,243	21,189	100
6	MG6H	41,064	17,658	28,252	116
7	MG6J	50,435	21,687	34,699	128
8	MG6K	64,380	27,683	44,293	144
9	MG6L	79,860	33,541	53,666	160
10	MG6M	97,188	38,875	62,200	176
11	MG6N	115,434	45,019	72,031	192
12	MG6P	136,095	51,716	82,746	208
13	MG6R	170,387	63,043	100,869	232
14	MG6S	220,844	79,504	127,206	264
15	MG6T	278,740	97,559	156,094	296
16	MG6U	343,368	116,745	186,792	328
17	MG6W	433,152	142,940	228,704	368
18	MG6X	533,352	170,673	273,076	408

Packaging

Sampling of Available Packaging

Package Type	Lead Count
Ceramic DIP	24, 28, 40, 48
Ceramic Quad Flatpaks	44, 68, 84, 128, 132, 144, 152, 172, 196, 256
Ceramic Pin Grid Arrays	68, 84, 124, 144, 155, 180, 224
Ceramic Ball Grid Arrays	Consult National CBU; industry-standard pin counts available
Plastic – TQFP, PQFP, MQUAD, SBGA/BGA, PGA, MQFP	Consult National CBU; industry-standard pin counts available