Non-Contact Test Access for Surface Mount Technology IEEE 1149.1-1990

National Semiconductor
Application Note 891
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June 1993

ABSTRACT

Mechanical and chemical process challenges initially limited acceptance of surface mount technology (SMT). As those challenges have been overcome, another obstacle has become apparent: electronic test access. Through-hole components on a 100 mil grid allowed physical aceess. SMT which has provided new levels of packing density has also denied physical test access. To overcome this challenge, the Institute of Electrical and Electronics Engineers (IEEE) has sponsored a new standard, IEEE 1149.1-1990, the Standard Test Access Port and Boundary-Scan Architecture.

THE SMT ASSEMBLY CHALLENGE

The use of SMT has required the refinement of several technologies including: photolithographic improvements in printed circuit etching, computer aided layout to support routing the large number of interconnects, and soldering to allow devices to be attached to first one and then the reverse side of the printed wiring board (PWB) without through-hole mechanical capture.

Equipment to pick and place fragile SMT components with adequate alignment to the prepared pad area was needed to assure high yield assembly. Optical alignment systems replaced the open loop equipment used to assemble boards with dual-in-line packages. The technology has matured. SMT has gained wide acceptance.

TRADITIONAL DEFECT DETECTION, DEFECT ISOLATION

A high yield assembly process, always a target, is important for SMT printed circuit cards because it can be difficult to isolate faults. There is risk of assembly damage during repair. If an incorrect diagnosis results in an unnecessary repair, not only are repair costs higher than necessary, but the risk of damage increases.

Bed-of-Nails test fixtures such as shown in *Figure 1* have provided test access for over twenty years. These fixtures have at least one test probe per IC pin to provide access for printed circuit continuity checking. Low voltage PWB interconnect continuity tests are usually run before applying full power to the PWB. Each connection point on each network is checked for continuity to all expected connections. In addition, by forcing a sequence of bits onto each output pin with the bed-of-nails and then reading the signal received on every other net, it is possible to detect nets that are shorted together and often to tell which two nets are shorted.

Once interconnection defects have been isolated and repaired, it has been common practice to use the bed-of-nails to drive each net of the fully powered board to test each integrated circuit on the assembly. For very simple ICs such test patterns were readily developed. A few microseconds were often adequate to determine that a simple IC was functioning correctly. During these functional tests, the electrical connection of the IC to the printed circuit board was checked as an integral side effect of the test.

Paper first published at Surface Mount International, 1992.

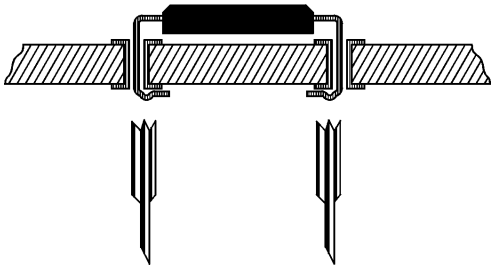

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FIGURE 1. Traditional Bed-of-Nails PCB Test Access Method, Now Challenged by Shrinking Physical Contact Possibilities

Forcing a net with a bed-of-nails contact often required backdriving an IC's output. It might be necessary to force several hundred milliamperes into an IC's output to force a network to the opposite logic level. Backdriving IC outputs does not improve component lifetime. As IC complexity has grown, it has taken more test vectors and therefore required more time backdriving IC outputs.

As SMT allowed packing density to grow, printed circuit layout software began to appear with features that allowed physical access to continue with traditional bed-of-nails testing. *Figure 2* shows a portion of a layout that supports continued access. While supporting test access to allow defects to be detected, this defeated the advantage of SMT: higher packaging density. In addition, layout software became more complex as it was used to help overcome access problems.

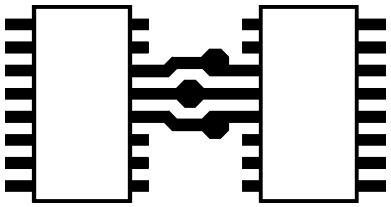

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FIGURE 2. Despite Shrinking Component Sizes, Some Users Have Kept Large Feature-Sized Etch to Continue to Support Physical Access

To support physical access some manufactures began using bed-of-nails fixtures that could contact both sides of a PWB. One user, in a personal communication, reported that these fixtures were so fragile that they might need to be repaired after testing as few as ten SMT printed circuit cards. And the time to develop such fixtures often extended beyond system development time and delayed the start of high volume production. Some users have reported that developing an SMT bed-of-nails fixture added 10% to their board development cost.

IEEE BOUNDARY-SCAN TEST ACCESS

IEEE 1149.1 was defined to replace the test access provided by a bed-of-nails test fixture. *Figure 3* shows an idealized concept of what was needed. As shown, a scan cell (SC) is located at each input and at each output pin. An output SC cell must be able, in test mode, to force the logic state of its output pin without regard to the state of the system logic. Similarly, each input SC must be able to monitor the signal on its input pin. IEEE 1149.1 was developed to provide this drive/sense capability using, not external test probes, but internal test circuits.

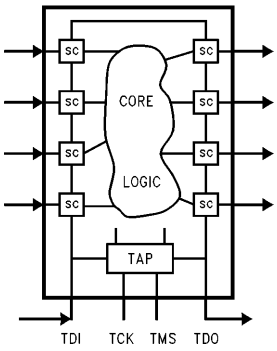

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FIGURE 3. Bed-of-Nails Test Access Has Been Replaced by Adding Embedded Test Probes to Each IC Input and by Providing Test Drivers at Each Output. Driving Outputs and Sampling Inputs is Called EXTEXT

As its name implies, boundary scan provides a scan path around the boundary of an IC as shown in *Figure 3.* Scan test access is a methodology that allows each IC to provide test access from within the IC itself, not from an external array of physical probes.

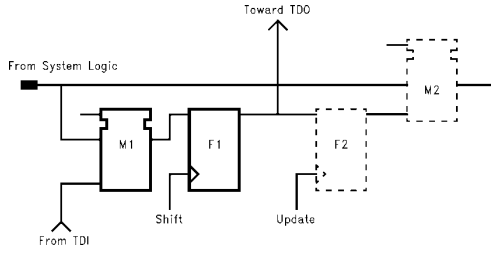
SILICON NAILS

Figure 4 shows an example of the kind of simple circuits needed to sample IC inputs and to replace the normal, mission mode drive values with test values. At each input we need a means for capturing the input signal and then shifting it out for external examation by automated test euuipment (ATE). This input circuit has shown in dashed lines some optional logic that will be discussed later.

The typical output boundary scan circuit is able, with limited external control signals, to become the source of the logic state that will drive the external interconnections. This is a solution to the simple problem of driving and sensing printed circuit board interconnections to detect process defects.

As shown in *Figure 3,* a test access port (TAP) controller is located in each IC to allow the ATE to control the boundary scan cells. The operation of the TAP controller and the implementation of its instructions have been described in detail in the IEEE standard.(1) The TAP has four dedicated test pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), and Test Mode Select (TMS). TDI and TDO are used to shift test data in and out of each 1149.1-compliant IC.

TCK shifts the data through each chip, while TMS controls a 16-state finite state machine in each IC. The state machine determines what each IC is doing. For example, an IC may be sampling its input, shifting data or driving outputs. In fact, the TMS input together with the TAP controller can shift TDI



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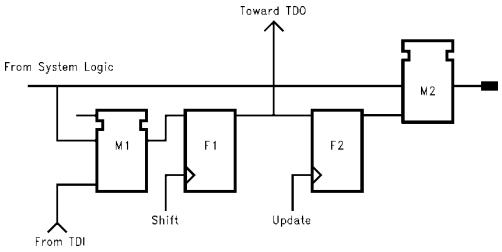

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FIGURE 4. With IEEE 1149.1 I/O Pins May Capture the Data Arriving at a Pin and They May Be Used to Control Output Pins. Test Circuits Such as These May Also Test Internal System Logic. Circuits Such as These are Added to All System Pins

data into an instruction register. With the flexibility provided by an instruction register, IEEE 1149.1 is able to support an almost unlimited number of optional test features.

In 1149.1 the ability to drive test values onto output pins and to capture input logic states using the test logic is called EXTEST for external test. Most interconnect faults may be detected. For example, if a surface mount IC has a lead that is not attached to the printed circuit module as shown in *Figure 5,* the fault can be detected. Assume that this is an output, if the boundary-scan cell at that pin attempts to force the connected network, there will no response on the inputs that should be driven. The input boundary-scan cells of other ICs will detect a defect when they sample their input net.

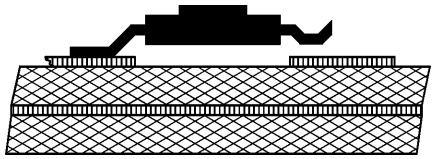

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FIGURE 5. Lifted IC Leads, Not Accessible with Bed-of-Nails by the Embedded Probes of the Driving and Receiving IC, if they Implement Boundary-Scan

Before 1149.1, to force the output driver in the IC with the lifted pin required that the automated test equipment generate a sequence of test vectors to force the inputs of the IC. This pattern would indirectly control the IC output. Controlling IC outputs from the inputs requires a complete functional understanding of the IC. This points out another advantage of IEEE 1149.1: PWB interconnect test programs can be developed without a detailed understanding of the function of each IC on the PWB. This simplification has resulted in test development time reductions that have compressed schedules from months to as little as one day.(2)

When bed-of-nails testers are used, it is necessary to control IC outputs by forcing the network to the desired test level even if the IC driving the net is attempting to force the net to the opposite level. This can result in forcing current levels well beyond manufacturer's specified maximum limits. The time spent backdriving an IC output must be limited to minimize reliability degradation. Using boundary-scan to test for interconnect faults removes the need to backdrive IC outputs.

REMOTE TEST ACCESS

Because direct physical access is not needed to detect faults, diagnostic tests may be run remotely. It is possible to test a digital system without even opening the system cabinet. Because physical access is not required, test engineers can run many PWB and system tests remotely using modem-connected testers without even leaving their office.

TESTING ICs AFTER PWB ASSEMBLY

IEEE 1149.1 can test more than the interconnections. It can also test ICS. Although bed-of-nails supported IC testing by forcing pins to required logic levels, boundary-scan registers allow test vectors to be shifted right into each IC. Once the vectors are in the IC commands such as INTEST for internal test can be used to deliver these test vectors to the inside of the IC. INTEST test results can be read using the scan cells at the IC output pins. INTEST uses the dashed line logic in *Figure 4* to connect the test stimulus to the IC's internal system logic. Using INTEST it is possible to deliver the same test vectors after PWB assembly as were used during component test at the IC foundry. The scan ring may be used to shift patterns to each IC allowing all ICs to be tested concurrently.

BUILT-IN-SELF-TEST (BIST) TECHNIQUES

IEEE 1149.1 can be used to support other test strategies. For example if an embedded deterministic pattern generator were built by reconfiguring a scan register, it might be possible to generate a new test vector with each clock pulse. This is a big time reduction compared to shifting in a new pattern with one clock pulses per bit in the PWB's scan path.

To test a multiplier, 1149.1 instructions could be used to reconfigure the test logic into a pattern generator and to connect the resulting patterns to the input ports of a multiplier. The reduce the time required to check each product at the multiplier output, other test logic can be used to compress the individual multiplier results into one composite test signature. If the test sequences are repeated in exactly the same way for unknown and for good multipliers, it is reasonable to conclude that multipliers that give the same result as a known good multiplier are probably defect free.

IEEE 1149.1 can be used to configure, to control and to observe BIST logic. For example, 1149.1 can be used to initialize the starting values for BIST pattern generators. It can be used to control test clocks. It can be used to shift out test results for examination by the ATE. BIST controlled by 1149.1 can reduce test time by orders of magnitude compared to the time required by shifting in vectors one at a time.

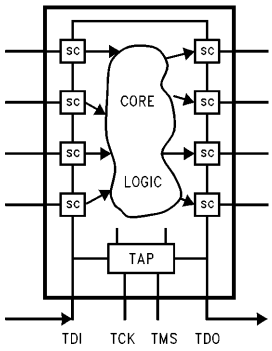

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FIGURE 6. Exploiting the Boundary-Scan Test Logic to Also Test the Interior of an IC. IEEE 1149.1 Defines a Standard Instruction Called INTEST

CHECKING FOR CORRECT COMPONENT SELECTION

IEEE 1149.1 can even be used to check for correct component selection. This feature was supported within the standard by defining an optional test feature called the IDCODE instruction. When the IDCODE command is included and executed, a 32-bit idcode will be the next pattern shifted out of the IC on the TDO pin.

The 32-bit code contains JEDEC-related manufacturer's identification, a part number as defined by the component manufacturer, and four bits that may be used to track design versions. Thus, without visual inspection, a printed circuit board may be inspected for correct component selection. The ability to electronically distinguish between different versions of an ASIC is intended to reduce errors caused by incorrect package labeling, and by accidental use of obsolete versions.

A system can be examined for the use of obsolete versions of an IC by reading each IDCODE. Remote access could be implemented. One day it may be possible to inspect systems that are in the field for known defective ICs. It is possible that the inspection could be completed without ever taking control of the system from a customer. With remote access, it may be possible to completely inspect a site without even visiting the facility.

EXAMPLE DESIGN

Some systems do not have spare backplane pins to allow 1149.1 to be added to the system. One solution to this test access problem is shown in *Figure 7.* Here a typical bus master, SCANPSC100[3,4,5], is connected to the system logic level backplane buses. The component converts the backplane bus to an 1149.1 test bus on the very PWB that needs the test bus.

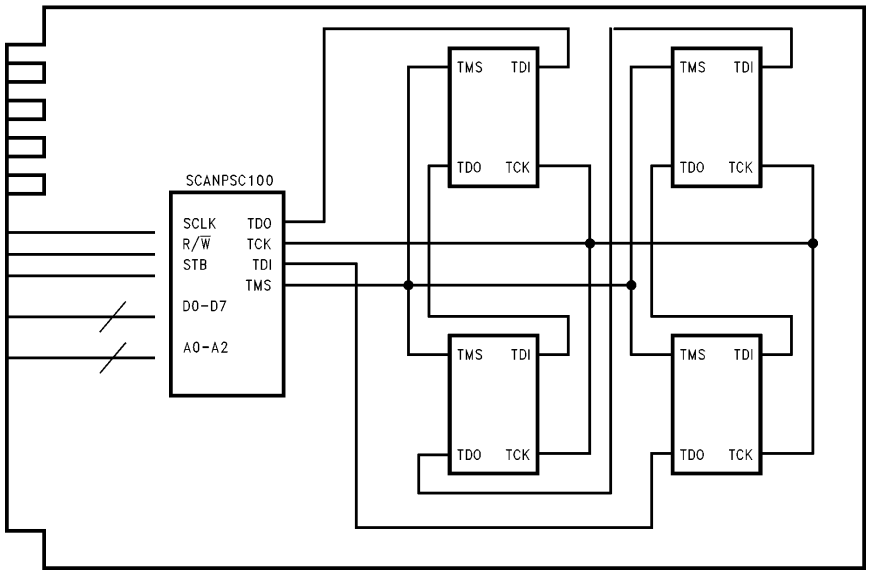

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FIGURE 7. An Example of 1149.1 Applied to the Test Access of a PWB with No Spare Backplane Pins to Provide Test Access. A Typical Bus Master, SCANPSC100, Develops the Needed Test Port on the Module

On the PWB are shown a few SCAN Widebus interface circuits whose 1149.1 test ports are connected to the bus master. These bus circuits and other 1149.1 compliant ASICs can be controlled by the four pin test bus. The diagnostic processor that stores and executes the 1149.1 tests could be the main system computer.

CONCLUSIONS

The IEEE has defined a boundary scan test access standard that supports test access that will allow packing density to continue to increase with regard to the need for direct physical test access. The standard offers features that allow not only interconnections to be tested, but for attached ICs as well.

DISCLAIMER

The opinions expressed herein are entirely personal and do not necessarily reflect those of either the IEEE or any of the 1149 Working Groups.

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