

A

ANSI/TIA/EIA-644 standard, 2

application notes, 77

applications, see LVDS applications

B

backplane, 16-17

behavioral models, see IBIS models

BER testing, 59-61

bidirectional, see LVDS configurations

bit error rate testing, see BER testing

bypassing, 27-28, 69

C

cable ground, see ground return paths

cable shielding, 39, 51-54

cables, 1, 3, 5-6, 11, 13-17, 33-34, 42-43, 51-58, 67-68, 70-71

CAT3 cable, see twisted pair cable

CAT5 cable, see twisted pair cable

Channel Link latency, 22

Channel Link, 6, 14-17, 22, 65, 78

clock vs. data rate, note on page 21

CMR, see common mode noise rejection

coax, 52

common mode noise rejection, 2, 28, 32, 33-37, 40-42, 51, 68-69

comparisons to other technologies, 3-4, 11-17, 33, 36-37, 38

configurations, see LVDS configurations

connectors, 30, 53

cost, **5-6**, **11-17**, 51-52

crosstalk, 27, **32**, 36-37, 40-45, 51-53, 68-69

current mode output, **1**, 2, 33

D

data rate over cables, 54-58

data vs. clock rate, note on page 21

demo boards, see evaluation boards

differential impedance, **27-29**, 30-31, 33-37, 45, 51, 68-69

differential waveform, 69

drivers & receivers, 1-2, 4-6, **12-13**, **21**, 42-45, 53-54, 58, 66-74, 78

E

electromagnetic interference/radiation/
compatibility, see EMI

EMC, see EMI

EMI tests, 38-39

EMI, 1-2, 11-17, 27-30, **33-39**, 40-42, 43-45, 51-54, 68

EMI: design for low EMI, 27-30, **33-39**

evaluation boards, 21-23, 65-73

F

fail-safe, 4, 30, **43-45**

Flat Panel Display -Link, see FPD-Link

flex circuit, 51

floating pins, see unused pins

FPD-Link, 6, **23**, 65, 78

G

ground return paths, 39, **53-54**

grounding, see ground return paths

H

hot insertion, see power off high impedance

hot swap, see power off high impedance

I

I/O models, see IBIS models

IBIS models, 78

IEEE 1596.3 standard, 3

I_{OFF} , see power off high impedance

J

jitter, 54-58

L

latency, see Channel Link latency

live insertion, see power off high impedance

LVDS operation, 1

LVDS applications, 6

LVDS configurations, 4-5, **42-43**

LVDS definition, 1

LVDS device selection, 21-23

LVDS standard, see ANSI/TIA/EIA-644 standard

M

microstrip, **28-29**, 34-36, 68-69

multidrop, see LVDS configurations

N

noise, 1-2, 4, 11-17, 27-42, 43-45, 51-61, 68-69, 73

P

PCB design, 27-39, 68-69

PCB trace shielding, **34-36**, 51

PECL, **3-4**, **11-17**

point-to-point, see LVDS configurations

power consumption, 4, **12**, **11-17**

power off high impedance, 45

power supply, 15, 17, **27-28**

printed circuit board, see PCB design

probing, see signal probing

R

receivers, see drivers & receivers

ribbon cable, 52

RS-422, **3-4**, **11-17**

S

SCI standard, see IEEE 1596.3 standard

shielding, see cable shielding or PCB trace shielding

signal probing, 30, 69-72

simulation models, see IBIS models

single-ended waveforms, 69

stripline, **28-29**, 34-35

T

TDR measurements, 30-31

termination, 3, **30**, 68

time domain reflectometer, see TDR measurements

twinax, 52

twisted pair cable, 1, 3, 5, 13-17, **52**, **54-58**, 67-68, 70-71

TWP, see twisted pair cable

U

unused pins, 4, **30**, **43-45**, **52-53**, 68

UTP, see twisted pair cable