LVDS Evaluation Boards

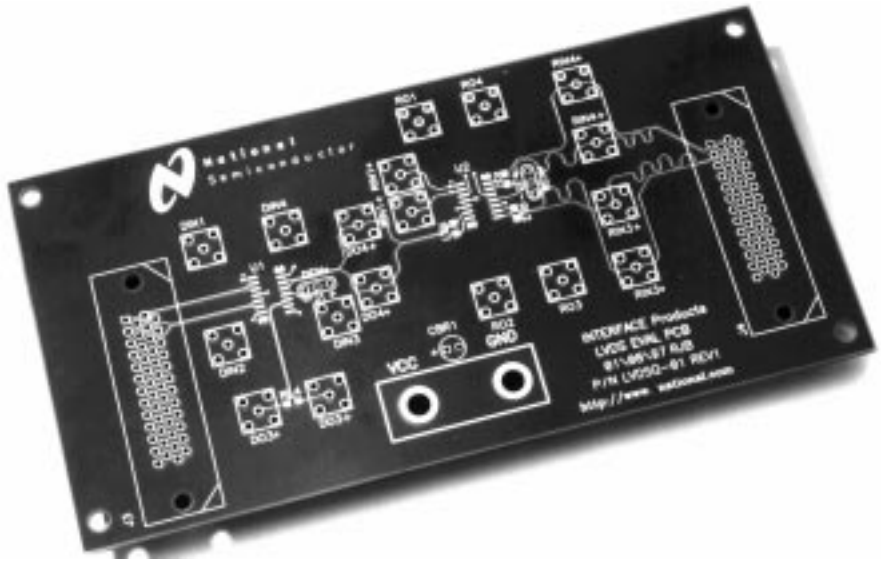
Chapter 6

6.0.0 LVDS EVALUATION BOARDS

Presently there are two types of evaluation boards available: The high speed link (includes Channel Link and FPD-Link) evaluation boards and the Generic LVDS Evaluation Board. (See the selection tables in chapter 3 for a cross reference list of boards versus devices.) The high speed link evaluation boards can be ordered through National's distributors and come complete with a transmitter board, receiver board, ribbon cable, instructions, and datasheets.

FPD-Link Evaluation Board (the Channel Link evaluation board is similar)

These boards are fully populated. TTL signals are accessed through a 50-pin IDC connector on the transmitter and receiver boards. The boards are interconnected via a ribbon cable that can be modified for custom lengths. These evaluation boards are useful for analyzing the operation of National's high speed Channel Link and FPD-Link devices in your system. For LVDS signal quality measurements over other interconnect media, use the Generic LVDS evaluation board.



The Generic LVDS Evaluation Board

The Generic LVDS Evaluation Board is used to measure LVDS signaling performance over different media. Individual LVDS channels can be evaluated over PCB trace, twisted pair cable, or custom transmission medium. Though LVDS quad drivers and receivers are used on the board, they can represent the LVDS I/O characteristics of most of National's LVDS devices.

a) Use the DS90C031/032 to represent the LVDS I/O characteristics of all 5V drivers/receivers, 5V Channel Link, and 5V FPD-Link devices.

b) Use the DS90LV031/032 to represent the LVDS I/O characteristics of the DS90LV031/032/017/027 devices.

c) Use the upcoming DS90LV031A/032A (available in October 1997) to represent the LVDS I/O characteristics of 3V Channel Link, 3V FPD-Link, and other 3V devices not listed in (b) above.

The remainder of this chapter is devoted to explaining the operation of the Generic LVDS Evaluation board.

6.1.0 THE GENERIC LVDS EVALUATION BOARD

6.1.1 Purpose

The purpose of the Low Voltage Differential Signaling (LVDS) Evaluation Printed Circuit Board (PCB) is to demonstrate the line driving capability of LVDS technology across a short PCB interconnect, and also across a variable length of twisted pair cable. Probe points for a separate driver and a separate receiver are also provided for individual line driver or receiver testing. The part number for the Evaluation PCB is LVDSEVAL-001 (stuffed) or Literature number 550061-001 (unstuffed - limit one per Customer, while supplies last). In this application note and on the PCB the following differential signal nomenclature has been used: "A" represents the true signal and "B" represents the inverting signal. Driver input signals are represented with an "I" while receiver outputs are with an "O."

6.1.2 Five Test Cases

Five different test cases are provided on this simple 4 layer FR-4 PCB. Each case is described separately next. Note that the driver / receiver numbers do not directly map to the LVDS test channel number (LVDS Channel 1 utilizes driver number 1 and receiver number 4). The five test cases are shown in figure 1.

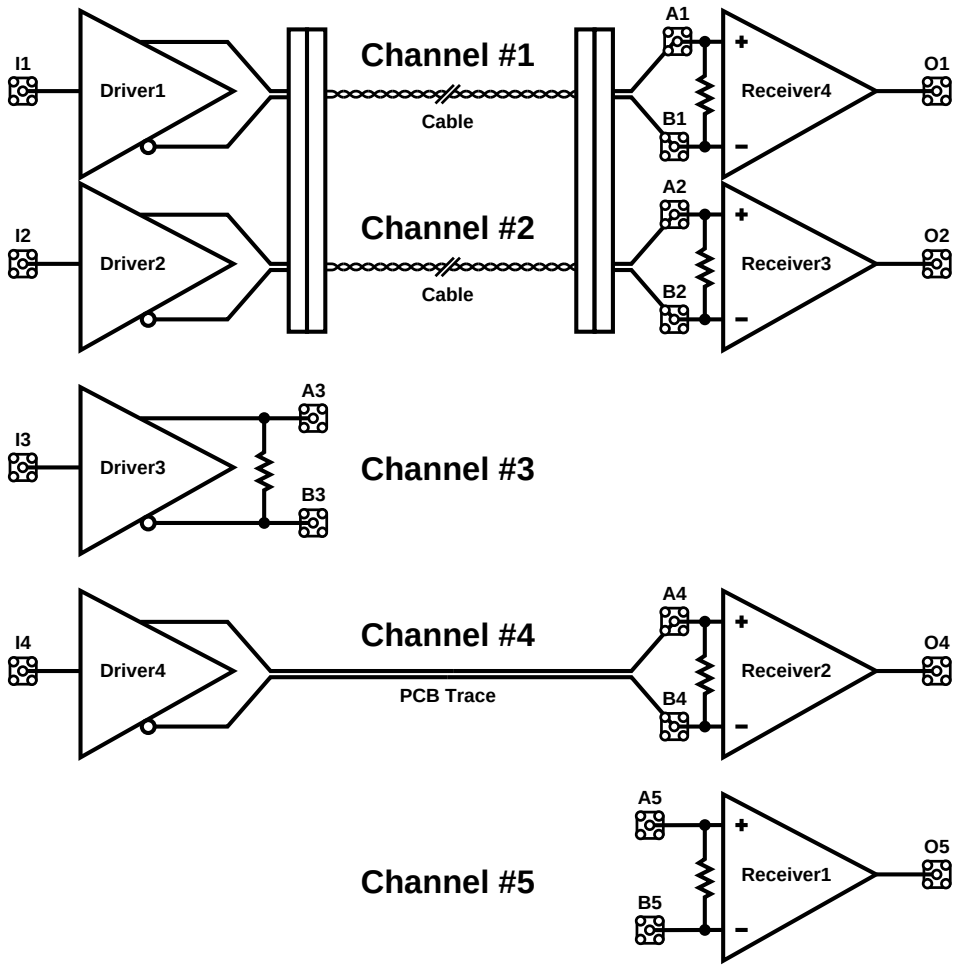


Figure 1: PCB Block Diagram

LVDS Channel # 1: Cable Interconnect

This test channel connects Driver #1 to Receiver #4 via the cable interconnect. A SMB test point interface is provided at the receiver input side of the cable. The driver input signal (I1) is terminated with a 50 Ohm termination resistor on the bottom side of the PCB. LVDS signals are probed via test points A1 and B1. The receiver output signal may be probed at test point O1. A PCB option for a series 450 Ohm resistor is also provided in case 50 Ohm probes are employed on the receiver output signal (see options section). A direct probe connection is possible with a high impedance probe (>100 k Ohm loading) on the LVDS signals at test points A1 and B1.

LVDS Channel # 2: Cable Interconnect

This test channel connects Driver #2 to Receiver #3 also via the cable interconnect. A SMB test point interface is provided at the receiver input side of the cable. The driver input signal (I2) is terminated with a 50 Ohm termination resistor on the bottom side of the PCB. LVDS signals are probed via test points A2 and B2. The receiver output signal may be probed at test point O2. A PCB option for a series 450 Ohm resistor is also provided in case 50 Ohm probes are employed on the receiver output signal. A direct probe connection is possible with a high impedance probe (>100 k Ohm loading) on the LVDS signals at test points A2 and B2. This channel duplicates channel #1 so that it may be used for a clock function or for cable crosstalk measurements.

LVDS Channel # 3: LVDS Line Driver

This test channel provides test points for an isolated driver with a standard 100 Ohm differential termination load. Probe access for the driver outputs is provided at test points A3 and B3. The driver input signal (I3) is terminated with a 50 Ohm termination resistor on the bottom side of the PCB.

LVDS Channel # 4: PCB Interconnect

This test channel connects Driver #4 to Receiver #2 via a pure PCB interconnect. A SMB test point interface of the LVDS signaling is provided at test points A4 and B4. The driver input signal (I4) is terminated with a 50 Ohm termination resistor on the bottom side of the PCB. The receiver output signal may be probed at test point O4. A PCB option for a series 450 Ohm resistor is also provided in case 50 Ohm probes are employed on the receiver output signal. A direct probe connection is possible with a high impedance probe (>100 k Ohm loading) on the LVDS signals at test points A4 and B4. This channel may be used for analyzing the LVDS signal without the bandwidth limiting effects of a cable interconnect.

LVDS Channel # 5: LVDS Receiver

This test channel provides test points for an isolated receiver. Termination options on the receiver inputs accommodate either a 100 Ohm resistor connected across the inputs (differential) or two separate 50 Ohm terminations (each line to ground). The second option allows for a standard signal generator interface. Input signals are connected at test points A5 and B5. A PCB option for a series 450 Ohm resistor is also provided in case 50 Ohm probes are employed on the receiver output signal. The receiver output signal may be probed at test point O5.

6.1.3 Interconnecting Cable and Connector

The evaluation PCB has been designed to directly accommodate a 25 pair (50-pin) SCSI-2 cable commonly referred to as an "A" cable. The pinout, connector, and cable electrical/mechanical characteristics are defined in the SCSI-2 standard and the cable is widely available. The connector is 50 position, with 0.050 centers and the pairs are pinned out up and down. For example pair 1 is on pins 1 and 26, not pins 1 and 2.

IMPORTANT NOTE: The 23 unused pairs and the overall shield are connected to ground. Other cables may also be used if they are built up.

6.1.4 PCB Design

Due to the high speed switching rates obtainable by LVDS a minimum of a four layer PCB construction and FR-4 material is recommended. This allows for 2 signal layers and full power and ground planes. The stack is: signal (LVDS), ground, power, signal (TTL/CMOS).

Differential traces are highly recommended for the driver outputs and the receiver inputs signal (LVDS signals, see PCB layout between U1 and J3). Employing differential traces will ensure a low emission design and maximum common mode rejection of any coupled noise. Differential traces require that the spacing between the differential pair be controlled. This distance should be held as small as possible to ensure that any noise coupled onto the lines will primarily be common mode. Also by keeping the pair close together the maximum canceling of fields is obtained. Differential impedance of the trace pair should be matched to the selected interconnect media (cable's differential characteristic impedance). Equations for calculating differential impedance are contained in chapter 4 of the LVDS Owner's Manual and also in National application note AN-905 for both microstrip and stripline differential PCB traces.

Termination of LVDS lines is required to complete the current loop and for the drivers to properly operate. This termination in its simplest form is a single surface mount resistor (surface mount resistor minimizes parasitic elements) connected across the differential pair as close to the receiver inputs as possible (should be within 0.5 inch (13 mm) of input pins). Its value should be selected to match the interconnects differential characteristics impedance. The closer the match the higher the signal fidelity and the less common mode reflections will occur (lower emissions too). Typical values are 100 or 121 Ohm ±5% (media specific).

LVDS signals should be kept away from CMOS logic signals to minimize noise coupling from the large swing CMOS signals. This has been accomplished on the PCB by routing CMOS signals on a different signal layer (bottom) than the LVDS signals (top) wherever possible. If they are required on the same layer, a CMOS signal should never be routed within three times (3S) the distance between the differential pair (S). Adjacent differential pairs should be at least 2S away also.

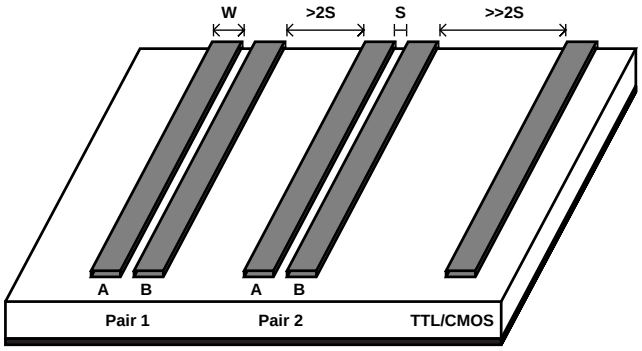


Figure 2: Pair Spacing for differential lines

Bypassing capacitors are recommended for each package. 0.1 µF is sufficient on the quad driver or receiver device (CB2 and CB3) however, additional smaller value capacitors may be added (i.e. 0.001 µF at CB12 and CB13) if desired. Traces connecting Vcc and ground should be wide (low impedance, not 50 Ohm dimensions) and employ multiple vias to reduce inductance. Bulk bypassing is provided (CBR1, close by) at the main power connection as well. Additional power supply high frequency bypassing can be added at CB1, CB11, and CB21 if desired.

6.1.5 Sample Waveforms from the LVDS Evaluation PCB

Single-ended signals are measured from each signal (true and inverting signals) with respect to ground. The receiver ideally switches at the crossing point of the two signals. LVDS signals should swing between 1.0 V (V_{OL}) and 1.3 V (V_{OH}) for a 300 mV V_{OD}. The differential waveform is constructed by subtracting the B (inverting) signal from the A (true) signal. V_{OD} = A - B. The V_{OD} magnitude is either positive or negative, so the differential swing (V_{SS}) is twice the V_{OD} magnitude. Drawn single-ended waveforms and the corresponding differential waveforms are shown in Figure #3.

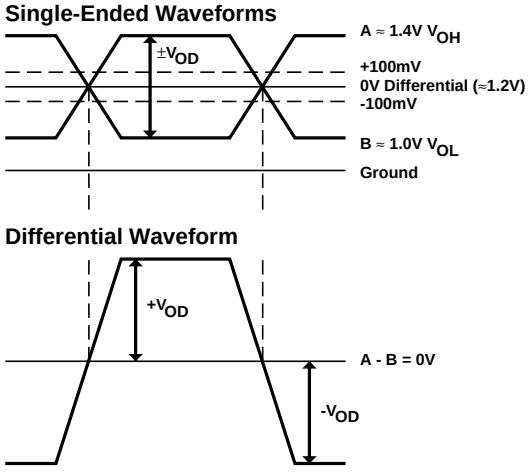


Figure 3: Single-ended & Differential Waveforms

The PCB interconnect signal (LVDS Channel #4) can be measured at the receiver inputs (test points A4 and B4). Due to the short interconnect path via the PCB little distortion to the waveform is caused by the interconnect. See figure 4. Note that the data rate is 50 Mbps and the differential waveform (V_{DIFF}) shows fast transition times with little distortion.

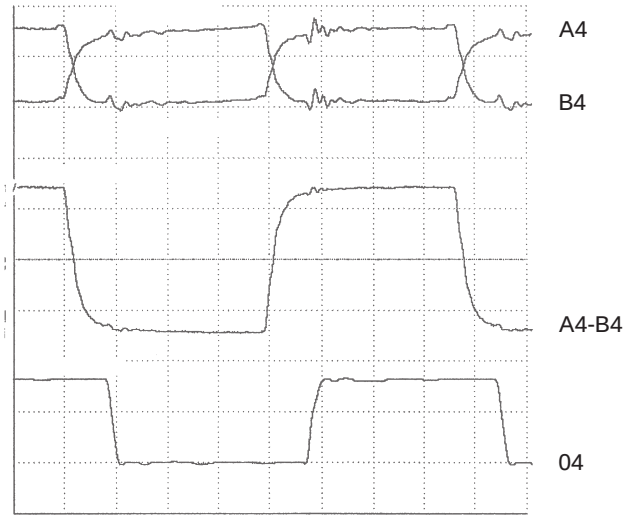


Figure 4: LVDS Channel #4 Waveforms — PCB Interconnect

The cable interconnect signal is also measured at the receiver inputs (test points A1 & B1 and A2 & B2). Due to the characteristics of the cable some waveform distortion has occurred. Depending upon the cable length and quality, the transition time of the signal at the end of the cable will be slower than the signal at the driver's outputs. This effect can be measured by taking rise and fall measurements and increasing the cable length. A ratio of transition time to unit interval (minimum bit width) is a common gauge of signal quality. Depending upon the application ratios of 30% to 50% are common. These measurements tend to be more conservative than jitter measurements. The waveforms acquired with a SCSI-2 cable of 1 meter and also 2 meters in length are shown in figure 5 and 6. Note the additional transition time slowing due to the cable's filter effects on the 2 meter test case.

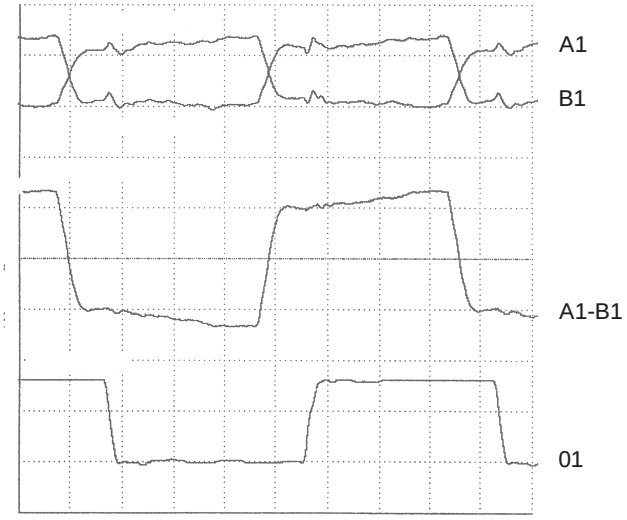


Figure 5: LVDS Channel #1 Waveforms - 1m Cable Interconnect

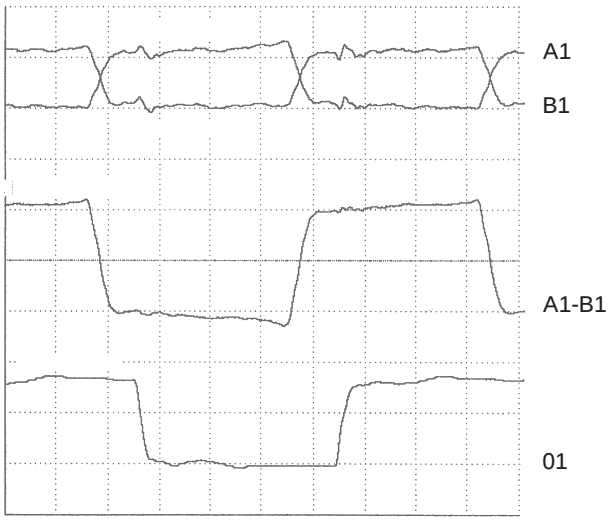


Figure 6: LVDS Channel #1 Waveforms - 2m Cable Interconnect

6.1.6 Probing of High Speed LVDS Signals

Probe specifications for measuring LVDS signals are unique due to the low drive level of LVDS (3 mA typical). A high impedance probe must be used (100k Ohm or greater). The capacitive loading of the probe should be kept in the low pF range, and the bandwidth of the probe should be at least 1 Ghz (4 Ghz preferred) to accurately acquire the waveform under measurement.

National's Interface Applications group employs a wide range of probes and oscilloscopes. One system that meets the requirements of LVDS particularly well is a TEK 11801B scope (50 Ghz Bandwidth) and SD14 probe heads. These probes offer 100k Ohm, 0.4 pF loading and a bandwidth of 4 Ghz. This test equipment was used to acquire the waveforms shown in figures 4, 5 and 6.

LVDS waveforms may also be measured with lower bandwidth / different loading probes such as common TEK probes P6135A (150 MHz/1M Ohm / 10.5 pF). These probes were connected to a TEK 602 scope. See figure 7 for the LVDS waveforms acquired in this set up and compare these to figure 5. The waveform shows less DC loading (1M Ohm compared to 100k Ohm) and also more capacitive loading and bandwidth limiting. Probes with standard 50 Ohm loading should not be since they will load the LVDS signals too heavily. 50 Ohm probes may be used on the receiver output signal in conjunction the 450 Ohm series resistor option (see option section below). Note that the scope waveform is an attenuated signal (50/(450 +50) or 1/10) of the output signal and the receiver output is loaded with 500 Ohm to ground.

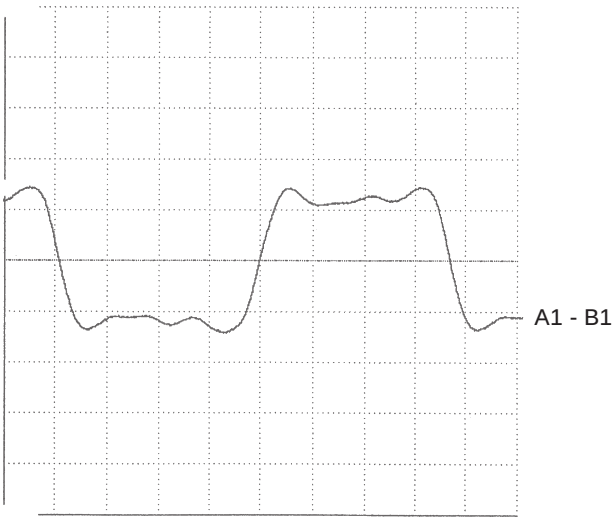


Figure 7: LVDS differential waveform measured with TEK P6135A probes and 602 scope

6.1.7 Demo PCB Options

Option 1: 450 Ohm Resistors

A provision for a series 450 Ohm resistor (RS1-4) is provided on the receiver output signal. By cutting the trace between the "RS" pads and installing a 450 Ohm resistor a standard 50 Ohm scope probe may be used (500 Ohm total load). Note that the signal is divided down (1/10) at the scope input.

Option 2: Disabling the LVDS Driver

The quad driver features a ganged enable. An active high or an active low input are provided. On the evaluation PCB the active high input has been hard wired to ground (-, off). The active low input (EN*) is routed to a jumper (J1). The jumper provides a connection to the Vcc plane (+) or to the Ground plane (-). To enable the driver connect the jumper to ground, to disable the driver connect the jumper to the power plane.

Option 3: Disabling the LVDS Receiver

The quad receiver features a ganged enable (same as the driver). An active high or an active low are provided. On the evaluation PCB the active high input has been hard wired to ground (-, off). The active low input (EN*) is routed to a jumper (J2). The jumper provides a connection to the Vcc plane (+) or to the Ground plane (-). To enable the receiver connect the jumper to ground, to disable the receiver connect the jumper to the power plane.

Option 4: Cables

Different cables may also be tested (different lengths, materials, constructions). A standard SCSI-2 50-pin connector/pinout has been used (J3 and J4). Simply plug in a SCSI-2 cable or build a custom cable.

Option 5: Power Supply /Components (C/LV/422)

The LVDS quads are offered in an industry standard pinout made popular by the 26LS31/2 quad 5V RS-422 devices. This standard pinout allows different devices (and power supplies) to be substituted and evaluated. The following National Semiconductor devices may be tested (U1/U2):

Devices (D/R)	Power Supply	Signaling Levels
DS90C031/2	5V	LVDS Signals
DS90LV031/2	3.3V	LVDS Signals
DS90LV031A/2A	3.3V	FAST LVDS (planned devices)
DS26C31/2A	5V	RS-422 Signals
DS26LV31/2A	3.3V	RS-422 Signals

Option 6: Receiver Termination (Channel #5)

The separate receiver input signals can be terminated separately (50 Ohm on each line to ground) utilizing pads RT5 (true input to ground) and RT6 (inverting to ground) for a signal generator interface. Or with a single 100 Ohm differential resistor (pad RL5) if the device is to be driven by a differential driver.

6.1.8 Plug & Play

The following simple steps should be taken to begin testing on your completed evaluation board:

1) Connect signal common (Ground) to the black binding post

2) Connect the power supply lead to the red binding post (5V or 3.3V)

3) Set J1 & J2 jumpers to ground (-) to enable the drivers and receivers

4) Connect a signal generator to the driver input (I4) with:

   a) frequency = 50 Mhz (100 Mbps)

   b) V_{IL} = 0V & V_{IH} = 3.0V

   c) t_r & t_f = 2 ns

   d) duty cycle = 50% (square wave)

5) Connect high impedance probes to test points A4 and B4

6) View LVDS signals using the same voltage offset and volts/div settings on the scope with high impedance probes. View the output signal on a separate channel from test point O4.

6.1.9 Common Mode Noise

When the receivers (DS90C032, DS90LV032) are enabled common mode noise is passed from the output of the receiver to the inputs. This noise shows up on the single-ended waveforms, but does not impact the differential waveform that carries the data. For improved signal fidelity a design improvement is under way to reduce the magnitude of the noise coupled back to the inputs. This noise will not be observed if the receiver device is disabled by setting J2 to “+”.

6.1.10 Summary

This evaluation PCB provides a simple tool to evaluate LVDS signaling across different media and lengths to determine signal quality for data transmission applications.

6.1.11 Appendix

Typical test equipment used for LVDS measurements:

Signal Generator	TEK HFS 9009
Oscilloscope	TEK 11801B
Probes	TEK SD-14

Bill of Materials

Type	Label	Value / Tolerance	Qty	Footprint	Part Number
IC	U1	(Quad Driver)	1	16-L SOIC	DS90LV031TM or other
IC	U2	(Quad Receiver)	1	16-L SOIC	DS90LV032TM or other
Connector	J3, J4	(50 pin SCSI-2)	2		AMP P/N 749721-5
Resistor	RT1-4	50 Ohm	4	RC0805	
Resistor	RL1-5	100 Ohm	5-Apr	RC0805	
Resistor	RS1-4	450 Ohm	0/4	RC0805	
Capacitor	CB2, CB3	0.1 uF	2	CC0805	
Capacitor	CB12, CB13	0.001 uF	0/2	CC0805	
Capacitor	CBR1	10 uF, 16V	1	CAP100RP	Electrolytic Radial Lead
Capacitor	CB1/11/21	na	0/3	CC0805	
Jumper Stakes	J1, J2x	3 STAKES	2		100 mil spacing
Jumpers	-		2		
SMB Jack	-		18	SMB Connector	Labels: I1-4, A1-5, B1-5, O1-2, O4-5. EF Johnson P/N 131-1701-201
Plug		Binding Post	2		Superior Electronic P/N BP21R, BP21B (1 each)
Cable	na	SCSI-2 type A Cable	0/1		
Legs			4		
bolts/washers			4		
PCB			1		LVDSEVAL-001 or LIT#550061-001