Designing with LVDS

Chapter 4

4.0.0 DESIGNING WITH LVDS

4.1.0 PCB BOARD LAYOUT TIPS

Now that we have explained how LVDS has super speed, and very low power, noise, and cost, many people might assume that switching to LVDS (or any differential technology) will solve all of their noise problems. It will not, but it can help a lot! LVDS has low swing, differential, ≈3.5mA current mode outputs that can help reduce noise/EMI significantly, but these outputs switch (rise and fall) in less than a nanosecond which means many signal paths act as transmission lines. Therefore, knowledge of ultra-high speed board design and differential signal theory is required. Designing high speed differential boards is not difficult or expensive, so familiarize yourself with these techniques *before* you begin your design.

The speed of LVDS means that impedance matching is very important even for short runs. Matching the differential impedance is as important as matching single-ended impedance. Discontinuities in differential impedance **will** create reflections which will degrade the signal and also show up as common mode noise. Common mode noise on the line will not benefit from the cancelling magnetic field effect of differential lines and will be radiated as EMI. You should use controlled differential impedance traces as soon as you can after the signal leaves the IC. Try to keep stubs and uncontrolled impedance runs to <12mm (0.5in). Also, do not make 90° turns since this causes impedance discontinuities, radius or bevel PCB traces.

Minimize skew between conductors within a differential pair. Having one signal of the pair arrive before the other creates a phase difference between voltages along the signal pairs which looks like and radiates as common mode noise.

Use bypass capacitors at each package and make sure each power or ground trace is wide and short (do not use 50Ω dimensions) with multiple vias.

A detailed list of suggestions for designing with LVDS is shown next. The suggestions are inexpensive and easy to implement. By using these suggestions as guidelines, your LVDS-based systems should be quick and easy to develop.

4.1.1 PC Board

a) **Use at least 4 PCB board layers** (top to bottom): LVDS signals, ground, power, TTL signals.

b) **Isolate TTL signals from LVDS signals**, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

c) Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

d) Bypass each LVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best.

Power Supply: A 10µF 35V tantalum capacitor works well between supply and ground. 4.7µF is common, but choosing a capacitor value which best filters the largest power/ground frequency components (usually 100 to 300MHz) is best. This can be determined by checking the noise spectrum of V_{CC} across bypass capacitors. The voltage rating of tantalum capacitors is critical and must not be less than 5 x V_{CC}. Some electrolytic capacitors also work well.

V_{CC} Pins: Two or three multi-layer ceramic (MLC) surface mount capacitors (0.1µF, 0.01µF, and 0.001µF) in parallel should be used between each V_{CC} pin and ground. The capacitors must be placed as close as possible to the V_{CC} pins. Wide (>4 bits) and PLL-equipped (e.g. Channel Link & FPD Link) LVDS devices should have three capacitors, while other LVDS devices are usually fine with a 0.1µF (possibly also a 0.01µF) capacitor. The bottom line: use good bypassing practices. EMI can be greatly reduced by keeping power and ground planes quiet.

e) **Power and ground should use wide (low impedance) traces.** Do not use 50Ω design rules on power and ground traces.

f) Keep ground PCB return paths short and wide.

g) Cables should employ a ground return wire connecting the grounds of the two systems. See section 5.3.0

h) **Use multiple (at least two) vias to connect to power and ground, traces and planes**. Surface mount capacitors can be soldered directly to these via pads to reduce stubs, though solderability may be impacted.

4.1.2 Traces

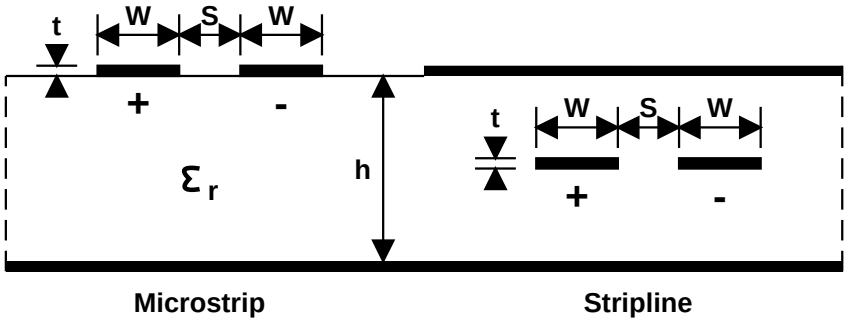
a) Microstrip or stripline both work well.

b) Microstrip offers the advantage that higher differential Z_0 is possible and no extra vias are required.

c) Stripline offers better shielding between signals.

4.1.3 Differential Traces

a) **Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be <10mm long)**. This will help eliminate reflections and ensure noise is coupled as common mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common mode which is rejected by the receiver.



When calculating differential Z_0 (Z_{DIFF}), adjust trace width "W" to alter Z_{DIFF}. Do not adjust "S" which should be the minimum spacing specified by your PCB vendor. You can use National's Transmission Line RapiDesigner slide rule (lit# 633200-001 metric or #633201-001 English units) and app note AN-905, lit# 100905-001) to calculate Z_0 and Z_{DIFF}, or you can use the equations below:

$$Z_{DIFF} \approx 2*Z_0 \left(1 - 0.48e^{-0.96\frac{s}{h}}\right) \text{ Ohms} \quad \text{Microstrip}$$

$$Z_{DIFF} \approx 2*Z_0 \left(1 - 0.347e^{-2.9\frac{s}{h}}\right) \text{ Ohms} \quad \text{Stripline}$$

where

$$Z_0 \approx \frac{60}{\sqrt{0.475\,E_r + 0.67}} \ln\left(\frac{4h}{0.67\,(0.8w + t)}\right) \text{ Ohms} \quad \text{Microstrip}$$

$$Z_0 \approx \frac{60}{\sqrt{E_r}} \ln\left(\frac{4h}{0.67\,\pi\,(0.8w + t)}\right) \text{ Ohms} \quad \text{Stripline}$$

Use consistent (e.g. centimeters only) dimensions for s, h, w, and t.
Cautionary note: The expressions for Z_{DIFF} were derived from empirical data and results may vary.

Common values of dielectric constant (E_r) for various printed circuit board (PCB) materials is given below. Consult your PCB manufacturer for actual numbers. Note that in most LVDS applications, the widely used FR-4 PCB material is acceptable. Teflon is about four times as expensive as FR-4, but can be considered for 100+MHz designs. Also note that E_r will vary within a single board. It is not uncommon for FR-4 PCBs to vary by 10% across one board, affecting skew. This is another good reason to keep differential lines close together.

PCB Material	Dielectric Constant (E_r)	Loss Tangent
Air	1.0	0
PTFE (Teflon)	2.1-2.5	0.0002-0.002
BT Resin	2.9-3.9	0.003-0.012
Polyimide	2.8-3.5	0.004-0.02
Silica (Quartz)	3.8-4.2	0.0006-0.005
Polyimide/Glass	3.8-4.5	0.003-0.01
Epoxy/Glass (FR-4)	4.1-5.3	0.002-0.02

b) Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, $v = c/E_r$ where c (the speed of light) = 0.2997mm/ps or 0.0118in/ps).

c) Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match
differential impedance and provide isolation for the differential lines.

d) Minimize the number of vias and other discontinuities on the line.

e) **Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels instead.**

f) Within a pair of traces, the distance between the two traces should be minimized to maintain common mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

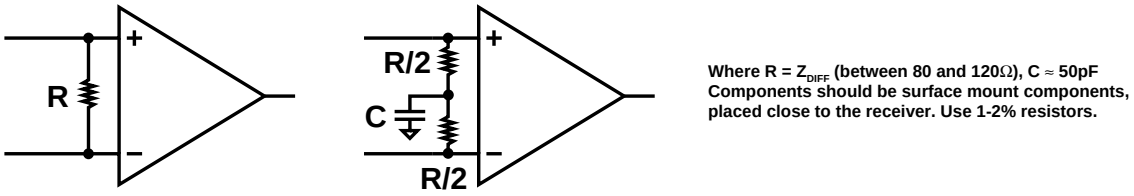
4.1.4 Termination

a) **Use a termination resistor which best matches the differential impedance of your transmission line.** It should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination.

b) Typically a single resistor across the pair at the receiver end suffices.

c) Surface mount 1-2% resistors are best. PCB stubs, component leads, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be <7mm (12mm MAX).

d) Center tap capacitance termination may also be used in conjunction with two ≈50Ω resistors to filter common mode noise at the expense of extra components if desired.



Where R = Z_{DIFF} (between 80 and 120Ω), C ≈ 50pF Components should be surface mount components, placed close to the receiver. Use 1-2% resistors.

Common termination schemes.

4.1.5 Unused Pins

a) **Leave unused LVDS receiver inputs open (floating).** Their internal fail-safe feature will lock the outputs high. These unused receiver inputs should not be connected to noise sources like cables or long PCB traces — float them near the pin.

b) Leave all unused LVDS and TTL outputs open (floating) to conserve power.

c) Tie unused TTL transmitter/driver inputs and control/enable signals to power or ground.

4.1.6 Probing LVDS Transmission Lines

a) **Always use a high impedance (>100kΩ), low capacitance (<0.5pF) scope probes with a wide bandwidth (>3GHz) scope.** Improper probing *will* give deceiving results.

4.1.7 Loading LVDS I/O

a) Avoid placing any devices which heavily load the low, ≈3.5mA LVDS output drive. If additional ESD protection devices are desired, use components which do not add a significant load to the LVDS output. Some of the connectors with integrated polymer ESD protection are a good option.

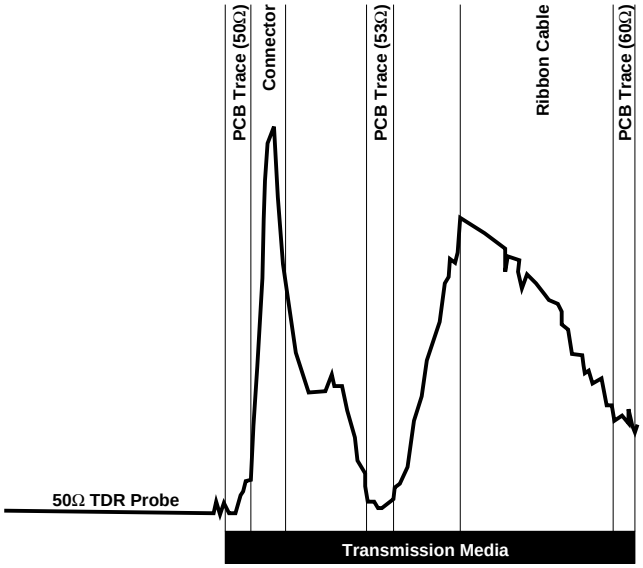
b) Try not to disturb the differential balance. Treat both members of a pair equally.

4.2.0 RESULTS OF GOOD VS. BAD DESIGN PRACTICES

4.2.1 Impedance Mismatches

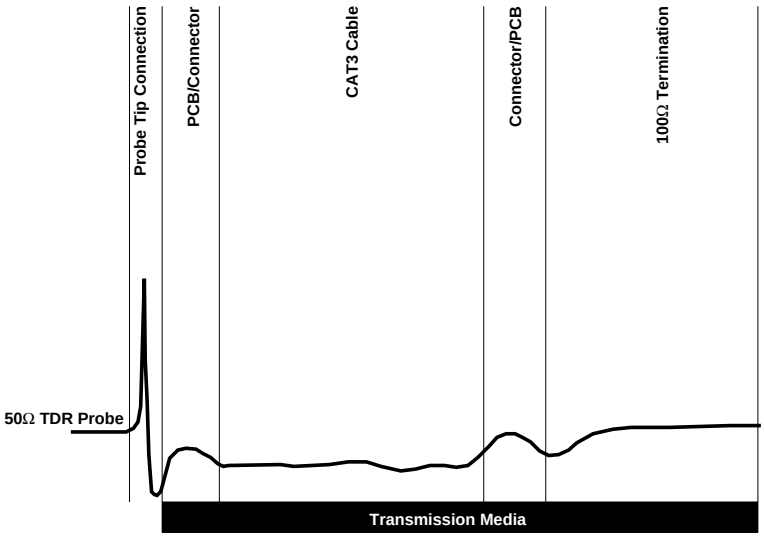
It is very common for designers to automatically use any off-the-shelf cables and connectors and 50Ω autorouting when doing new designs. While this may work for some LVDS designs, it can lead to noise problems. Remember that LVDS is differential and does have low swing, current mode outputs to reduce noise, but that its transition times are quite fast. This means impedance matching (especially differential impedance matching) is very important. Those off-the-shelf connectors and that cheap blue ribbon cable

are not meant for high speed signals (especially differential signals) and do not have controlled impedance. The figure below shows a time-domain reflectometer (TDR) impedance trace of such a system. As one can plainly see, impedance are neither matched nor controlled. Beware, this example is not worst case — it is a typical example reflecting common TTL design practices. The reflections caused by impedance mismatching will generate a lot of noise and EMI.



TDR plot of transmission media with mismatched impedance.

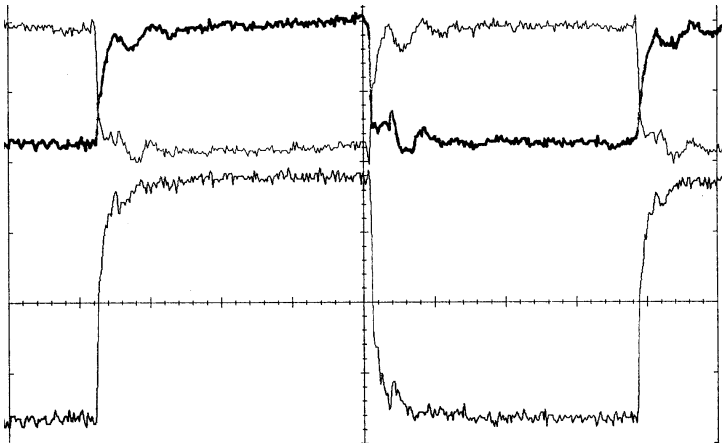
Below is a much improved design which follows most of the high speed differential design practices listed in Section 4.1. The TDR differential impedance plot is much flatter and noise is **dramatically** reduced.



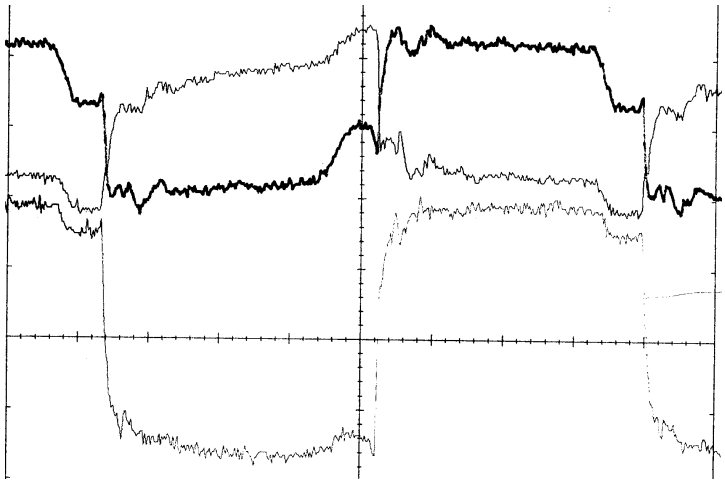
Minimize impedance variations for best performance.

4.2.2 Crosstalk Between TTL and LVDS Signals

The next two figures show the effects of TTL coupling onto LVDS lines. The first figure shows the LVDS waveforms before coupling, while the second shows the effects of a 25MHz, 0V to 3V TTL signal upon the LVDS signals running adjacent for 4 inches. The result is an LVDS waveform modulated by the TTL signal. Note that the LVDS pair is not affected exactly equally — the signal which runs closest to the TTL trace is affected more than the other. This difference will not be rejected by the receiver as common mode noise and though it will not falsely trigger the receiver, it does degrade the signal quality of the LVDS signal reducing noise margin. The common mode noise will be rejected by the receiver, but can radiate as EMI.



LVDS signals before crosstalk.



LVDS signals affected by TTL crosstalk.

In summary, place TTL signals at least 12mm away from LVDS signals or place a power or ground plane between them.

4.3.0 LOWERING ELECTROMAGNETIC INTERFERENCE (EMI)

4.3.1 LVDS and Lower EMI

High speed data transmission usually means fast edge rates and high EMI. LVDS, however, has many positive attributes that help lower EMI:

1) The low output voltage swing (≈350mV)

2) Relatively slow edge rates, dV/dt ≈ 0.350V/0.5ns = 0.7 V/ns

3) Differential (odd mode operation) so magnetic fields tend to cancel

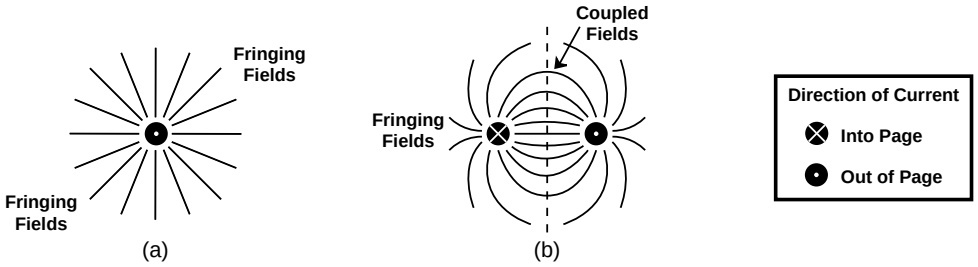
4) "Soft" output corner transitions

5) Minimum I_{CC} spikes due to low current mode operation

To realize these advantages, however, designers must take care to ensure the close proximity of the pair conductors and to avoid creating impedance imbalances within a pair. The following sections describe these EMI-friendly design practices.

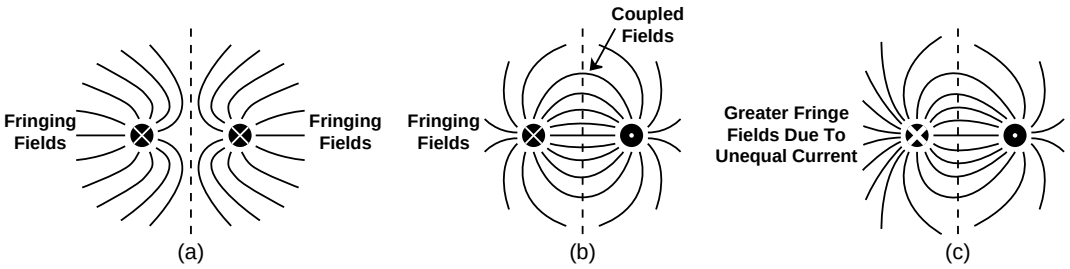
4.3.2 Electromagnetic Radiation of Differential Signals

Today's increasing data rates and tougher electromagnetic compatibility (EMC) standards are making electromagnetic radiation an increasing concern. System designers are usually most concerned with far field electromagnetic radiation, propagated through transverse electromagnetic (TEM) waves which can escape through shielding causing a system to fail EMC tests. Fields around a conductor are proportional to voltage or current, which are small in the case of LVDS. The fields are distorted by and interact with their environment, which is why EMI is so hard to predict. The fields can be distorted to advantage, however, and such is the case with tightly coupled differential lines ("+" and "–" signals in close proximity with one another). In single-ended lines like CMOS/TTL shown below, almost all the electric field lines are free to radiate away from the conductor. These fields may be intercepted by other objects, but some can travel as TEM waves which may escape the system causing EMC problems.



Electromagnetic field cancellation in differential signals (b) through coupling versus a single-ended signal (a).

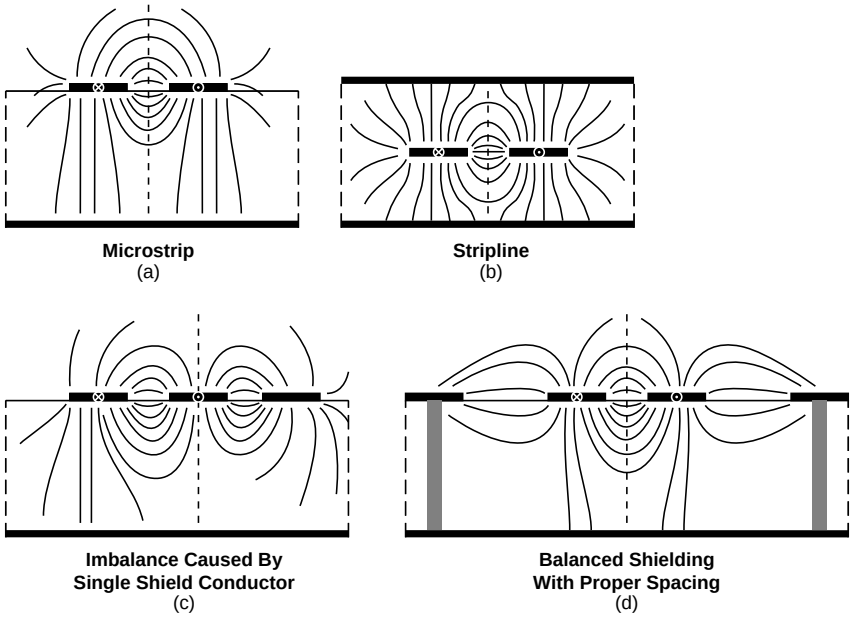
Balanced differential lines, however, have equal but opposite ("odd" mode) signals. This means that the concentric magnetic fields lines tend to cancel and the electric fields (shown above) tend to couple. These coupled electric fields are "tied up" and cannot escape to propagate as TEM waves beyond the immediate vicinity of the conductors. Only the stray fringing fields are allowed to escape to the far field. Therefore, for coupled differential signals much less field energy is available to propagate as TEM waves versus single-ended lines. The closer the "+" and "–" signals, the tighter or better the coupling.



Even or common mode signals (a), ideal equal and opposite odd mode signals (b), and unbalanced signals (c) on differential lines.

Clearly, the voltages and currents of the two ("+" and "–") conductors are not always equal and opposite. For LVDS, the DC currents should never flow in the same direction as in (a) above, but factors can cause an imbalance in currents (c) versus the ideal case in (b). When this imbalance happens, an excess of field fringing occurs since the field strength of the two conductors is unequal. The extra fringe fields can escape as TEM waves and lead to more EMI.

Similar effects can be seen in microstrip and stripline PCB traces shown below. The ideal cases for microstrip and stripline are represented by (a) and (b). Here we see that the microstrip ground plane helps couple additional field lines from below, tying up more field lines and reducing EMI. Stripline almost completely shields the conductors and therefore can significantly decrease EMI, but has the penalty of slower propagation velocity (about 40% slower than microstrip), more PCB layers, additional vias, and difficulty in achieving 100Ω Z_{0DIFF}. More shielding can be achieved using microstrip without significantly impacting propagation velocity using shield traces as in (d), but be careful to add the shield trace (preferably ground) on both sides of the pair (d). Running the shield trace — or any trace — on one side (c) creates an imbalance which can increase EMI. Ground trace shields should have frequent vias to the underlying ground plane at regular (<1/4 wavelength) intervals, and should be placed at least 2s from the pair.

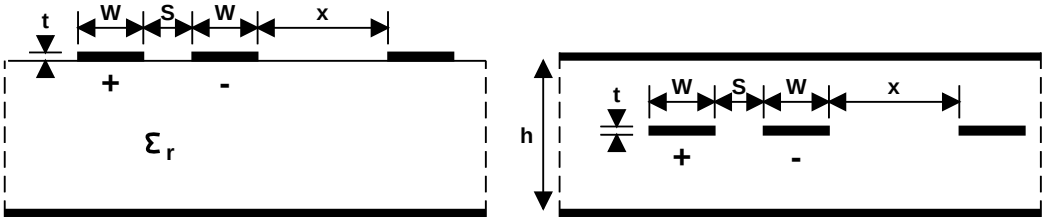


Ideal differential signals on microstrip a) and stripline (b), negative effects of unbalanced shielding (c), and positive effects of balanced shielding (d).

4.3.3 Design Practices for Low EMI

As discussed in the preceding paragraphs, the two most important factors to consider when designing differential signals for low EMI are close coupling between the conductors of each pair and minimizing the imbalances between the conductors of each pair. Let us discuss close coupling first.

In order for sufficient coupling to occur, the space between the conductors of a pair should be kept to a minimum as shown below. (Note that matched transmission impedance must also be maintained). Stripline power and ground planes/traces should not be closer than the distance between conductors to preserve closer coupling between the conductors versus the power and ground planes. A good rule is to keep S < W, S < h, and x greater or equal to the larger of 2S or 2W. The best practice is to use the closest spacing, "S," allowed by your PCB vendor and then adjust trace widths, "W," to control differential impedance.

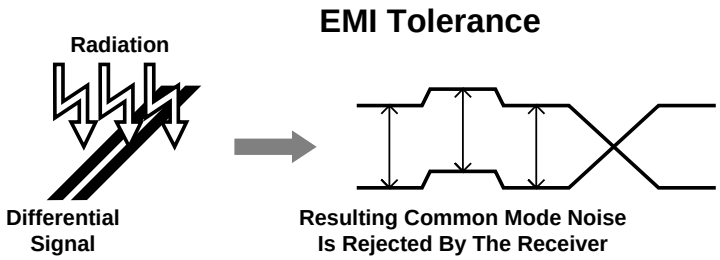


Microstrip **Stripline**

For good coupling, make S < 2W, S < h, and x ≥ 2W & 2S.

For sufficient coupling (cancelling) of electromagnetic fields, "+" and "–" signal distance must be minimized.

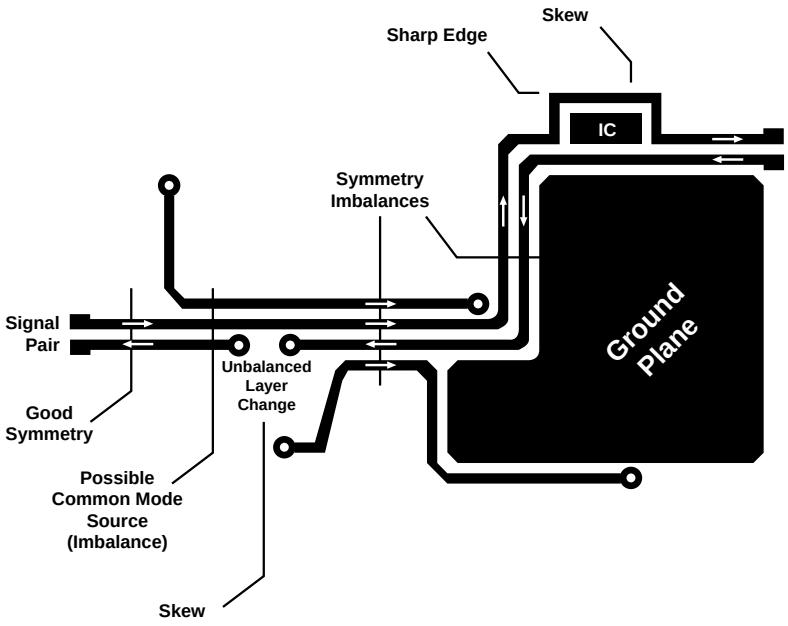
Close coupling between conductors of a pair not only reduces EMI, but it helps to ensure noise coupled onto the conductors will do so equally as common mode noise which will then be rejected by the receiver. Since the differential pair is a current loop, minimizing conductor spacing also reduces the antenna loop.



Close coupling not only reduces EMI, but improves EMI tolerance too.

Imbalance minimization is the other important factor in reducing EMI. Although fields result from the complex interaction between objects of a system and are difficult to predict (especially in the dynamic case), certain generalizations can be made. The impedance of your signal traces should be well-controlled. If the impedance of one trace changes versus another, the voltage and fields of one signal will be different from its partner. This will tend to create more fringing fields and therefore more EMI as we have seen.

The basic rule to follow is: if any discontinuity must be introduced in proximity to differential lines, it should introduced equally to both members of the pair. Examples of discontinuities include: components, vias, power and ground planes, PCB traces, etc. Remember, the key word is **balance**.



This PCB layout contains many sources of differential signal imbalance that will tend to increase electromagnetic radiation.

Unfortunately unless you have an elaborate EMI lab, fields resulting from imbalances cannot easily be measured. Waveforms, however, are easy to measure. Since fields are proportional to voltage/current amplitude at any given point in time, any factors affecting the time (delay, velocity, etc.) and/or amplitude (attenuation, etc.) properties of the signals can increase EMI and can be seen on a scope. The next figure illustrates how waveforms — easily seen on a scope — can help predict far field EMI. First, the beneficial field cancelling effects of ideal differential signals (b) versus single-ended signals (a) are compared.

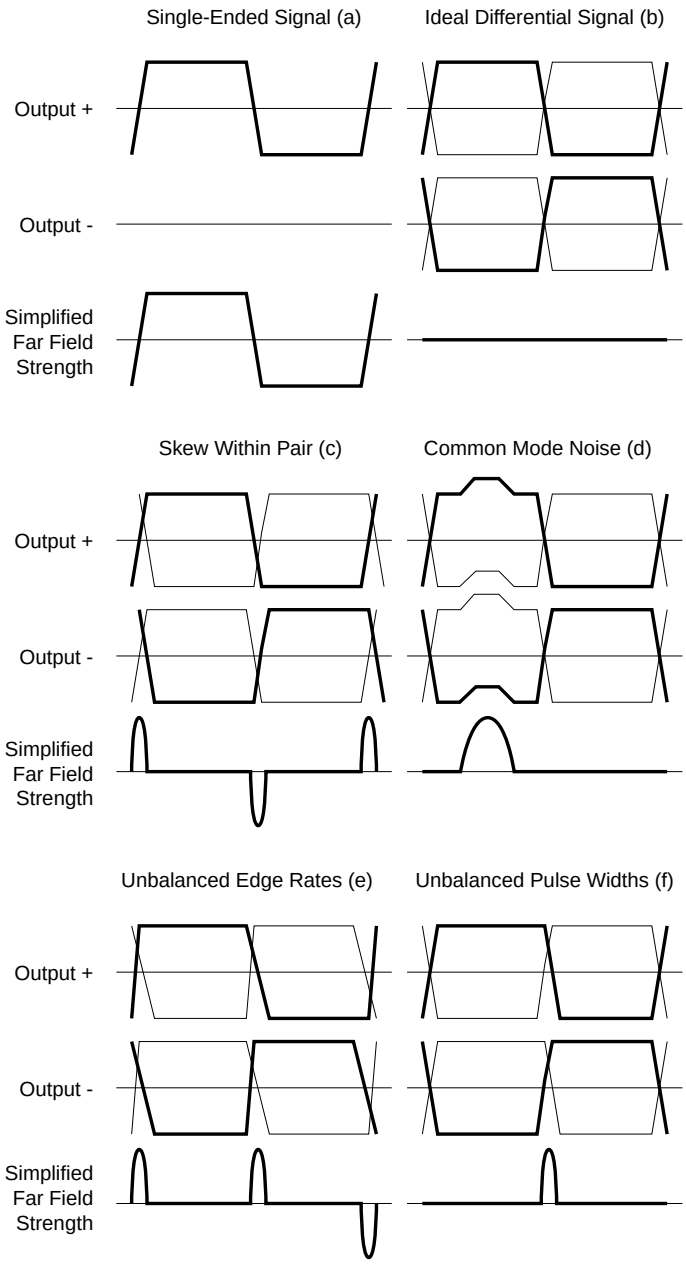
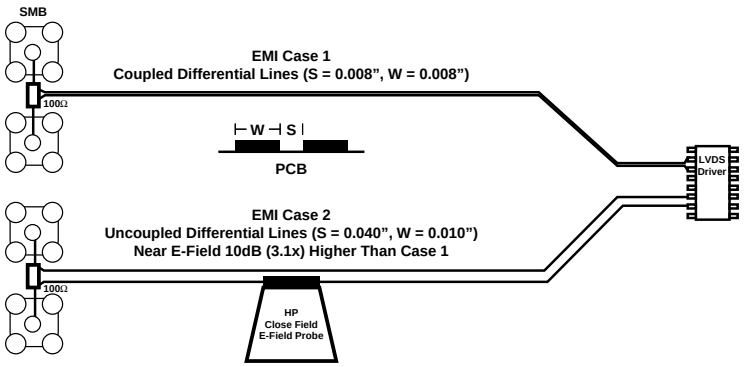


Diagram showing simplified far field radiation under various situations.

A real differential signal, however, is non-ideal and contains skew, unbalanced pulse widths and edge rates, common mode noise, unbalanced attenuation, etc. These affect the relative amplitudes of the fields at any given moment, reducing the cancelling effects of the differential signals, and potentially increasing EMI. Thus, the waveforms of one conductor of a pair should balance or mirror the other to minimize EMI.

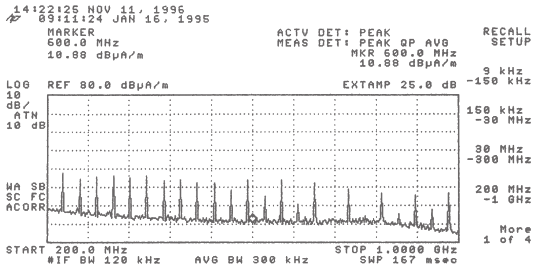
4.3.4 EMI Test Results

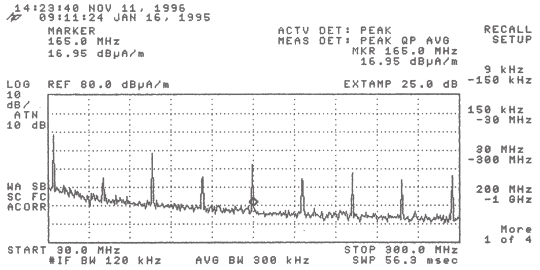
The PCB setup shown below was used to examine the effects on EMI of closely coupled differential signals versus uncoupled signals. The setup compares two sets of LVDS signals: one set in which pair spacing is less than trace width (S<W) and another set in which S>>W so that the pair members are no longer closely coupled (though the differential impedance of the transmission line is still 100Ω).



EMI Test Setup

Near (close) field electric field measurements were made for both cases while using a 32.5MHz 50% duty cycle clock as the source. The two plots below show the E-field strength results for case 2, the uncoupled case. The first plot shows the E-field strength over 200MHz to 1GHz. The second plot looks more closely at the frequencies between 30MHz and 300MHz. The electric field noise shows up as "spikes" which occur at harmonics of the input frequency.

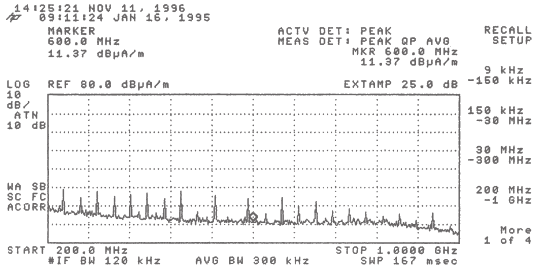


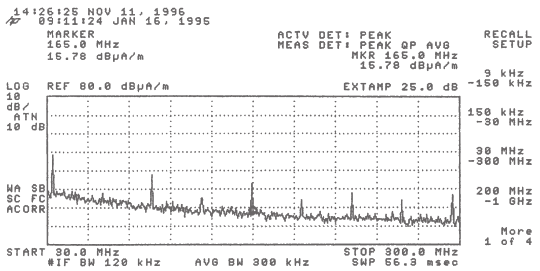


Near E-Field Strength for Uncoupled Signals

(Case 2): 200MHz-1GHz *(Case 2): 30MHz-300MHz*

The next two plots show the E-field strength for case 1 in which the differential pair is closely coupled. Notice that the harmonics are significantly reduced.





Near E-Field Strength for Closely Coupled Signals

(Case 1): 200MHz-1GHz *(Case 1): 30MHz-300MHz*

In the far field, the EMI of the closely coupled pair should radiate much less due to the coupling of the electric fields. Even in the near field, however, the closely coupled pair generated much weaker electric fields. The closely coupled pair showed about 10dB (>3 times) lower electric field strength than the uncoupled pair.

This test illustrates two things:

1) Use of differential signals versus single-ended signals can be used effectively to reduce emissions.

2) The EMI advantages of differential signs will be lost or greatly diminished unless the signals are closely coupled.

This test used uncoupled LVDS signals to represent single-ended signals. Most single-ended signals such as TTL or GTL, have a much greater swing and involve much greater currents, so their EMI is expected to be even greater than is seen here.

4.3.5 Ground Return Paths

A conductor that carries current requires an opposite mirror current to return through some part of the system. This return current path will be the path of least impedance.

Since LVDS is differential, differential current that flows in one conductor of a pair will flow back through the other conductor, completing the current loop. This is ideal, because the current return antenna loop area is minimized since the traces of a pair are closely spaced. Real signals, however, will have some common mode noise current which must return also. This common mode current will be capacitively coupled to ground and return to the driver through the path of least impedance. Therefore, a short ground current return path is needed between the driver and receiver in differential systems as well as single-ended (though to a lesser extent).

On PCBs, the best current return path is a uniform, unbroken ground plane beneath the LVDS signals. The ground plane will allow the common mode (even mode) current to return directly under the LVDS signals. This closely coupled path is the path of least impedance and means that the current loop area is minimized.

Similarly, in cable ground return wire or wires should be used between driver and receiver. This allows the return path to be in close proximity to the signal pairs reducing the current loop area (see Chapter 5).

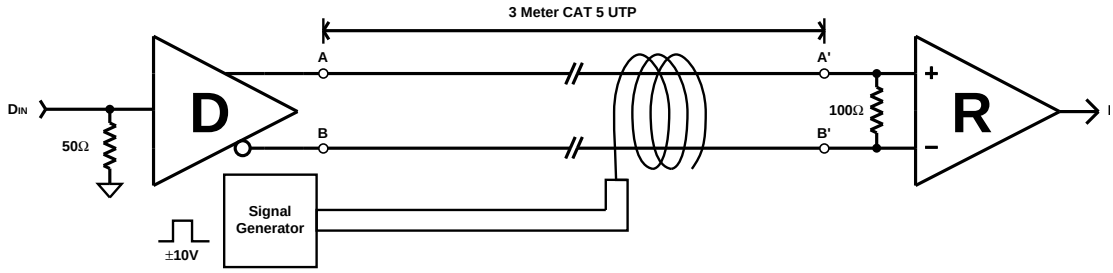
4.3.6 Cable Shielding

Shielding is an effective way to reduce EMI. Shielding should be connected directly to both driver enclosure and receiver enclosure when possible. Many shields are not designed to handle significant ground return currents, so it may be necessary to construct a filter network which isolates the shield from ground at one end (see Chapter 5).

4.3.7 Conclusion

To take advantage of the inherent low EMI properties of LVDS, designers should ensure the conductors of each pair are (1) closely coupled and (2), well-balanced. Impedance, both single-ended and differential, should be controlled.

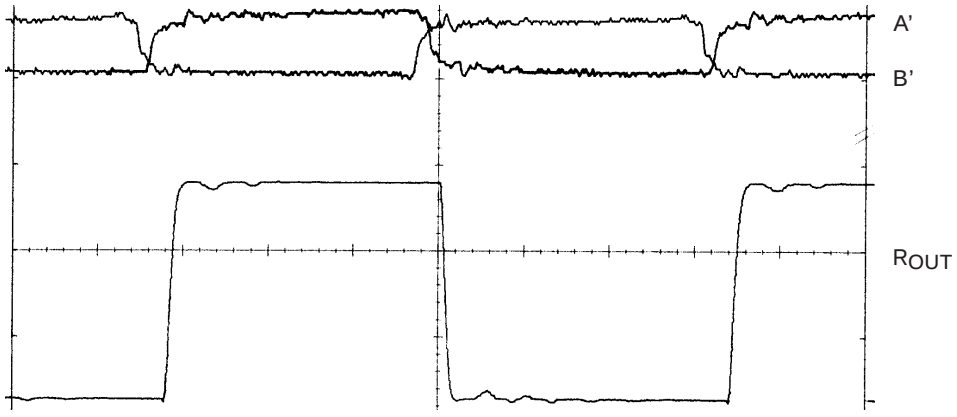
4.4.0 COMMON MODE NOISE REJECTION



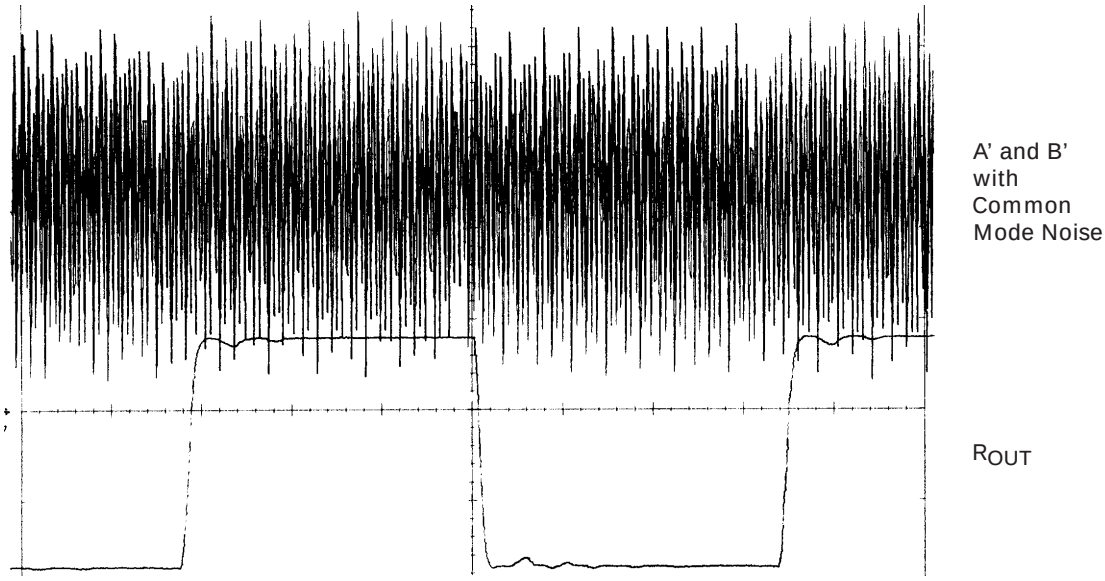
Common mode noise rejection test setup.

Test Setup:
Driver: DS90C031 (one channel)
Receiver: DS90C032 (one channel)
V_{CC} = 5V
T = 25°C

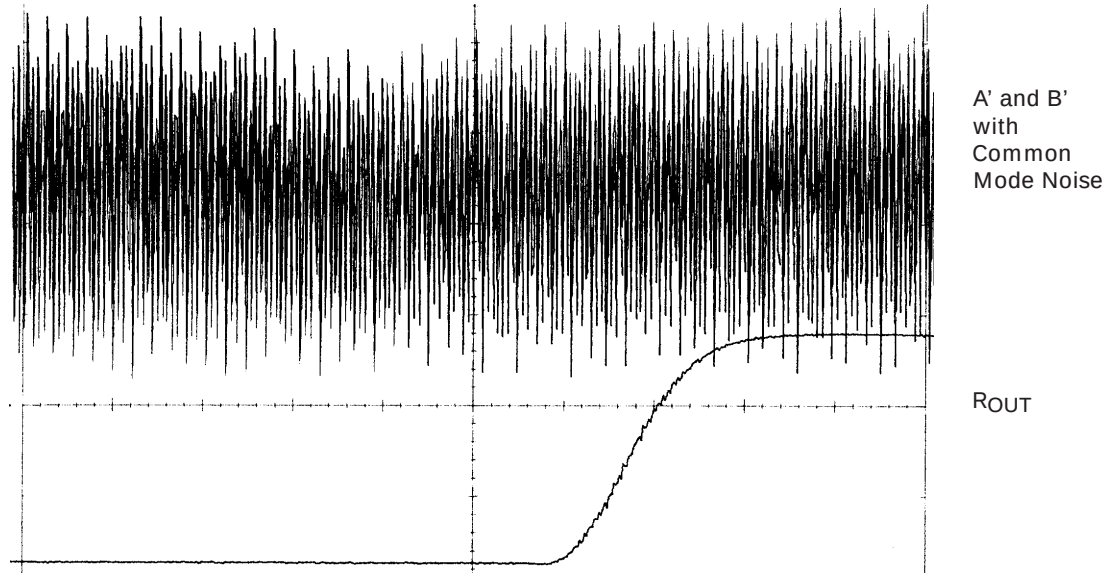
This test demonstrates the common mode noise rejection ability of National's LVDS receivers. Some have expressed concern over the noise immunity of LVDS because of its low voltage swing (≈±350mV swing with <±100mV thresholds). Provided that the differential signals run close together through controlled impedance media, however, most of the noise on LVDS lines will be common mode. In other words, EMI, crosstalk, power/ground shifts, etc. will appear equally on each pair and this common mode noise will be rejected by the receiver. The plots below show common mode noise rejection with VCM noise up to –0.5V to +3.25V peak-to-peak.



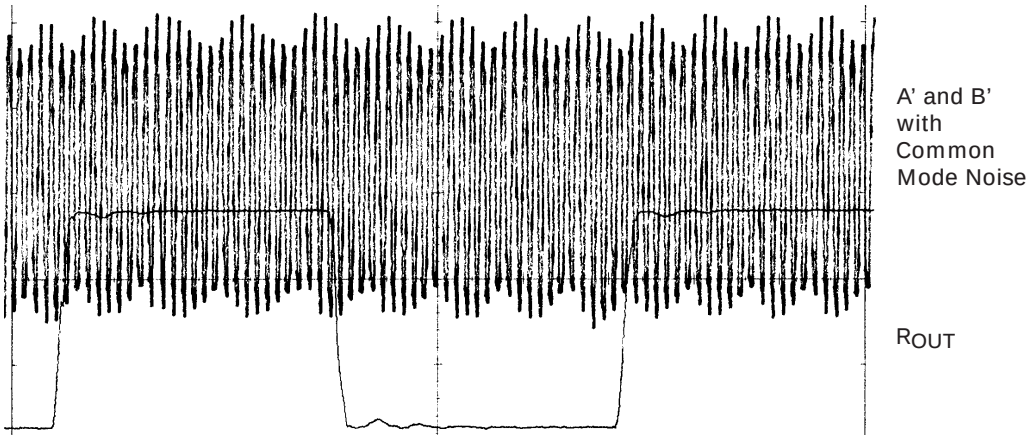
Reference waveform showing LVDS signal and receiver output.



Coupled common mode noise of 0.5V to 1.75V peak-to-peak and resulting clean receiver output.

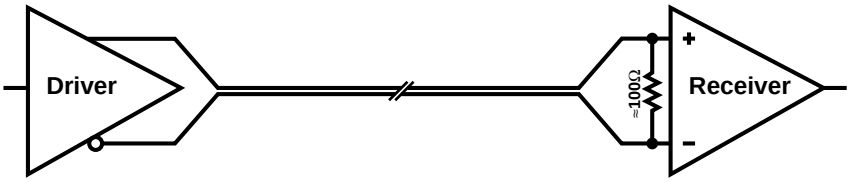


Expanded view of coupled common mode noise waveform and clean receiver output.



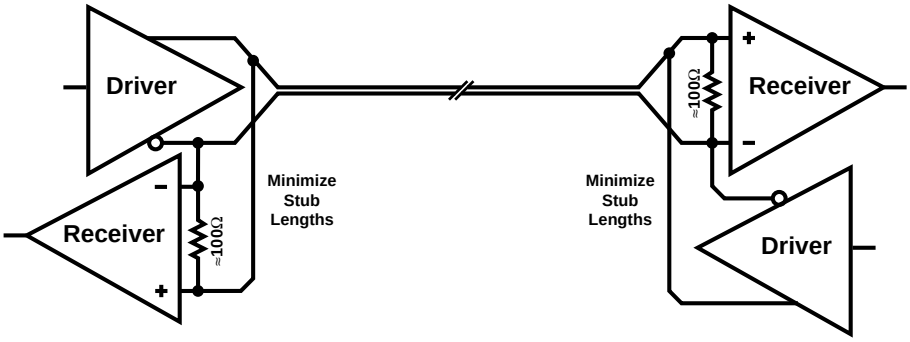
Clean receiver output despite –0.5V to +3.25V peak-to-peak common mode noise.

4.5.0 LVDS CONFIGURATIONS

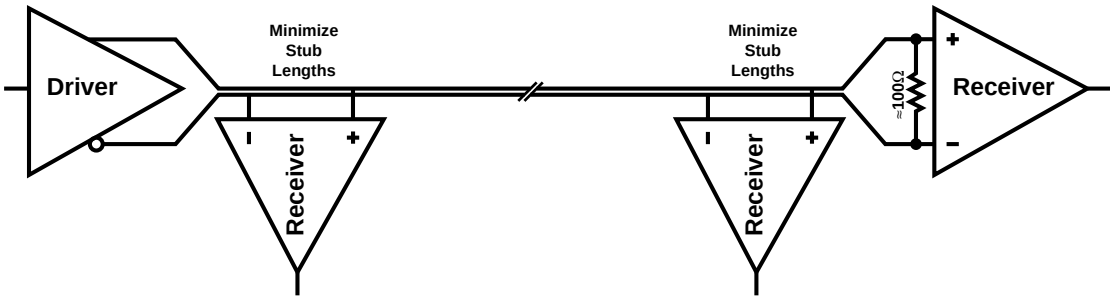


Point-to-point configuration.

Although LVDS drivers and receivers are typically used in a point-to-point arrangement (above), other topologies are possible. The configuration shown below allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin), so this configuration should be considered only where noise is low and transmission distance is short (≤10m). Typical LVDS I/O capacitances are 5-7 pF for receiver inputs and 3.5-4pF for driver outputs.



Bi-directional half-duplex configuration.



Multidrop configuration.

Since LVDS receivers have high impedance inputs, a multidrop configuration can also be used if transmission distance is short and stub lengths are less than 12mm (<7mm is recommended). Use receivers with power-off high impedance if the network needs to remain active when one or more nodes are powered down.

4.6.0 FAIL-SAFE FEATURE

4.6.1 Most Applications

To help ensure reliability, LVDS receivers have internal fail-safe circuitry that forces the output to be in a known logic state (HIGH) under certain fault conditions. These conditions include open, shorted, and terminated receiver inputs. Here is a summary of LVDS fail-safe conditions:

1) Open Input Pins
   Unused receiver inputs should be left OPEN. Do not tie unused receiver inputs to ground or other voltages. The internal failsafe bias resistors will pull the "+" input high, and the "–" input low, thus guaranteeing a high, stable output state.

2a) Terminated Input Pins
   If the driver is in a TRI-STATE® condition, in a power-off condition, or is disconnected (cable unplugged), the receiver output will be in a high state, even with the termination resistor across the input pins.

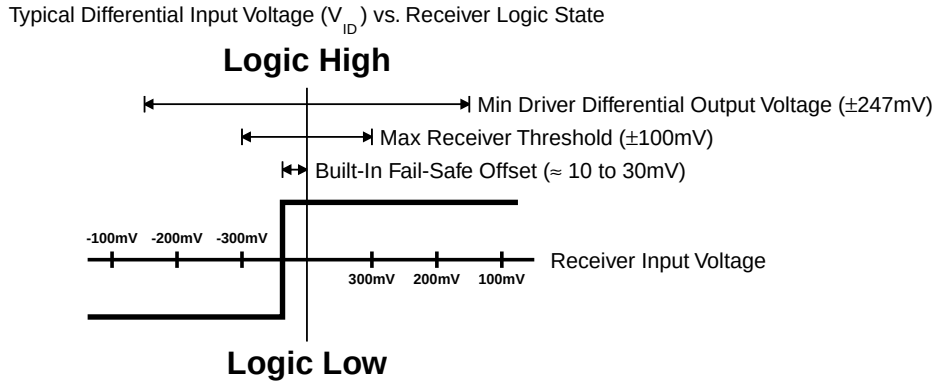
2b) Terminated Input Pins — Noisy Environments
   See section 4.6.2 if fail-safe must be guaranteed in noisy environments when the cable is disconnected from the driver end or the driver is in TRI-STATE®.

3) Shorted Inputs
   The receiver output will remain in a high state when the inputs are shorted.

4.6.2 Boosting Fail-Safe In Noisy Environments

The internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection for floating receiver inputs, shorted receiver inputs, and terminated receiver inputs. It is not designed to provide fail-safe in noisy environments when the cable is disconnected from the driver end or the driver is TRI-STATE. When this happens, the cable becomes a floating antenna which can pick up noise. If the cable picks up more differential noise than the internal fail-safe circuitry can overcome, the receiver may switch or oscillate. If this condition can happen in your application, it is recommended that you choose a balanced and/or shielded cable which will reduce the amount of differential noise on the cable. In addition, you may wish to add external fail-safe resistors to create a larger noise margin. However, adding more fail-safe current will tend to unbalance the symmetrical LVDS output drive (loop) current and degrade signal quality somewhat. Therefore a compromise should be the ultimate goal.

4.6.3 Choosing External Fail-Safe Resistors



External fail-safe can be added, but must be small enough not to significantly affect driver current.

The chart above shows that National's present LVDS devices typically have an internal fail-safe voltage of about 10 to 30mV. If the receiver will not always be driven by the driver in your application and the cable is expected to pick up more than 10mV of differential (not common mode) noise you may need to add additional fail-safe resistors. The resistors are chosen by first measuring the amount of differential mode noise you will need to overcome, V_{FSB}, by biasing the termination resistor (≈100Ω) to generate this voltage. Note that you do not need to provide a bias, V_{FSB}, which is greater than the receiver threshold (100mV). You only need enough to overcome the differential noise, since the internal fail-safe circuitry will always guarantee a positive offset. In fact, making V_{FSB} too large will contend with the driver output causing the driven signal to become imbalanced and reduce signal quality.

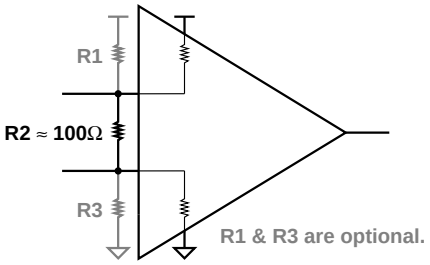


Diagram showing simplified internal fail-safe circuitry and optional external "helper" fail-safe resistors.

For best results, follow these procedures when choosing external fail-safe resistors:

1) First ask the question "Do I need external fail-safe?" If your LVDS driver is always active, you will not need external fail-safe. If the cable is never disconnected from the driver end while the system is active and/or your cable will not pick up much differential mode noise you may not need to boost fail-safe.

2) Measure the amount of **differential (odd) mode** noise at the receiver end of the cable in worst case conditions. If you have a lot of noise, **use a balanced cable** like twisted pair which tends to pick up mostly common mode noise , not differential mode noise. Do not use simple ribbon or coax cables which can pick up differential mode noise.

   Use a **shielded cable** if possible. Using a balanced and/or shielded cable is best way to prevent instead of fix the noise issue!

3) Once you have chosen the appropriate cable, measure the amount of differential voltage at the receiver under worst case conditions. Set this equal to V_{FSB} in the equation below and solve for the external fail-safe resistors R1 and R3.

$$V_{FSB} = \frac{R2}{R1 + R2 + R3} V_{CC}$$

$$I_{BIAS} = \frac{V_{CC}}{R1 + R2 + R3} << I_{LOOP} \quad (\text{Use } I_{BIAS} \leq 0.1 * I_{LOOP})$$

$$V_{CM} = \frac{R3 + R2/2}{R1 + R2 + R3} V_{CC} = 1.2V \implies R1 \approx R3 \left(\frac{V_{CC}}{1.2V} - 1 \right)$$

$$R_{TEQ} = \frac{R2\,(R1 + R3)}{R1 + R2 + R3} = \text{match transmission line } Z_{0DIFF}$$

4) You now have an equation relating R1 to R3. Choose R1 and R2 so that: (1) they approximately satisfy the third equation for V_{CM} = 1.2V, and (2) they are large enough that they do not create a bias which will contend with the driver current (I_{BIAS} << I_{LOOP}, equation two). In general, R1 and R2 should be greater than 20kΩ for V_{CC} = 5V and greater than 12kΩ for V_{CC} = 3.3V. **Remember that you want just enough I_{BIAS} to overcome the differential noise, but not enough to significantly affect signal quality.**

5) The external fail-safe resistors may change your equivalent termination resistance, R_{TEQ}. Fine tune the value of R2 to match R_{TEQ} to within about 10% of your differential transmission line impedance.

4.7.0 POWER OFF HIGH IMPEDANCE

Power off high impedance is a useful feature:

1) For receivers which might be powered down while the driver is active. Note that since LVDS drivers only source about 3.5mA of current, NOT having power off high impedance may be acceptable.

2) For receivers in multi-drop mode when the network must remain operational if one or more receivers are powered down.

3) For drivers, receivers, and transceivers in multi-point or bidirectional applications when the network must remain operational if one or more receivers are powered down or live insertion capability is desired.

LVDS devices will behave differently during power down. Here is a summary of power off conditions and the results to various devices:

a) Driver power OFF, receiver power ON:

- LVDS receivers have fail-safe to avoid oscillation.
- LVDS quad, dual, and single receivers outputs will be locked to logic high.
- LVDS Channel Link and FPD-Link device outputs will remain in last known state until clocked at which point the outputs will lock high.
- Some driver outputs will power off to high impedance (check datasheet).

b) Driver power ON, receiver power OFF:

- 5V receivers will sink driver current, but since this current is small, it will not damage the driver (transmitter) or receiver.
- 3V receiver inputs will power off to high impedance.